Prepared by
SEM/CVBEP JACKY LIU
Contents responsible if other than preparer

Approved by
SEM/CVBEP (DAVID XU)

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Susan technical description

Technical description of transceiver units:

Type Number: AAD-3880065-BV
FCC ID: PY7A3880065
IC Number: 4170B-A3880065
Marketing Name:
Band: Quad EDGE/GSM/GPRS 850/900/1800/1900 and W-CDMA band I/VIII

Type Number: AAD-3880067-BV
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IC Number: 4170B-A3880067
Marketing Name:
Band: Quad EDGE/GSM/GPRS 850/900/1800/1900 and W-CDMA band I

Contents

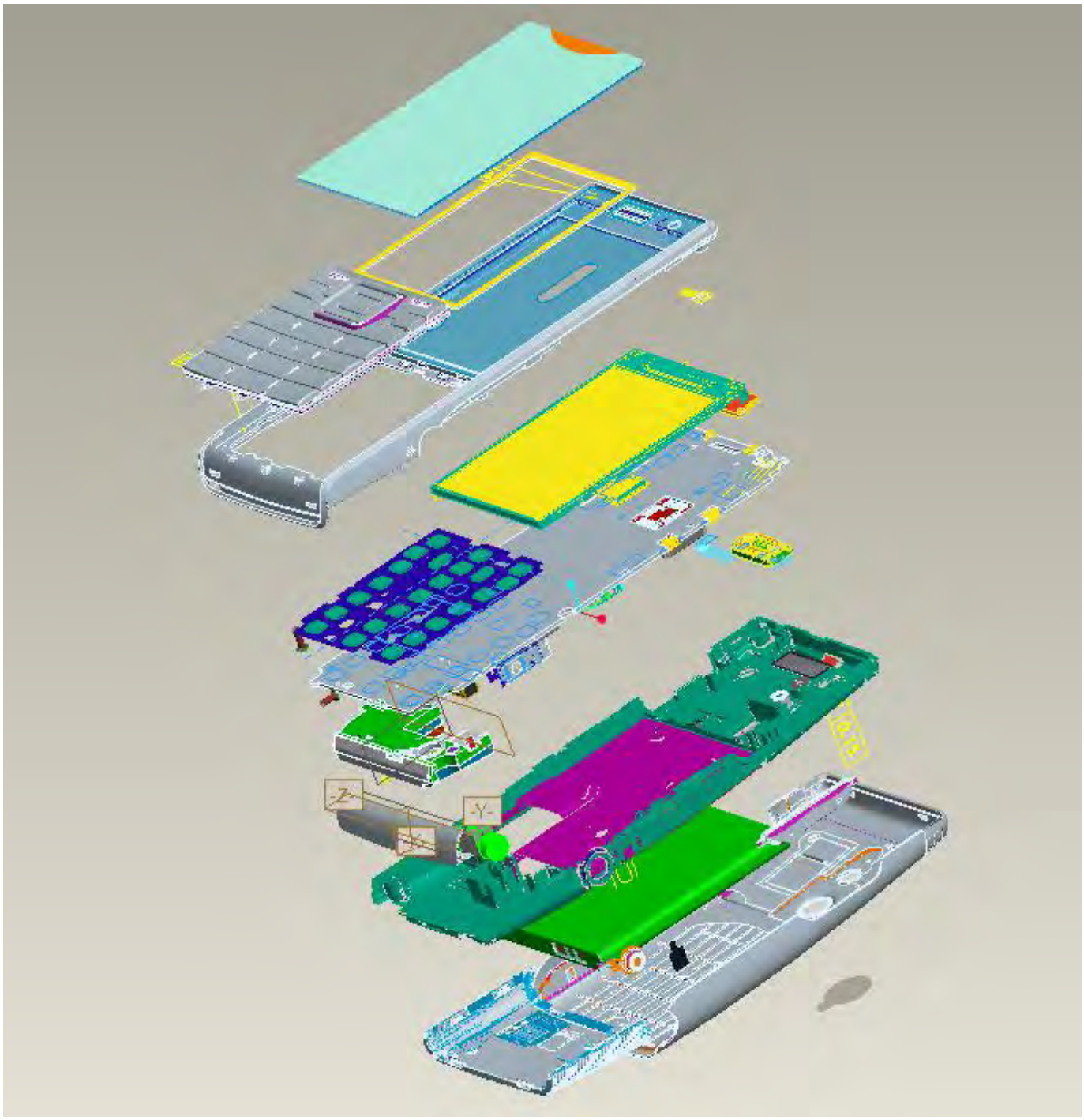
1 Mechanical concept

The mobile phone is a “Bar-type” Phone. The main PCB contains all GSM/GPRS/EDGE/W-CDMA transceiver functionality, including SIM reader and micro SD memory card. The main PCB does also host Bluetooth™ & W-LAN antenna, as well as a GPS receiver on top. The 5Mpixel camera is connected to the main board with a socket.

The battery fits in a dedicated cavity and is covered with a battery cover.

Dimensions

Length	110 mm
Width	45 mm
Thickness	13.85 mm
Weight	90g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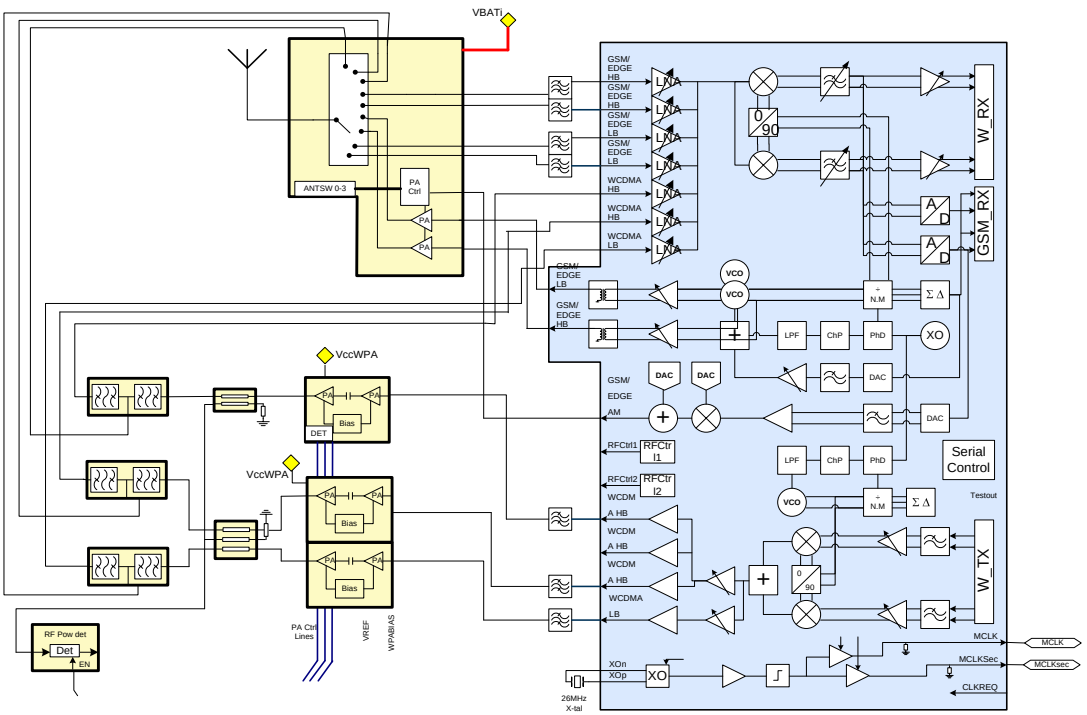
2 Radio concept

The system supports a quad EDGE/GSM/GPRS solution (850, 900, 1800, 1900 MHz). The system does also include UMTS/HSPA, FDD W-CDMA for Band I (uplink 1900 MHz, downlink 2100 MHz), and Band VIII (900 MHz). It supports a maximum packet data raw downlink throughput of 7.2Mbps in HSDPA, a maximum packet data raw uplink throughput of 2.0Mbps in HSUPA. MPR (maximum power reduction) is supported for HSDPA and HSUPA.

Regarding 2G support, the device is an EGPRS class 10 terminal supporting packet switched (PS) data. In 3G mode the device supports UMTS release 99 (both CS and PS data), plus HSDPA category 8 and HSUPA category 5.
Sony Ericsson´s HSPA/UMTS/EDGE product is designed to be compliant to all mandatory 3GPP Release 99 requirements in addition to all mandatory release 5 requirements for HSDPA and any mandatory release 6 requirements for HSUPA.

The actual phone can be delivered Quad EDGE/GSM/GPRS and W-CDMA band I and VIII or Quad EDGE/GSM/GPRS and W-CDMA band I, II and V. The actual configuration is controlled by SW settings and HW configuration by choice of number of WCDMA power amplifiers, TX-SAW filters and duplex filters (see type numbers at page 1).



2.1 Front End

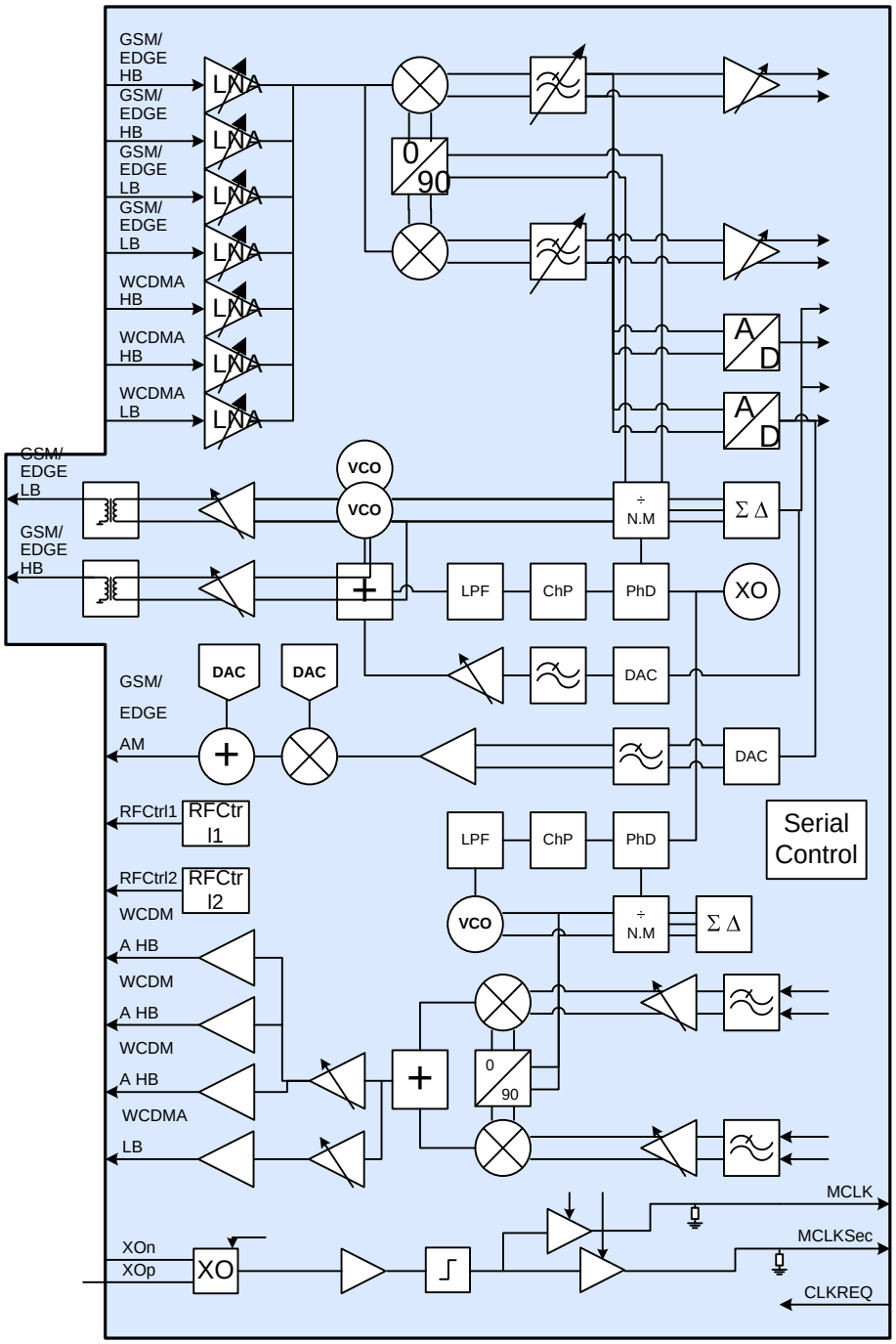
A single antenna is used for all bands. The single antenna is used for all transmission and reception.

The Front End block connects the proper block in the radio system to the antenna. The Front End has two inputs for EDGE/GSM/GPRS, one for low band (850/900 MHz) and one for high band (1800/1900 MHz). The EDGE/GSM/GPRS power amplifier output is filtered by a low pass filter in the Front End and then connected to the antenna through a switch. In receive mode, the EDGE/GSM/GPRS signal from the antenna passes through the switch to one of the four receive SAW filters. The SAW filter provide receive band selectivity.

In GSM/GRPS/EDGE systems, transmit and receive operations are divided in time and the switch connects the proper block in accordance with the mode of operation (that is, transmit or receive; one at a time).

In WCDMA the transmit outputs from the WCDMA transceiver are filtered by a SAW filter that cleans up the spectrum. The SAW filter output is connected to the power amplifier, one for each band. For power control, a sample of the transmit output is taken by a directional coupler and converted to a DC level by the power detection circuit. This signal is used to control the transmitter output power. The transmit signal passes through a duplexer. The duplexer output is selected by the switch in the Front End for connection to the antenna. In WCDMA receive mode the signal from the antenna is switched by the Front End to the correct duplexer. The output from the duplexer is connected to the LNA input in the WCDMA receiver.

2.2 Transceiver



The transceiver is a multi-mode transceiver for WCDMA/EGDE/GPRS/GSM.

The EDGE/GPRS/GSM part of the transceiver use a digital baseband interface that is shared between received and transmitted data. The receive interface is based on I and Q data and the transmitter interface is based on envelope and frequency data.

The WCDMA part of the transceiver use differential analog in-phase and quadrature phase interfaces that are an IQ-interface, in the receiver and the transmitter data paths.

The EDGE/GSM/GPRS part of the transceiver has the following general features:

• Power class

- GMSK low bands: Class 4 (33 dBm)

- GMSK high bands: Class 1 (30 dBm)

- 8PSK low bands: Class E2 (27 dBm)

- 8PSK high bands: Class E2 (26 dBm)

- WCDMA: class 3 (+24dBm)

• EDGE/GPRS Multi slot class 10

• Zero-IF receiver

• EDGE/GPRS/GSM Polar modulation transmitter

• WCDMA direct IQ modulation transmitter

2.2.1 Frequency Generation

The 26 MHz reference signal is used as the reference for the on-chip synthesizers. To cover the required frequency range, the integrated Voltage Controlled Oscillator (VCO) operates at twice the frequency for band 1800/1900/2100, and at four times the desired frequency for band 800/900. The two synthesizers are controlled through the serial bus from the access side of the digital baseband controller.

2.2.2 EDGE/GPRS/GSM Transmitter Part

Polar modulation transmitter architecture based on the direct phase/frequency modulation/synthesizer architecture is used for GSM, GPRS and EDGE. This architecture has the capability of generating both the GSM/GPRS constant envelope GMSK modulation and the linear EDGE 8-PSK modulation.

The phase/frequency modulator is a sigma-delta controlled fractional-N frequency synthesizer with an additional frequency insertion point after the loop filter at the input of the VCO. The Phase-locked Loop (PLL) has two information inputs: the divider ratio in the feedback path and a direct path to the VCO. The phase locked loop generates the radio frequency carrier including the phase modulation information at the desired channel frequency.

2.2.3 WCDMA Transmitter Part

The WCDMA transmitter architecture is an on frequency linear direct up-conversion IQ-modulator. The in-phase and quadrature-phase reconstruction filters are fully integrated and a programmable gain amplifier implements the gain control. A SAW filter between the WCDMA circuit and the power amplifier is used to improve noise performance. After the power amplifier, the signal is sent through a duplex filter, which directs the transmit signal to the antenna connector through the antenna switch.

The supply voltage and bias of the power amplifier are adapted depending on the output power to achieve high efficiency at every transmitter power level. A high efficiency DC/DC converter regulates the supply voltage and the bias operation point is controlled by a D/A-converter in the WCDMA radio circuit.

2.2.4 Receiver Part

The receiver architecture is a direct down-conversion zero-IF receiver with integrated low pass filters. The complete receiver with seven Low Noise Amplifiers (LNAs), one for each supported band, is integrated on chip. After the down-conversion, the in-phase and quadrature-phase components are low pass filtered and if the receiver is in EDGE/GPRS/GSM mode the signals are fed to the integrated high dynamic range sigma-delta A/D-converters.

2.2.5 Control Flow

The access side of the digital baseband controller controls the radio system.

In both EDGE/GSM/GPRS and W-CDMA air interface mode the digital baseband controller controls the radio system through a three-wire serial bus.

The digital baseband controller also manages PA band control and antenna switch mechanism in the Front End.

The 26 MHz VCXO clock residing in the EDGE/GSM/GPRS/W-CDMA transceiver is turned on only when required, the digital baseband controller initiates this.

The EDGE/GSM/GPRS/W-CDMA RF system requires control which is temperature dependent. The temperature within the RF system is estimated by a voltage measurement performed by the analog baseband controller.

3 Digital Baseband Control

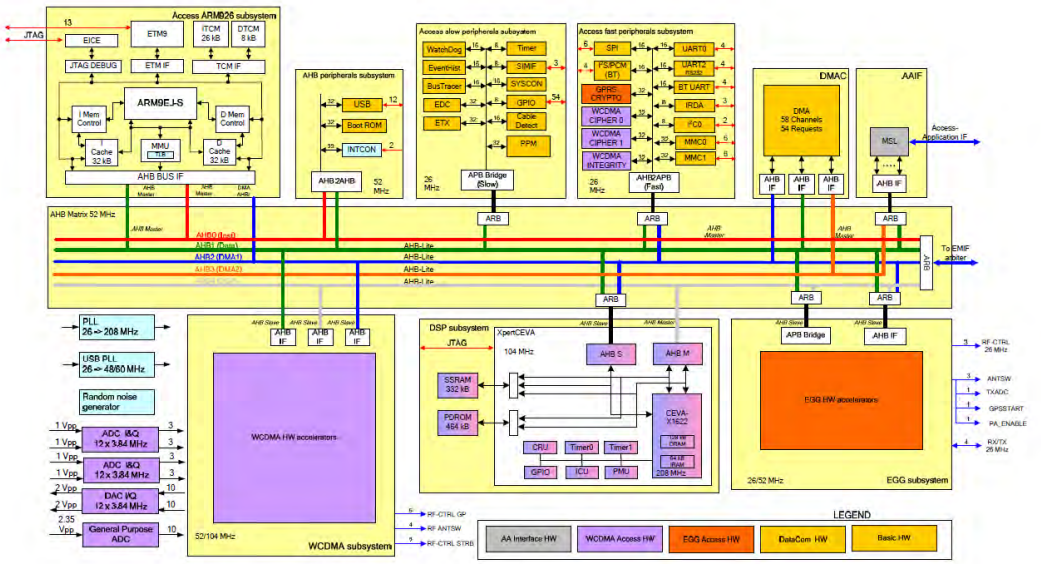
The digital baseband controller is the main controller of the platform. It has the following features:

- CPU subsystem including two ARM CPUs, 208 MHz
- Access DSP system, 208 MHz

- Memory bus structure, 104 MHz

The digital baseband controller is equipped with two ARM CPUs; one dedicated for the Access subsystem, the other for the Application subsystem. Each CPU includes a Direct Memory access (DMA) controller, Tightly Coupled Memory (TCM), boot ROM and backplane bus fabric.

3.1 Access subsystem



All modem functionality in the digital baseband controller resides in the Access subsystem. This includes EDGE/GSM/GPRS interface, W-CDMA interface, USB and other peripheral modules. The Control CPU is an ARM and a DSP used for signal processing and layer 1 control code.

The main communication between the blocks in the Access subsystem is done through the Advanced High-performance Bus (AHB) matrix, which is a set of connecting the different parts together.

A block called Syscon is responsible for distributing clocks and resets to all parts of the Access subsystem. This block is under SW control.

The Access subsystem is connected to the Shared EMIF, an interface for communication with external SDRAM. The Shared EMIF is shared between the Access subsystem and the Application subsystem.

The Access subsystem contains among others the following blocks:

- CPU

  The CPU block contains a CPU with 32 kB instruction cache, 32 kB data cache and a MMU. All runs at 208MHz.

- DSP

The DSP block provides support for processor intensive activities such as voice coding and audio decoding. The core part is running at maximum 208 MHz the rest at 104 MHz. Master and slave AHB bus interfaces are running at 52MHz.

- EDGE, GSM and GPRS

  The EDGE/GSM/GPRS subsystem (EGG) includes the complete functionality for the digital paths of the EGG receiver and transmitter paths. This includes several HW accelerators and a dedicated DMA controller for data transfers within EGG. The subsystem is controlled through two AHB slave interfaces; one for register setup, and one for data communication between the DSP and the EGG internal memory.

- W-CDMA

  The W-CDMA block includes the complete functionality for the digital parts of the W-CDMA receiver and transmitter paths. This includes several HW accelerators, a control sequencer, and a dedicated DMA controller for data transfers within W-CDMA. The block is controlled through three AHB slave interfaces; one for register setup, one for data communication, between DSP and internal memory, and one for dedicated Rake memory.

- Access DMAC

  The Access DMAC is a DMA controller used to transfer data between different blocks within the Access subsystem.

- AAIF

  The Access-Application interface (AAIF) is used for communication between the CPUs in the Access and Application subsystems and for data transfers between them.

- AHB bus matrix

  The AHB bus matrix is a set of AHB busses connected to AHB masters and slaves in the Access subsystem. Each AHB master has ownership of one AHB bus and these are in priority order:

  1. CPU instruction
  2. CPU data
  3. DSP
  4. DMA controller
  5. DMA AAIF

- AHB peripheral

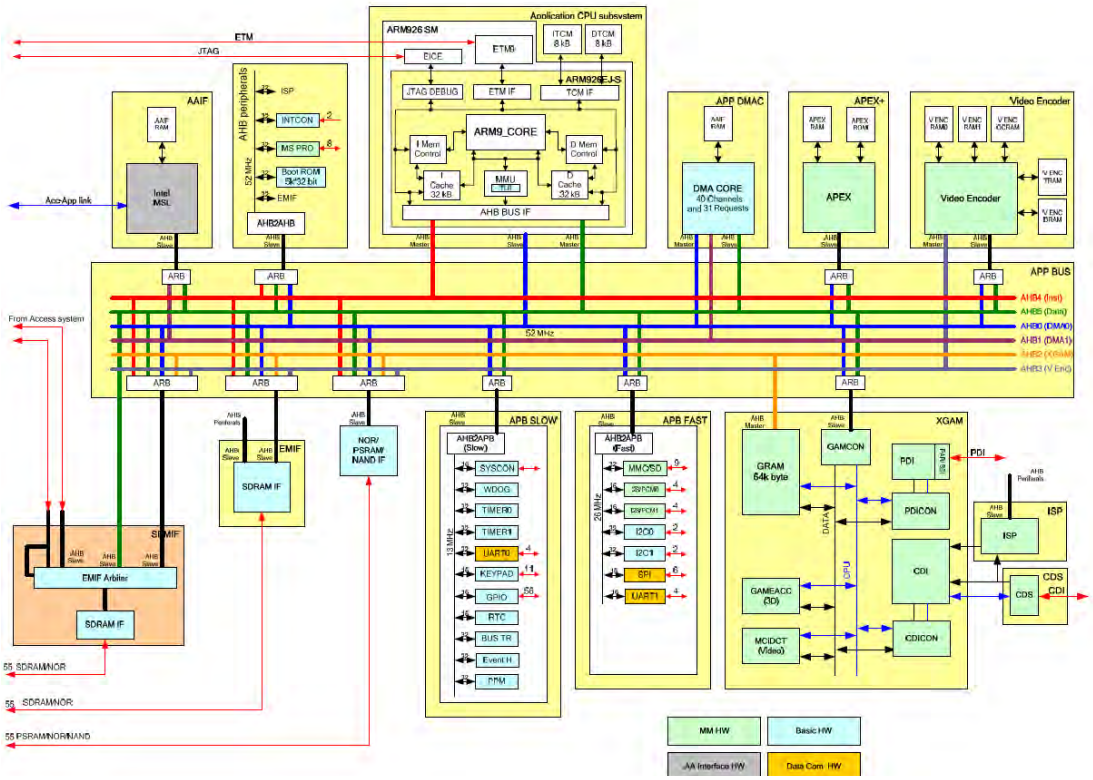
  The AHB peripheral subsystem contains a set of blocks with AHB interface that does not require high speed access. The blocks are:

  1. Boot ROM

2. USB
3. Interrupt controller from ARM CPU

- Fast ARM peripheral bus
  1. SPI
  2. I2S/PCM
  3. GPRS, Crypto
  4. UARTs
  5. IrDA
  6. I2C
  7. W-CDMA Ciphering
  8. W-CDMA Integrity
- Slow ARM peripheral bus
  1. Watchdog
  2. Event history
  3. Bus tracer
  4. Security functions
  5. Timer
  6. System connector
  7. General Purpose I/O
  8. Cable detect

3.2 Application subsystem



The Application subsystem contains functionality related to functions such as MMI, graphics, audio and memory media. The control CPU is an ARM with three external memory interfaces; one shared with the Access subsystem and two dedicated for the Application subsystem.

The Application subsystem contains several blocks. The main communication between the blocks is done through the Advanced High performance bus (AHB) matrix, which is a set of control busses connecting different parts.

A block called Syscon is responsible for distributing clocks and resets to all parts of the Application subsystem. This block is under SW control.

The Application subsystem is connected to the Shared EMIF that is used for code execution or data storage. In addition there are dedicated EMIF and a Flash IF.

The Application EMIF is a general interface for communication with for example SDRAM, PSRAM, NOR flash, NAND flash and companion chips.

The Application subsystem contains among others the following blocks:

- CPU

  The CPU block in the Application subsystem is an ARM with 32 kB instruction cache, 32 kB data cache and an MMU running at maximum 208 MHz.

- XGAM

The eXtended Graphics Accelerator Module (XGAM) is a graphics accelerator block used for several graphics related tasks. These tasks include display control, camera data processing, 2D and 3D graphics, JPEG encoding, H.264 & MPEG4 video decoding. XGAM is controlled and set up by SW, and has a built-in AHB master and cache functionality for efficient transfer to and from external memory.

- APEX

  The Audio Processing Execution (APEX) is used to create MIDI tones from wave tables and perform audio re-sampling.

- Video encoder

  The Video Encoder provides HW acceleration for H.264 video encoding.

- Application DMAC

  The Application DMAC is a DMA controller used to transfer data between different blocks within the Application subsystem.

- AAIF

  The Access-Application interface (AAIF) is used for communication between the CPUs in the Access and Application subsystems and for data transfers between them.

- AHB bus matrix

  The AHB bus matrix is a set of AHB busses connected to AHB masters and slaves in the Application subsystem. Each AHB master has ownership of one AHB bus and these are in priority order:

  1. CPU instruction
  2. CPU data
  3. XGAM
  4. Video Encoder
  5. DMA
  6. DMA AAIF

- AHB peripheral

  The AHB peripheral subsystem contains a set of blocks with AHB interface that does not require high speed access. The blocks are:

  1. Boot ROM
  2. Interrupt controller from ARM CPU

- Fast ARM peripheral bus

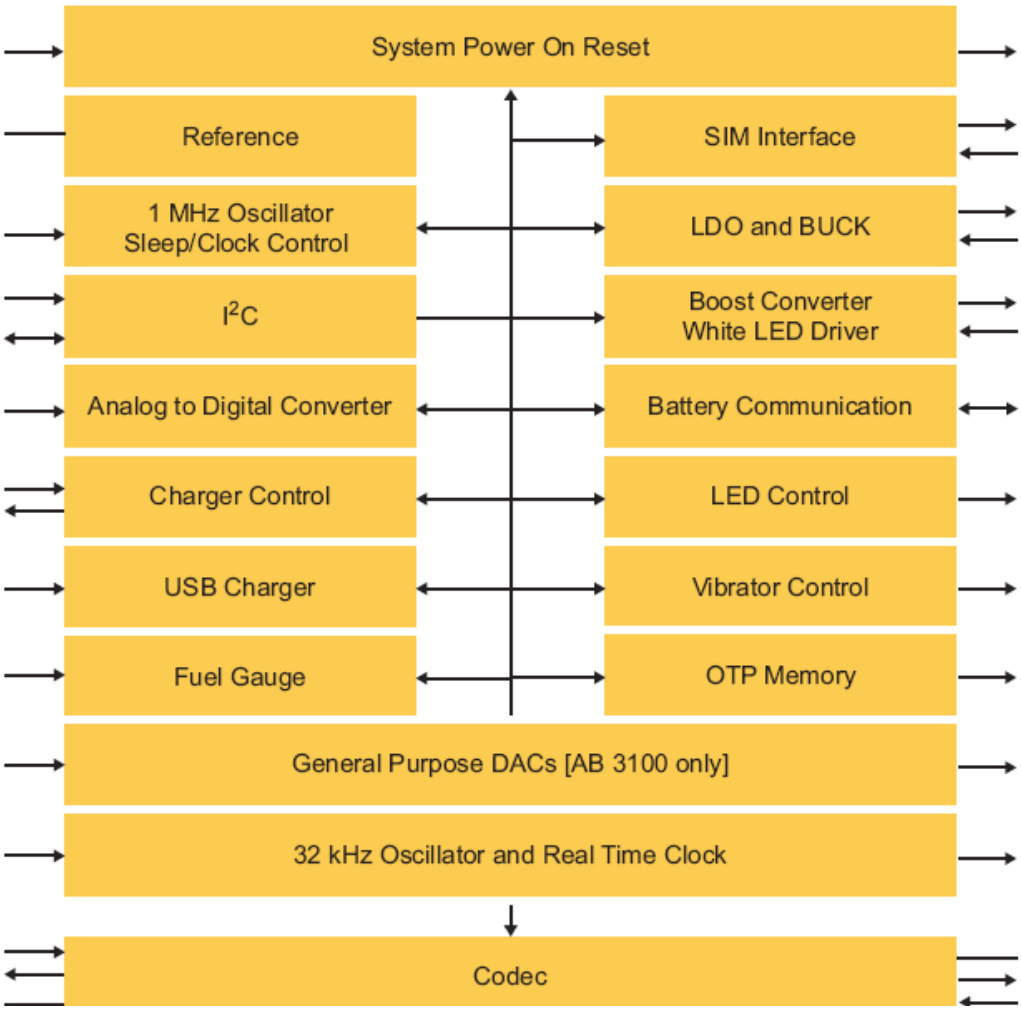
  1. MMC/SD

2. I2S/PCM
3. SPI

- Slow ARM peripheral bus
  1. Syscon
  2. Watchdog
  3. Timer
  4. UART
  5. Keypad
  6. GPIO
  7. RTC
  8. Bus tracer

4 Analog Baseband Control

The analog baseband controller is the main power management circuit equipped with a number of converters and regulators generating the required supply voltages. It is controlled through an I^2C interface and a three-wire bus.



The analog baseband controller has the following features:

- Supports Lithium battery
- Full audio CODEC functionality
- Supports stereo audio sampling rates of 8/16 kHz voice coding/encoding and 8/16/44, 1/48 kHz for high quality audio recording/playback (eg. MIDI and MP3).
- Microphone interface
- Earpiece interface
- Speaker interface
- Audio mixing functionality
- Boost driver for driving LEDs
- USB charging
- OTP with build-in change pump.
- Fuel gauge to monitor battery capacity

- 32 kHz real time clock with wake up capability

4.1 System Power on Reset

When power is applied to the analog baseband controller the interrupt functionality, low power regulator, DCIO detector and boot strapping logic in the power on reset block are powered on and active.

The system can be started by three events:

- A charger is connected
- A power switch is activated
- An alarm occurs

4.2 Reference

The reference block uses de-coupling capacitors and resistors.

4.3 SIM interface

The SIM interface supplies level shifting between digital baseband controller and a SIM card.

4.4 1 MHz oscillator, Sleep/Clock control

The internal 1 MHz oscillator is used as a clocking device that is activated or deactivated when needed by internal blocks to complete a task. If an external 26 MHz clock signal is present the oscillator locks onto that.

For the LDO regulators and BUCK converter there is an additional low power mode referred to as *sleep mode*. When this mode is selected the LDO regulators and BUCK converter enter low power consumption state or are switched off depending on the setting in the I^2C registers.

4.5 LDO and BUCK

The LDO regulators and the BUCK converter generate a range of programmable voltages. When the analog baseband controller boots up or down, internal signals activate or deactivate the LDO regulators and the BUCK converter. In active mode the LDO regulators and BUCK converter are activated and deactivated through I^2C.

The low power regulator is on all the time. It provides power for the 32 kHz oscillator and the real-time clock (RTC).

4.6 I^2C

The digital baseband controller uses the serial control block to change modes and parameters in the analog baseband controller. The I^2C bus is also used to read various registers eg. ADC and chip ID.

4.7 Boost Converter LED Driver

The analog baseband controller incorporates a boost converter for driving LEDs.

4.8 Analog to Digital Converter

The general purpose ADC consists of a 14-input multiplexer and an 8-bit ADC. The analog signal is selected with the multiplexer and converted in the ADC. The digital output data is stored in a register in the I^2C block.

4.9 Battery Communication

The analog baseband controller supports the following battery communication:

- UART communication
- Capacitance identification
- Resistance identification and temperature measurement
- Battery removal detection

4.10 Charger Control

The charger supports:

- Constant current charging
- Constant voltage charging
- Trickle charging
- Pulse width modulation controlled charging
- Over-voltage and over-current protection
- Watchdog termination
- DCIO assertion and removal detection
- Voltage and current measure functions

4.11 LED control

The LED control block controls six ports.

It is controlled through the I^2C bus.

4.12 USB Charger

The USB charger is compliant with the USB specification.

4.13 Vibrator Control

The vibrator motor driver is an LDO voltage source that regulates the voltage down to a level suitable for the vibrator.

4.14 Fuel Gauge

The analog baseband controller supports measurement of current consumption/charging current with a fuel gauge block. By constantly integrating the current flowing in and out of the battery the fuel gauge block determines the remaining battery capacity.

4.15 One Time Programmable Memory (OTP)

The OTP consists of an E^2PROM memory that can be written to using I^2C. Writing to the OTP can continue until the OTP lock bit is asserted and programmed into the E^2PROM. After this the OTP cannot be programmed or erased.

4.16 Real Time Clock (RTC)

A 32.768 kHz crystal oscillator provides a low frequency clock as long as the main battery is connected. This clock is used to keep the Real Time Clock (RTC) block functioning, so that the platform can keep track of time and date.

There is also an alarm register available. When RTC counter register value corresponds to the value set in the alarm register and alarm is triggered. The alarm will pull an internal ON switch that can start up the platform if it is powered down.

4.17 Codec

The codec encodes analog audio signals and analog voice signals into digital signals using A/D converters. The codec also decodes digital audio signals and digital voice signals into analog signals using D/A converters.

Both the audio codec and the voice codec are a 16 bit linear pulse code modulation (PCM) codec's.

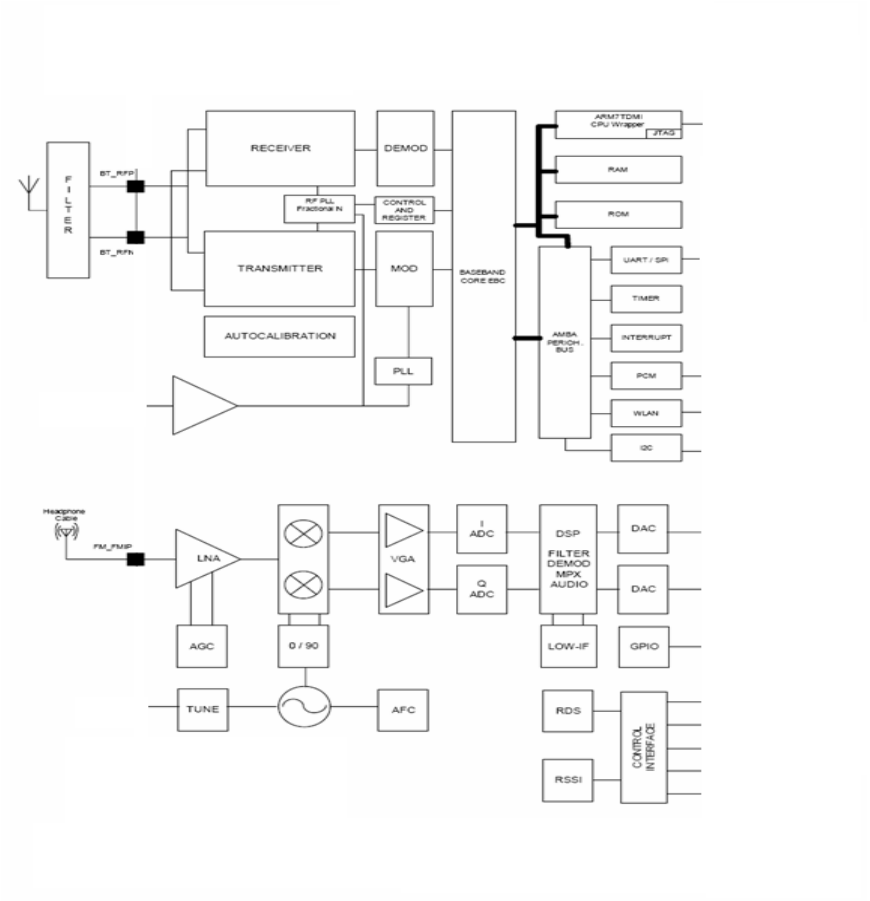
The codec encoder paths accept analog audio or analog voice input signals either from microphone sources or from auxiliary audio signal sources. The encoder paths generate PCM output bit streams and I^2S output bit streams.

There are also voice and audio decoder paths which works simultaneously and independently from the voice and audio encoders for duplex operation. The decoder section accepts PCM and I^2S digital input signals and regenerates analog audio and analog voice output signals though decoder paths which are sent to the output amplifiers.

Sampling rates: 8kHz, 16kHz, 44.1kHz and 48kHz.

5 Bluetooth

The Bluetooth implementation is compliant with Bluetooth version 2.1 + EDR.



5.1.1 RF part

The Bluetooth™ transceiver has frequency channels with 1 MHz separation from 2402 to 2480 MHz. The same band is used for both transmission and reception. This gives 79 frequency channels.

5.1.2 Frequency generation

The Bluetooth™ transceiver uses the 26 MHz system clock as reference clock to the synthesizer. One synthesizer is used for both RX and TX. To separate the receiver from the transmitter an integrated antenna switch is used.

5.1.3 Receiver

The first stage of the receiver is an external antenna filter, which suppresses unwanted frequencies. The receiver is of a “near-zero” IF receiver architecture. The local oscillator is generated by a frequency synthesizer, which allows the receiver to be set at frequencies in intervals of 1 MHz. The synthesizer is controlled from the logic part.

The received signal is sampled in the logic for later signal processing.

5.1.4 Transmitter

The synthesizer generates the TX frequency which modulated by the BT baseband block. It is then amplified. The BT system is a class 1 device with maximum of +5 dBm output power (minimum setting is about -50 dBm).

5.1.5 Baseband

The purpose of the logic part is to control and monitor the transmission and reception functions of the Bluetooth™ transceiver in the mobile phone. The logic therefore has links with all the relevant parts of the radio. Its functions, with reference to the radio, include selection of radio channel and control of radio timing. It also generates the data to be sent over the link after burst building and channel coding. The logic/audio part also demodulates the received base-band signal including channel decoding.

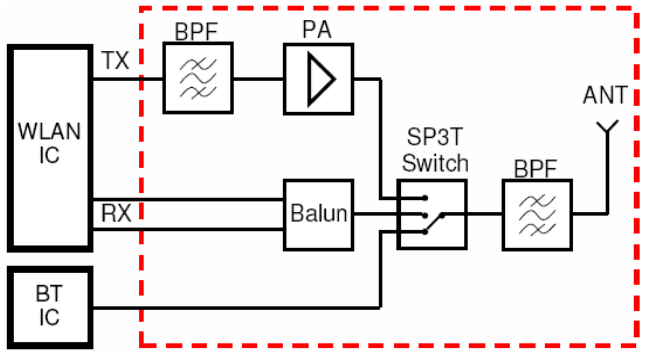
Its functions, with reference to the audio parts, include a PCM interface.

6 Wi-Fi (Type Number:**AAD-3880067-BV** haven't this function)

A dedicated WiFi component is used in the phone.

The WiFi IC implements all functionality needed for 802.11b/g and is used together with a front end module (FEM) that includes the needed RF components (PA, antenna filtering, balun, antenna switch).

The WiFi antenna is shared between Bluetooth and WiFi according to the figure below. The items in the red box except the antenna are included in the FEM.

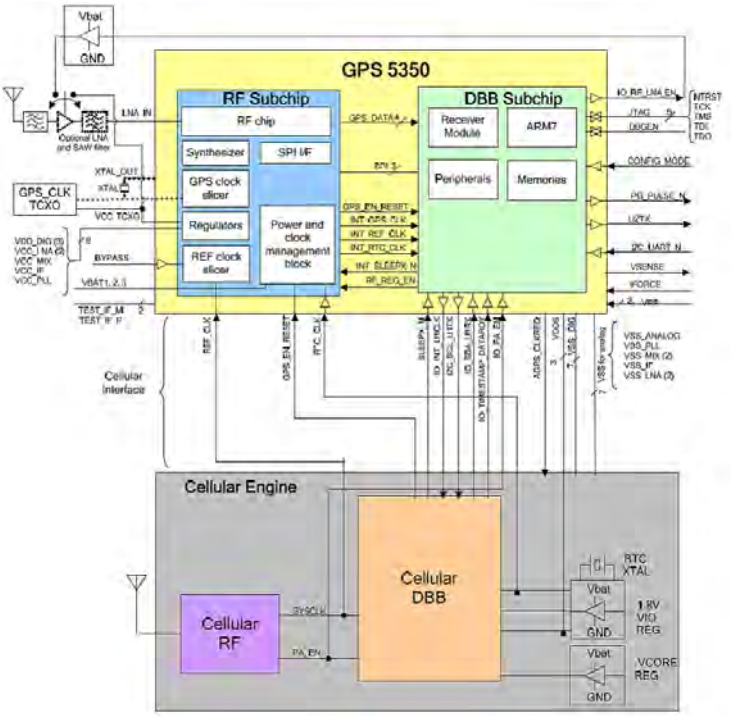


WiFi FEM connected to Bluetooth and WiFi ASICs.

Three signals are connected between Bluetooth and WiFi in order to allow coexistence via time division (PTA) since they use the same frequency band 2.402 – 2.480 GHz. The signals indicate activity on each side, and the application will set priority for WiFi data or Bluetooth data/audio depending on the use case.

WiFi is connected to the access SPI bus. This bus has maximum 13 MHz clock speed, which will result in a throughput around 5-10 Mbps even though the physical rate over the air is up to 54Mbps.

7 A-GPS (Type Number:**AAD-3880067-BV** haven't this function)



The unit has a built-in GPS antenna and receiver placed in the upper half, right side on the main board. It has equal performance when the handset is in its open or closed position.

The solution uses a stand alone GPS chip with a dedicated crystal oscillator running at 16.368 MHz. The GPS chip is connected to the main CPU via UART.

The user can select to obtain positioning either stand-alone (using the GPS receiver only) or together with assistance data from the cellular network/lookup service (using A-GPS).

Emergency locationing always uses available assistance data together with GPS to secure the fastest possible response time and accurate positioning.

8 FM radio

The FM radio receiver is a stereo radio able to decode RDS information.

8.1.1 RF part

The FM radio can tune to the US/European broadcast FM frequency band, 87.5 – 108 MHz

8.1.2 Frequency generation

The FM radio receiver uses a 32.768 kHz reference clock to tune the local oscillator.

8.1.3 Receiver

The RF signal to the FM radio is first fed into a low noise amplifier. The amplified signal is then mixed with the local oscillator. The IF is of low frequency-type.

The signal is then further amplified, limited and demodulated. The demodulated signal is fed into a decoding circuitry where the right and left audio signals and RDS information are separated.

8.1.4 Baseband

The logic part of the FM radio controls the frequency tuning system, and various settings within the FM radio system. It also handles the communication, including transfer of RDS data, with the CPU of the mobile phone. The communication with the CPU is over a two-wire I^2C interface.

8.1.5 Antenna

The cord to the portable hands-free headset functions as the antenna for the FM radio.

9 Audio DSP FM31

Fortemedia's FM31-331, an innovative wideband digital voice processor, is a choice for portable applications such as mobile phone, PDAs, handhelds and automotives. Fortemedia's SAM™ (Small Array Microphone) technology in FM31-390 supersedes conventional array microphone design for it utilizes 2 microphones based voice processing.

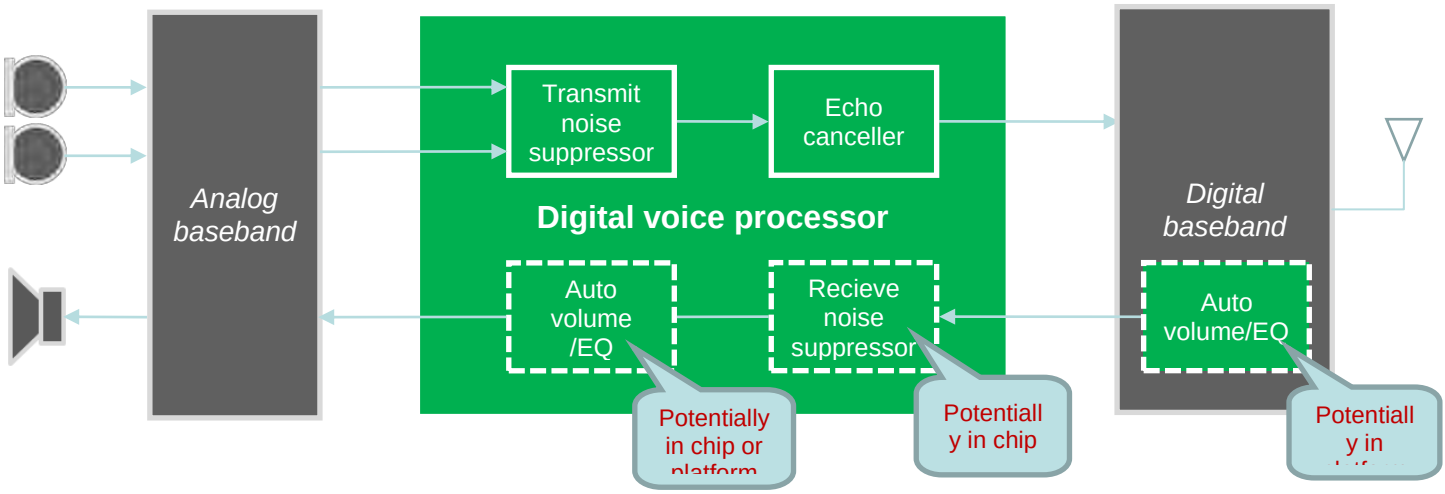
9.1.1 Frequency Generation

The FM 31 uses a 26 MHz reference clock .

9.1.2 Baseband

FM31-331 has the ability of communication to the host system either through I²S (Inter-IC Sound) or PCM (Pulse Code Modulation) interfaces. The microphone input is captured through digital microphone interface and passed through digital voice processing and outputs the processed data to the host system. This voice processor includes a high performance and low power DSP (Digital Signal Processor) that comes with a hardware accelerator, an internal ROM and a RAM. The new BrightVoice™ signal processing technology enhances the playback intelligibility by monitoring the ambient noise and enhancing the speaker output.

9.1.3 Block



10 Peripherals

The digital baseband controller includes support for data communication, MMI, basic services and operation services.

The functional blocks of the peripherals subsystem connect to either the Fast ARM peripheral bus (BT, USB, memory cards display, camera) or the Slow ARM peripheral bus (keypad).

10.1 Data communication

Data communication HW provides support for data communication with external equipment such as accessories and PCs.

The external USB transceiver supports full speed USB (12Mb/s) and high speed (480Mb/s) and is compliant to the USB 2.0 standard. Transfer rate for USB HS is in practice around 25 Mbps because of the protocol overhead and file system.

Bluetooth 2.0 including Enhanced data Rate (EDR) with up to 1.8 Mbps is supported, as well as RS232.

10.2 Man-Machine interface

The MMI HW provides the physical interface between the user and the system. The HW associated with the MMI allows the user to navigate though menus enter information via keyboard /some functionality can also be controlled from a touch MMI) and activate other dedicated keys.

- Vibrator is supported.
- Parallel and serial display data interface are supported.
- Camera interface with view finding.
- Audio generation: DTMF, MIDI

- Keypad illumination.
- Display backlight.

10.3 Basic Services

The Basic Services handles the SIM cards, memory cards, General Purpose I/O, and serial control of circuits.

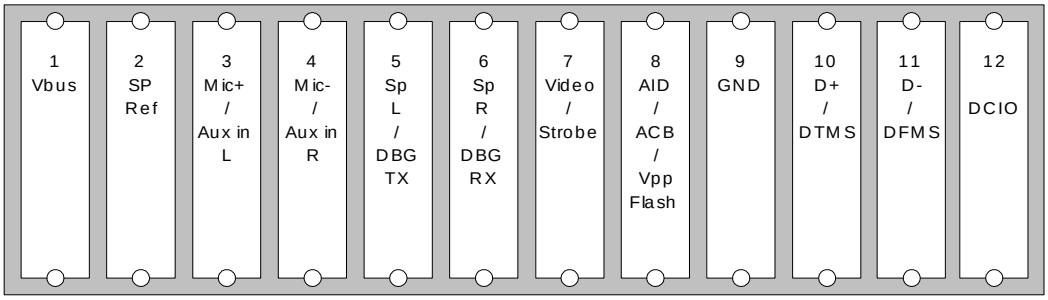
10.4 Operation Services

The battery interface is used for handling and changing Lithium batteries.

The cryptography engine handles security algorithms such as ciphering and authentication of application data and streaming data. The security algorithms are used by applications for internet browsing and online banding and when playing DRM protected music.

10.5 System connector

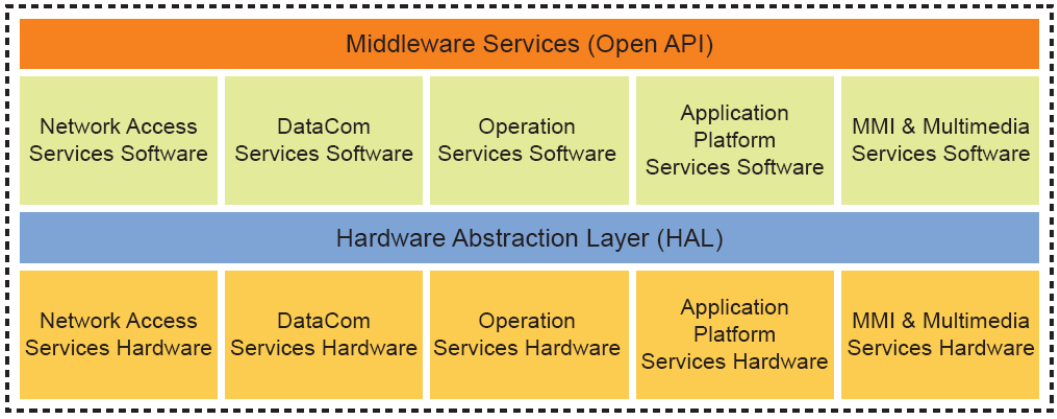
External units are connected to the transceiver by means of a 12-pin connector on the bottom of the phone. The pin numbering is starting from the right when looking at the system connector with the front up.



11 Software

11.1 SW Architecture

The system SW architecture is a layered design divided into 5 stacks.



Data flows horizontally between service stacks to provide efficient data transport without moving time critical parts up to middleware or applications.

11.2 Network Access Stack

The Network Access Stack provides radio bearer services for data communication (eg. streaming, messaging, internet browsing, e-commerce).

Network Access Stack also provides bearer services for voice communication both as stand-alone and in parallel with data communication services.

The Network Access Stack consists of:

- Network signalling stack
- Audio control
- Audio processing for circuit-switched radio
- Positioning measurements for A-GPS

Fundamental control of the physical layers together with audio signal processing and tasks such as channel encoding/decoding, channel estimation, equalization and interleaving/deinterleaving are executed in the DSP. Higher layers of the Network signalling stack are executed in the Access CPU.

11.2.1 Network signalling stack

The Network signalling stack consists of:

- Common Access SW (CAS): Handles non-access stratum of UMTS/3GPP standard. CAS handles functionality that is common to different technologies and standards.
- W-CDMA Access SW (WAS): Handles L3 RRC and L2 of W-CDMA access stratum of 3GPP standard. User interfaces provided by PHY to communicated with W-CDMA L1.
- GSM Access SW (GAS): Handles layer L1, L2 and L3 of the GSM access stratus of 3GPP standard.

11.2.2 Audio Control

The audio control handles the audio paths on the access side. The application side has the overall control of the audio in the platform. The digital audio in the form of PCM samples can either be transported over the Interface service or over a simple PCM interface that is located in the Network Access Services.

11.2.3 Audio Processing

The audio processing is performed in a DSP controlled by the Access CPU and FM31 external DSP. They provides the following functionality:

- Speech trans-coders
- Echo cancellation

- Noise reduction
- GSM band pass filter
- Acoustic compensation
- Soft limiter
- FM31 DSP is a external DSP for the Noise reduction .

11.2.4 DSP SW

In addition to audio functionality the DSP controlled by Access CPU provides functions for GSM/EDGE/GPRS and W-CDMA:

GSM/EDGE/GPRS

- Equalizer for Gaussian Minimum Shift Keying (GMSK) modulation and 8 position Phase Sift Keying (8-PSK) modulation.
- Channel decoding/encoding
- Interleaving and normalization
- Single Antenna Interference Cancellation (SAIC)
- Crypto – GSM

W-CDMA

- Frame structure of Transport channels
- Physical channel management
- Channel estimation
- Fast loop power control

Misc.

- Tone generation
- Volume control for circuit switched radio
- TTY – Cellular telephone test modem functionality

11.3 DataCom Stack

The DataCom Stack provides the following services:

- Socket interface: Using either UMTS,Bluetooth or W-Lan the socket interface allows applications to communicate with services connected through the UDP or TCP.
- Dial-Up networking: Using Bluetooth, RS232 or USB interfaces the DataCom Stack enables DUN from an e.g. a laptop or PDA.

- Network Access Point (NAP): As an alternative to the dial-up networking approach the DataCom Stack enables a bridging functionality between an incoming network connection (the local area network where the PC/PDA is connected) and an outgoing network connection (the wide area network reached through the UMTS services). For incoming connection both USB and Bluetooth are supported. For outgoing connection both UMTS CS and UMTS PS are supported.

11.4 Basic Services Stack

The Basic Services Stack supports the following functionality:

- System control: Handles power up and power down. Handles lock control of SIM and phone lock.
- SIM/USIM management: Handles access to ICC/UICC including SAT.
- Access power management: Handles the system power, battery functionality, and current save by controlling the Enabling/disabling and clocks to the HW blocks in the system.

  The power management of the Access and Application subsystems is handled separately. The Application subsystem has the main power management responsibility, but after power up and boot the Access subsystem is responsible for enabling and disabling of its clocks.

  The power management system will set the Access subsystem in sleep mode when the CPU has stopped al activity and there are no other blocks (UART, USB, AAIF and timer) that are enabled.

  The timer can be used to wake up the CPU. In this case the timer is clocked by the 32 kHz RTC.
- Security: Basic functionality for standard algorithms for encryption, hashing and digital signing.
- Core Platform Security (COPS): Framework to meet the GSMA/EICTA, 3GPP and US FCC Part22 requirements on IMEI protection and personalization in mobile equipment. This includes:
  - Reprogramming protection
  - IMEI protection
  - SIM lock protection
  - Phone lock protection
  - DRM keys

11.5 Interface Services Stack

The Interface Services Stack carries all the traffic, data and control, between the access and application sides, including digital audio to and from access side. The physical data link between the two CPU's allows full duplex operation.

11.6 Operation Services

The Operation Services Stack provides the Real-time operating system (OSE) and all basic functionality for the Application subsystem.

- System control: Responsibility for coordinating the activation, execution and deactivation of the application side core functionality.
- Persistent storage: Provide storage of data on any storage media that is accessible through the file system (e.g. internal memory, non-removable flash media, and removable flash such as uSD card).
- Application power management: Controls the clocks to the various HW blocks in the system in order to turn off as many blocks as possible when not used.

  The Application subsystem has the main power management control and turns on the Access subsystem after power up and boot. Hereafter each subsystem is responsible for its own power management.

  The Application subsystem uses the RTC in both active and sleep mode.
- Battery management: Divided in to two separate functionality blocks:
  - Battery charging: Two modes of charging are supported: *Slow mode* which works for most batteries, charges with low current and stops when a safe voltage level is reached; *Time optimized mode* which is tailored to the battery type.
  - Capacity reporting: Fuel gauging functionality used to estimate the remaining battery capacity.
- XML toolkit: Provides parsing and encoding of XML documents both for platform internal and external usage.
- Security: Services similar to the ones for Access subsystem.
- COPS: Services similar to the ones for Access subsystem.

11.7 Application Platform Stack

The Application Platform Stack provides server functionality to the customized applications through the OPA interface. The services are:

- Phone book server
- Accessory server
- Positioning application server
- Clock server
- Messaging transport server
- Cell broadcast server

11.8 Multimedia Protocol Stack

The Multimedia Protocol Stack provides includes multimedia protocols, HTTP, OBEX, Bluetooth. The DataCom Stack on the Access subsystem handles layers below IP.

11.9 MMI & Multimedia Stack

The MMI & Multimedia Stack supports the user interface and multimedia by providing a window system and access to codec's, graphics, video and camera services. Also

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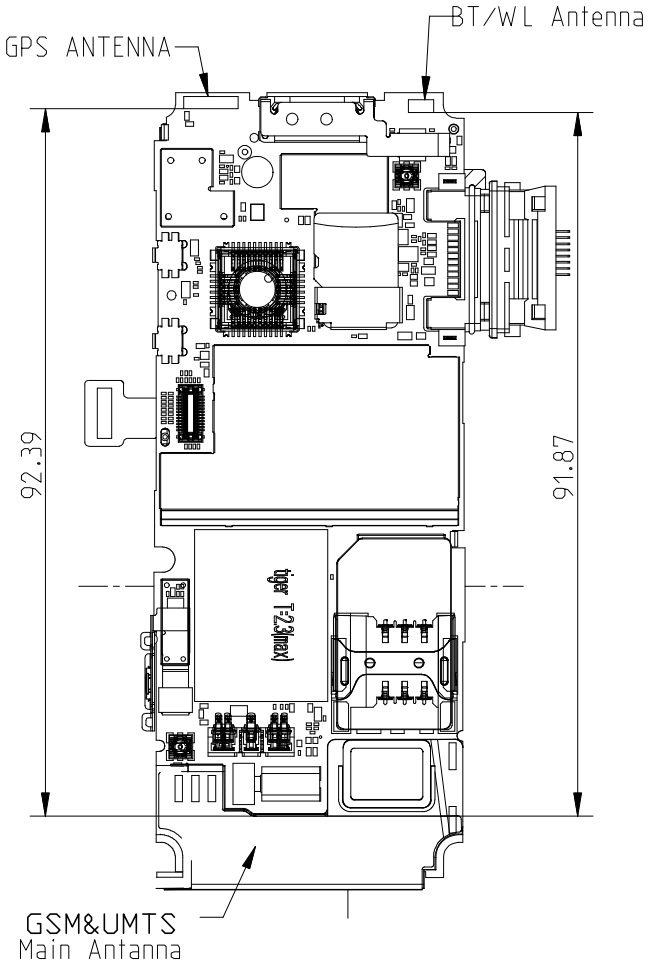

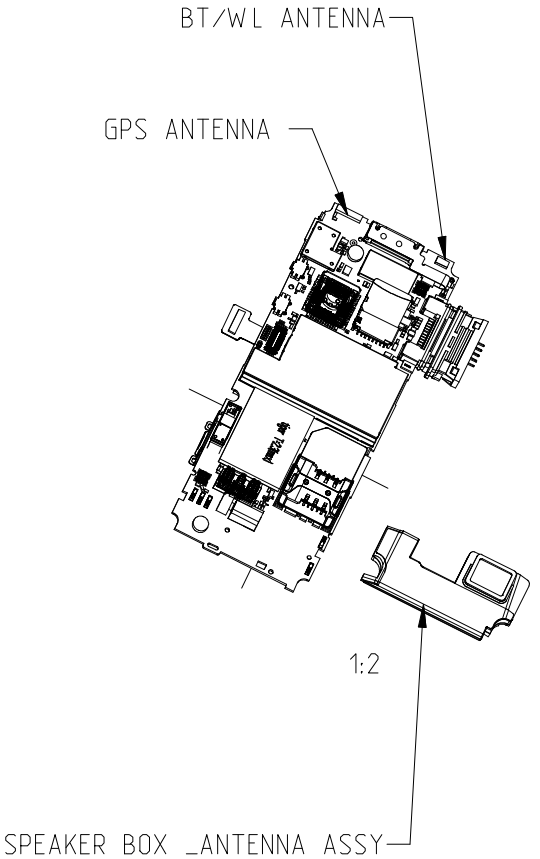

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Sony Ericsson

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Drawing Rules ISO

Tolerance

Doc Responsible/Approved
DUB

Date
2009-11-05

Rev

Product Name
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Reference

Document No.

Project Name

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