THEORY OF OPERATION

(MODEL: IFG-400)

1. FREQUENCY GENERATION

The frequency generation circuit is composed of the synthesizer IC 101 and the VCO. The block diagram illustrates the interconnect and support circuitry used in the design. Refer to the schematic for reference designator.

The supply for the synthesizer is regulated 4.2 volts which also serves the rest of the radio. In addition to the VCO, The synthesizer must interface with the logic and AF filter circuitry. Programming for the synthesizer is accomplished through the clock, data and strobe signals (pin 38, 39 and 40) from the microprocessor IC602.

A serial data is sent whenever the synthesizer is programmed. While unlock is indicated by a low voltage on this pin. The audio signal from the AF filter is modulated by D101 of VCO.

PLL FREQUENCY SYNTHESIZER

The IC101(PLL IC) includes all the functions such as the phase comparator, the programmable divider, the lock detector, and reference oscillator.

The synthesizer uses a 21.25 MHz crystal (X100) to provide the reference frequency for the system.

The loop filter, composed of R102, R111, C112, C115, C116, provides the necessary DC steering voltage for the VCO as well as filtering of spurious signals from the phase detector. The pre-scaler for the PLL is internal to IC101 with the value determined by the frequency band of operation.

The 21.25 MHz crystal (X100) is the temperature compensation circuit to maintain the frequency within the allowable error range even on -30℃.

V C O

The VCO, in conjunction with the synthesizer (IC101), oscillates 462.5125 MHz to 462.7125 MHz in the transmit mode and 440.8625 MHz to 441.0125 MHz in the receive mode. The VCO consists of the colpitts oscillator of the Q102. A sample of the RF signal from the enabled oscillator is routed from C114, through to the pre-scaler input (IC101 pin 1). After frequency comparison in the synthesizer, a resultant control voltage is received at the VCO. This voltage is a DC voltage between 1.0 and 4.5 volts when the PLL is locked on frequency.

In the receive mode, the RF signal through Q103 is the local oscillator RF injection and it is applied to the first mixer at Q202.

In the transmit mode, the RF signal at Q302 is run to the input of the pre-drive transistor (Q303 base). This RF signal is the Tx RF injection. Also in transmit mode, The audio signal to be frequency modulated onto the carrier is received by the transmit VCO modulation circuitry at audio in.

During reception, a relative low frequency should be oscillate compared to transmission. Therefor, the D402 is adversely biased by the Q401, and as a result, the C415-416 which is added in serial to the resonance circuit of the VCO is removed to oscillate the desired reception frequency.

2. RECEIVER

The receiver of the UHF consists of 4 major blocks each: the Front-end ,the Mixer , the First IF and the Second IF / Demodulator IC.

FRONT - END

The UHF Front-end contains two separate circuits : the RF Amplifier and SAW Filter. The RF Amplifier, consist of transistor Q201 This Amplifier has approximately 20dB gain owing to high output impedance , a noise figure of approximately 3dB and is supplied by the receive 4.0V line.

The SAW Filter is BPF of high stability and reliability with good performance and is fixed-tuned design to eliminate the need for tuning and to provide narrow-band operation. The 3dB bandwidth is approximately 6MHz, centered on 462MHz with an insertion loss of approximately 2dB.

The net-gain from the Front-end selection is approximately 20dB in the center of the band, falling to approximately 4dB at band edges, with a center band noise figure of approximately 5.5dB.

MIXER

The Mixer operates with a local oscillator drive level minimum -4dBm. The mixer provides excellent isolation between the ports and operates over a large bandwidth. The received signal is mixed down to 21.7MHz, the frequency of the first IF.

FIRST IF

The first IF consists of a 21.7MHz crystal filter and amplifier. The crystal filter provides second image protection and inter-modulation protection with approximately 3.75kHz bandwidth(3dB) for 12.5kHz models. The IF Amplifier, Q203, provides approximately 10dB of gain at 21.7MHz.

SECOND IF/DEMODULATOR IC

The Second IF/Demodulator IC(DBL5018-V; IC201) accepts the 21.7MHz IF input and mixes it with a second local oscillator signal(21.25MHz). This produces a second IF of 450kHz, which is filtered externally by a ceramic filter and passed back into the IC for amplification.

The signal is passed to a quadrature detector for demodulation and, after being filtered, is passed to the output. The IC, along with some external components, controls the squelch sensitivity, squelch tail, and hysteresis. Internal variable resistor, VR11, controls the noise squelch setting.

Ⅲ. TRANSMITTER

The IFG-400 transceiver is composed of five basic circuits : a Pre-Driver, Driver, Final Amplifier, Antenna Switch and a Harmonic Filter. Refer to the block diagram and the schematic for more information.

POWER AMPLIFIER

The Power Amplifier consists of three stages : a Pre-Diver, Driver, Power Amplifier. It requires a supply voltage of 6 volts, and is capable of supplying maximum 2.0W(ERP).

ANTENNA SWITCH

The antenna switch circuit consists of two pin diodes (D301 and D302),In the transmit mode, Tx B+ is applied to the circuit to bias the diodes "on". The shunt diode (D301) shorts out the receiver port and the PI network, which operates as a quarter wave transmission line and transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter.

In the receive mode, The diodes are both off, hence, there exists a low attenuation path between the antenna and receiver ports.

HARMONIC FILTER

The harmonic filter consists of part of L308, L309, C310, C321, C322, C323. The design of the harmonic filter is 5th order chevyshev filter with 0.5dB ripple. This type filter has the advantage that it can give greater attenuation in the stop-band for a given ripple level.

Ⅳ. AUDIO PATHS

RX AUDIO PATH

After de-emphasis and volume adjustment VR401, it is fed to the Audio Power Amplifier, IC603. This is a Bridged-tied Load amplifier with a fixed gain of 40dB, developing 300mW output at less than 5% harmonic distortion into the 4Ω internal loudspeaker with nominal 6V battery and supply. Maximum audio power output is greater than 1W.