TERMINAL CIRCUIT DESCRIPTION

MODEL : WS-4100

- CONTENTS -

1. General

It is a WLL(Wireless Local Loop) phone using CDMA. Exactly it is a fixed WLL Phone. There are two types in WLL Phone. One is phone type and the other is terminal type. Phone type is integrated type so it does not require another telephone. Terminal type is not integrated type so it require standard telephone or compatible equipment.

2. Standards

2.1 Air interface standard : J-STD-008, IS-95B, IS-95C

2.2 Vocoder : IS-96A,IS 127,IS-733

2.3 Data Service :IS-99

2.4 RF specification : IS-98C

2.5 SPECIFICATIONS

2.5.1 Power SPECIFICATION

2.5.2 POWER SUPPLY

1) INPUT : 90 400 VAC, 47 63 Hz

2) OUTPUT : DC 12V, 1.0A

2.5.3 BACK-UP BATTERY

1) TYPE : Ni-MH

2) CAPABILITY : 6V 2500mAh

2.5.4 POWER CONSUMPTION

1) NORMAL(Stand-by) : 75mA

2) TALK : 500mA @ SVC OPT2 ,SECTOR POWER ? 92.5dBm ,HALF RATE

2.6 GENERAL SPECIFICATION

I T E M	SPECIFICATION
Air Interface	J-STD-008,IS-95B,IS-95C
Channel access method	DS-CDMA
MOD/DEMOD	OQPSK/QPSK
VOCODER	8KQCEPL,13KQCELP,8KEVRC

Max Data transmission	86.4Kbps(IS-95B), 153.6Kbps(IS 95C)
Battery backup time	Talk time : Up to 3 hours Standby time : Up to 20 hours
Operating Temperature	0 50
Operating Humidity	5% 95%

2.7 RF SPECIFICATION (IS-98C)

I T E M	SPECIFICATION
Freq. Range	Tx : 1850 - 1910 MHz , Rx : 1930 ? 1990 MHz
Bandwidth	1.25MHz
TX maximum output power	0.2W (23dBm) ~ 1W (30dBm)
TX minimum output power	-50dBm below
RX Sensitivity	-104dBm below (at FER = 0.5%)
Freq. Stability	Fo □150 Hz
Single tone Desensitization	-101dBm below (at FER = 1%)
Rx conducted spurious Emission	TX Band : -61dBm/1MHz below RX Band : -81dBm/1MHz below Out of Band : 47dBm/30kHz below.
Intermodulation spurious response attenuation	-101dBm below at CW1:Fc □1.25MHz,CW2:Fc □2.05MHz, 43dBm
Tx conducted spurious Emission @ Max Power	Spurious emission levels shall be less than 1) Greater than 1.25MHz ? 42dBc/30kHz or ? 54dBm/1.23MHz 2) Greater than 1.98MHz ? 50dBc/30kHz or ? 54dBm/1.23MHz 3) Greater than 2.25MHz
Open loop power control	-51dBm □9.5dB at system power -25dBm -11dBm □9.5dB at system power -65dBm

Time reference	Within □1
Waveform quality	0.944 above

Table 1 - CDMA Channel Number to CDMA Frequency Assignment

Transmitter	Channel Number	Channel Allocation (MHz)
Mobile Station	0≤N≤1199	0.05*N + 1850.000
Base Station	0≤N≤1199	0.05*N + 1930.000

Table 2 ? CDMA Channel Number and Corresponding Frequencies

Block Designator	CDMA Channel Validity	CDMA Channel Number	Transmit Frequency Band (MHz)	
			Mobile Station	Base Station
A (15 MHz)	Not Valid	0-24	1850.000-1851.200	1930.000-1931.200
	Valid	25-275	1851.250-1863.750	1931.250-1943.750
	Cond. Valid	276-299	1863.800-1864.950	1943.800-1944.950
D (5 MHz)	Cond. Valid	300-324	1865.000-1866.200	1945.000-1946.200
	Valid	325-375	1866.250-1868.750	1946.250-1948.750
	Cond. Valid	376-399	1868.800-1869.950	1948.800-1949.950
B (15 MHz)	Cond. Valid	400-424	1870.000-1871.200	1950.000-1951.200
	Valid	425-675	1871.250-1883.750	1951.250-1963.750
	Cond. Valid	676-699	1883.800-1884.950	1963.800-1964.950
E (5 MHz)	Cond. Valid	700-724	1885.000-1886.200	1965.000-1966.200
	Valid	725-775	1886.250-1888.750	1966.250-1968.750
	Cond. Valid	776-799	1888.800-1889.950	1968.800-1969.950
F (5 MHz)	Cond. Valid	800-824	1890.000-1891.200	1970.000-1971.200
	Valid	825-875	1891.250-1893.750	1971.250-1973.750
	Cond. Valid	876-899	1893.800-1894.950	1973.800-1974.950
C (15 MHz)	Cond. Valid	900-924	1895.000-1896.200	1975.000-1976.200
	Valid	925-1175	1896.250-1908.750	1976.250-1988.750
	Not Valid	1176-1199	1908.800-1909.950	1988.800-1989.950

Note : Total Channel : 1200

2.8 SUBSCRIBER INTERFACE SPECIFICATION

I T E M	SPECIFICATION
Line Voltage	-50 □6 V
Line Current	20 40mA
OFF-HK Threshold Current	5 9mA
Ring Driving	3.0 REN (1REN=6930 +8.0uF: US Standard)
Ring Voltage Ring Frequency	64 □3Vrms (25Hz, 1REN) Selectable 16/20/25 Hz
Normal Ring Cadence	Selectable -. 1sec On – 2sec Off . 0.4sec On – 0.2sec Off – 0.4sec On – 2sec Off -. 1sec On – 4.5sec Off -. 1sec On – 4sec Off -. 0.25sec On–0.25sec Off-0.25sec On –1.25sec Off -. 1sec On – 4sec Off
Dial Tone Frequency	Selectable -. 350 + 440Hz Dual Tone

Dial Tone Cadence	-. 400Hz single Tone -. 425Hz single Tone -. 450Hz single Tone Continuous
Warning Tone Frequency	Selectable . 350 + 440Hz Dual Tone -. 400Hz single Tone -. 425Hz single Tone -. 450Hz single Tone
Warning Tone Cadence	-. 0.2sec On – 0.2sec Off
Howler Tone Frequency	3950 Hz
Howler Tone Cadence	. 0.2sec On – 0.2sec Off
Hook Flash time	Selectable -. 100 ~ 200ms -. 100 ~ 500 ms . 100 ~ 700ms -. 100 ~ 1800ms
PCO Interface	Metering Pulse : **16KHz** / 12KHz □.5 % Tone Level : 540 □00 mVrms
Tel-line Impedance	600
CLIP	Bellcore : 500 mVrms □00 mVrms PB : 2.4 Vpp □Vpp

2.9 Dimension and Weight

1) Dimension : 190 x 170 x 55mm(DxWxH)

2) Weight : 750 g (Include Backup battery)

3. Configuration

3.1 Basic configuration

1) Terminal, Antenna(Di-pole)

2) SMPS(Switching Mode Power supply)

3) Back-up Battery

3.2 Optional accessory

1) External antenna kit : Panel antenna, RF cable

2) External Battery

3) Wall mounty bracket

3.3 Structure AND Function

3.3.1 LED

1) RSSI : Indicate receive status

- Color : GREEN-ORANGE-RED

2) BATTERY : Indicated when using the built-in back-up battery

Color : GREEN-ORANGE-RED

3) POWER : Indicate main power (external power) supply status

- Color : RED

3.3.2 SWITCH

1) POWER : Main Power ON/OFF

Type : SLIDE SWITCH

3.3.3 CONNECTOR

1) ANTENNA CONNECTOR : For connection to basic antenna or external antenna

- Type : TNC-RB

2) TERMINAL CONNECTOR : For connection to standard telephone or terminal for telephone communication

- Type : RJ-11(M623 Modular jack)

Quantity : 2 EA

3) POWER CONNECTOR : For connection to external main power (power supply unit)

- Type : JACK TYPE

4) SERIAL CONNECTOR : For program debugging, terminal data setting, Data SVC

- Type : DB9 with cover

3.4 PCB assembly type

1) Main PCB Assembly

2) G3 FAX PCB Assembly

3) RF PCB Assembly

4) LED PCB Assembly

4.Features

4.1 Installation

- Terminal : For desk top or wall mounting

  Power Supply unit

4.2 Connection

  Connection of standard telecommunication equipment

- Origination and termination of call, and call connection

4.3 Operation status indication

- RSSI: Indicate field strength received to the terminal
- BATTERY: Indicate the status of built-in back-up battery (battery charging and discharging)
- POWER: Indicate main power (external power) supply status

4.4 Operation in case of the stoppage of main power supply

- Operated by the back-up battery in case of the external power (main power) blocking

5.Logic Part Circuit Description

Logic part consists of power unit, digital unit, audio unit and SLIC & CALLER ID unit and DATA SVC & FAX unit.

5.1. Power unit

5.1.1 Adapter (SMPS)

AC power input is converted to a current to be used in the terminal. It converts 90V ~ 400V AC input to a 12V DC @ 1.0A output.

5.1.2 Battery charging and Power supply unit

This unit charges the back-up battery using the current supplied by the adapter in preparation to a power outage.

12V current charges the battery through D702,705,706,707and R708. The charging current is determined by R700,708,709.

When the power supply to the adapter is interrupted, Q705 is set off and Q701, Q704 are set on by U702 supplying the battery power to the circuit. Q704 is controlled by MSM and when the battery gets fully discharged

MSM sets Q704 off by using PS-HOLD port, and at this time, all power is cut off.

And this unit supplies power to each end using the 12V DC current supplied by the adapter.

VPOS,12VDS : 12V → SLIC IC main power and Fax board power

U001 ,RFU POWER,4V : 4V → RF MODULE main power , Led and Data service part power

U005 , 3.0D : 3.0V → Digital power for such as MSM, memory

5.2 Digital unit

The most important part of the digital unit consists of MSM5000 (Mobile Station Modem 5000) ASIC, flash ROM, SRAM, and EEPROM as shown in figure 1. MSM5000 is an ASIC chip set designed for baseband digital signal processing of CDMA terminal, and it needs the following 3 clocks to operate.

- CHIPX8 (9.8304MHz)
- TCXO (19.68MHz)
- XTAL_IN (27MHz)

CHIPX8 and TCXO are provided by RF unit, and XTAL_IN is oscillated using an external resonator. CHIPX8 is a clock mainly for CDMA signal processing. TCXO is for signal processing during sleep mode. XTAL_IN is a clock needed for the operation of the microprocessor integrated into MSM5000. From figure 1, MSM5000 features and characteristics can be summarized as follows.

General Features

- Voice mode 1 (EVRC, IS-96-A, PureVoice) all radio configurations
- High-speed data using both fundamental and supplemental channels
  - Supports peak rates of 153.6 kbps on forward or reverse link
- Quick Paging Channel
- 8x Searcher, plus an independently controlled 16x Searcher
  - Approximately three times the searching capabilities of the MSM3000
- Radio Link Protocol 3 (RLP3)
- Support for Fast Power Control (both forward and reverse links)
- P-Rev 6 compliant
- Voice Recognition (optional)
  - Speaker-dependent, Speaker-independent, and voice prompt support
  - Multiple languages supported
- Supports low-power, low-frequency crystal to enable TCXO shutoff

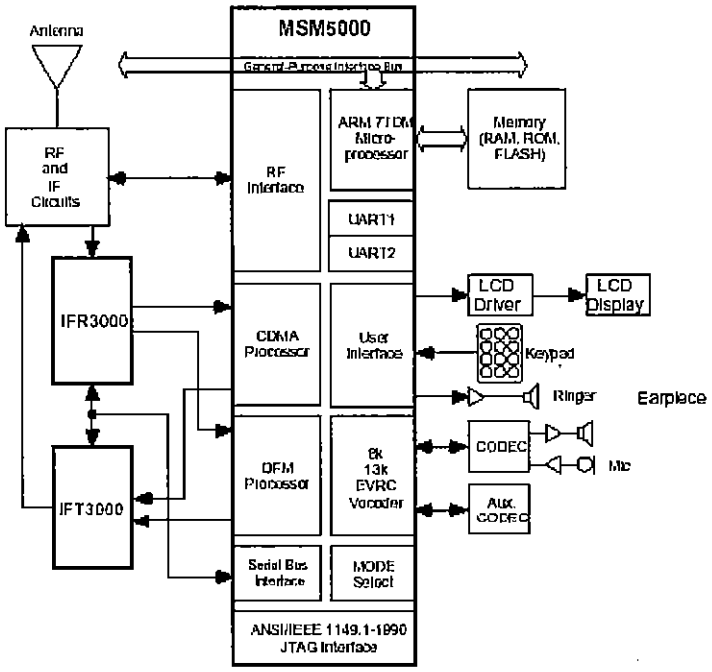
- Two packages available:
  - 196-ball Plastic Ball Grid Array (PBGA)
  - 176-ball Fine-pitch Ball Grid Array (FBGA)
- Enhanced Tx AGC control, eliminating the need for external gain-step compensa
- Enhanced I/O support for faster RS-232
- 16-bit wide Flash and SRAM support
- Backward compatible with cdmaOne standards

IS-2000 1x MC RTT Features supported by MSM5000

- Fast 800 Hz Forward Power Control
- Quasi-Orthogonal Functions
  - L= 256 chip, 4 masks
  - Increased number of available forward link channels
- Supplemental Channel (SCH) support
- IS-2000 Quick Paging Channel (F-QPCH) support
- Turbo and convolutional encoding/decoding for SCH
- FTU 144 kbps requirement achieved
  - 153.6 kbps SCH forward or reverse link
- Forward dedicated control channel (F-DCCH)
- Reverse dedicated control channel (R-DCCH)
- RLP3

IS-2000 Features not supported by MSM5000

- Orthogonal Transmit Diversity (OTD)
- Space Time Spreading Diversity (STS)
- Auxiliary Pilots
- 5 ms, 10 ms, 40 ms, and 80 ms framing
- New Reverse Link Common Channels (R-CCCH, R-EACH)
- Other new Forward Link Common Channels (F-CCCH, BCCH, CACH, CPCH)
- Simultaneous service options
- V2, V3, P3 modes



MSM5000 Functional Block Diagram

MSM Pin Names and Pinouts

Pin Name	Type	I_O[3] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
Memory Interface Pins						
A0 [UB_N]	B	3.0	Address bits[19:0]	111	G14	G13
A1	B	3.0		112	F13	H14
A2	B	3.0		113	F14	G12
A3	B	3.0		114	G12	F13
A4	B	3.0		115	F11	H15
A5	B	3.0		116	E14	G14
A6	B	3.0		117	E13	F12
A7	B	3.0		119	F12	G15
A8	B	3.0		120	D14	F14
A9	B	3.0		121	E11	E12
A10	B	3.0		122	D13	D13
A11	B	3.0		123	E12	E14
A12	O	3.0		124	C14	F15
A13	O	3.0		125	E10	D12
A14	O	3.0		126	C13	C13
A15	BS	3.0		128	D12	D14
A16	BS	3.0		129	B14	D15
A17	B	3.0		130	B13	C15
A18	BS	3.0		131	C12	C14
A19	BS	3.0		132	D11	B15

Pin Name	Type	I_O[3] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
GPIO_INT2	BS-PD	3.0, pd	This pin functions as the A22 address output when the ADDR_22_EN bit of the GPIO_INT_ADDR_SEL register is set (1). When this control bit is clear (0) and after the assertion of RESOUT_N, this pin has the GPIO_INT2 function. This pin is pulled to a logic low and has the GPIO_INT2 function upon powerup.	71	L9	R8
GPIO_INT3	BS-PD	3.0, pd	This pin functions as the A21 address output when the ADDR_21_EN bit of the GPIO_INT_ADDR_SEL register is set (1). When this control bit is clear (0) and after the assertion of RESOUT_N, this pin has the GPIO_INT3 function. This pin is pulled to a logic low and has the GPIO_INT3 function upon powerup.	72	P10	P9
GPIO_INT4	BS-PD	3.0, pd	This pin functions as the A20 address output when the ADDR_20_EN bit of the GPIO_INT_ADDR_SEL register is set (1). When this control bit is clear (0) and after the assertion of RESOUT_N, this pin has the GPIO_INT4 function. This pin is pulled to a logic low and has the GPIO_INT4 function upon powerup.	73	N10	M10

Pin Name	Type	I_O[a] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
D0	B-KP	3.0	Data bus bits[7:0]	93	L13	N14
D1	B-KP	3.0		94	L14	M15
D2	B-KP	3.0		95	K11	M13
D3	B-KP	3.0		96	K12	L12
D4	B-KP	3.0		98	K13	M14
D5	B-KP	3.0		99	K14	L13
D6	B-KP	3.0		100	J11	K12
D7	B-KP	3.0		101	J12	L14
D8	B-KP	3.0		102	J13	K15
D9	B-KP	3.0		103	J14	K13
D10	B-KP	3.0		104	H11	J12
D11	B-KP	3.0		105	H12	K14
D12	B-KP	3.0		107	H13	J13
D13	B-KP	3.0		108	H14	H12
D14	B-KP	3.0		109	G13	J14
D15	B-KP	3.0		110	G11	H13
GP_CS_N	O	3.0	General-purpose chip select output	43	M 3	N2
HWR_N	BS-PU	3.0, pu	Memory interface high-byte write strobe	86	N13	R13
LWR_N [WE_N]	BS-PU	3.0, pu	Memory interface low-byte write strobe	82	N12	N13
RAM_CS1_N	O	3.0	Memory interface RAM chip select 1 output	92	L12	M16
RAM_CS2_N [LB_N]	O	3.0	Memory interface RAM chip select 2 output	88	L11	R14
RD_N	BS	3.0	Memory interface read strobe	84	M11	P12
ROM_CS1_N	O	3.0	Memory interface ROM chip select 1 output	91	M14	P15
ROM_CS2_N	O	3.0	Memory interface ROM chip select 2 output	90	N14	P14

Pin Name	Type	I_O[3] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
Baseband Interface Pins						
ADC_CLK_SBCK	BS	2.0in SBI mode	Clock input from the general-purpose ADC on BBA. When high, ADC_DATA is valid. When the Serial Bus Interface is enabled, this pin becomes the SBCK clock output.	3	C1	B1
ADC_DATA_SBDT	BS-OD	2.0in SBI mode	Serial data input from the general-purpose ADC on BBA. When the Serial Bus Interface is enabled, this pin becomes the SBDT data port.	2	B1	B2
ADC_ENA_SBST	O	1.0	When this output goes high, the general-purpose ADC on BBA initiates an analog-to-digital conversion. When the Serial Bus Interface is enabled, this pin becomes the SBST start output.	1	C2	A1
C_RX_IDATA0	I-PD	pd	I-channel data (C_RX_IDATA[3:0]) input from the CDMA ADC on IFR3000	20	G1	H4
C_RX_IDATA1	I-PD	pd		19	G2	G3
C_RX_IDATA2	I-PD	pd		17	G3	F2
C_RX_IDATA3	I-PD	pd		16	G4	G4
C_RX_QDATA0	I-PD	pd	Q-channel data (C_RX_QDATA[3:0]) input from the CDMA ADC on IFR3000	15	F1	F3
C_RX_QDATA1	I-PD	pd		14	F2	F1
C_RX_QDATA2	I-PD	pd		13	F3	E2
C_RX_QDATA3	I-PD	pd		12	F4	F4
CHIPX8	I-PD	pd	9.8304 MHz clock input from IFR3000. CHIPX8 is used primarily for CDMA and vocoder processing.	21	H2	G2
FM_RX_CLK	O	1.0	Clock output to the Rx FM ADCs on IFR3000	10	E2	D2
FM_RX_IDATA	I-PD	pd	Serial data input for 8-bit FM Rx I-channel data from IFR3000	7	E4	D3
FM_RX_QDATA	I-PD	pd	Serial data input for 8-bit FM Rx Q-channel data from IFR3000	8	E3	E4
FM_RX_STB	O	1.0	Strobe output to the Rx FM ADCs on BBA. When high, initiates the FM ADCs to do an analog-to-digital conversion.	11	E1	E3
TX_CLK	O	2.0	Clock output to the CDMA I-channel transmit DAC	23	H1	J3
TX_CLK_N	O	2.0	Clock output to the CDMA Q-channel transmit DAC	22	H4	H3

Pin Name	Type	I_O[3] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
TX_IQDATA0	O	1.0	I- and Q-channel Tx data (TX_IQDATA[7:0]) output from MSM3000 to IFT3000	32	L1	K2
TX_IQDATA1	O	1.0		31	J3	J1
TX_IQDATA2	O	1.0		29	K2	K4
TX_IQDATA3	O	1.0		28	K1	J2
TX_IQDATA4	O	1.0		27	J4	H1
TX_IQDATA5	O	1.0		26	H3	K3
TX_IQDATA6	O	1.0		25	J1	J4
TX_IQDATA7	O	1.0		24	J2	H2
Codec Interface Pins						
AUX_PCM_CLK	O	3.0	PCM data clock for Auxiliary CODEC port	142	B10	B12
AUX_PCM_DIN	IS-PD	pd	PCM data input for Auxiliary CODEC port	139	D10	C12
AUX_PCM_DOUT	O	3.0	PCM data output for Auxiliary CODEC port	138	A11	A12
AUX_PCM_SYNC	BS-PD	3.0	PCM data strobe for Auxiliary CODEC port	140	C10	D11
PCM_CLK	B-PD	2.0, pd	Data clock for receive and transmit PCM data	137	B11	B13
PCM_DIN	I-PD	pd	Serial PCM data input	135	A12	A14
PCM_DOUT	Z-PD	2.0, pd	Serial PCM data output	134	A13	B14
PCM_SYNC	B-PD	2.0, pd	Data strobe for receive and transmit PCM data	136	C11	A13
WDOGSTB_PCMSCS	O	2.0	This pin functions as the PCM_SCS output for the CODEC interface when the WDOGSTB_SCS_SEL bit of the CODEC_CTL2 register is set (1). When this bit is clear (0), this pin is the Watchdog Strobe (WDOGSTB) output. Upon assertion of RESOUT_N, this pin has the WDOGSTB function.	133	B12	A15

Pin Name	Type	I_O[3] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
UART and MIN Counter Pins						
CTS_N	IS-PD	pd	UART Clear-To-Send signal	52	M5	M5
DP_RX_DATA	IS-PD	pd	UART Input	51	L5	M4
DP_TX_DATA	O	3.0	UART output	50	P4	R4
RFR_N	O	3.0	UART Ready-For-Receive signal	54	N5	P4
AUX_PCM_CLK	O	3.0	This pin functions as the RFR2_N (Ready-For-Receive) pin of UART2 when the UART2_SEL bit of the CODEC_CTL2 register is set (1). When this control bit is clear (0), this pin is the PCM data clock for the Auxiliary CODEC port. After assertion of RESOUT_N, this pin has the AUX_PCM_CLK function	142	B10	B12
AUX_PCM_DIN	IS-PD	pd	This pin functions as the DP_RX_DATA2 (Data Input) pin of UART2 when the UART2_SEL bit of the CODEC_CTL2 register is set (1). When this control bit is clear (0), this pin is the PCM data input for the Auxiliary CODEC port. After assertion of RESOUT_N, this pin has the AUX_PCM_DIN function.	139	D10	C12
AUX_PCM_DOUT	O	3.0	This pin functions as the DP_TX_DATA2 (Data Output) pin of UART2 when the UART2_SEL bit of the CODEC_CTL2 register is set (1). When this control bit is clear (0), this pin is the PCM data output for the Auxiliary CODEC port. After assertion of RESOUT_N, this pin has the AUX_PCM_DOUT function.	138	A11	A12
AUX_PCM_SYNC	BS-PD	3.0	This pin functions as the CTS2_N (Clear-To-Send) pin of UART2 when the UART2_SEL bit of the CODEC_CTL2 register is set (1). When this control bit is clear (0), this pin is the PCM data strobe for the Auxiliary CODEC port. After assertion of RESOUT_N, this pin has the AUX_PCM_SYNC function.	140	C10	D11
YAMN1	O	1.0	General-purpose microprocessor-programmable M/N counter that is clocked by TCXO	48	M4	R3
GP_CS_N	O	3.0	General-purpose chip select output 2	43	M3	N2

Pin Name	Type	I_O[a] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
General-purpose I/O and Interrupt Pins						
GPIO0	BS-PU	1.0, pu	General-purpose I/O pins which are programmed as inputs on RESOUT_N	167	C5	B5
GPIO1	BS-PU	1.0, pu		166	B4	C4
GPIO2	BS-PU	1.0, pu		165	D5	D5
GPIO3	BS-PU	1.0, pu		164	A4	B6
GPIO4	BS-PU	1.0, pu		163	C6	A7
GPIO5	BS-PU	1.0, pu		160	A5	B7
GPIO6	BS-PU	1.0, pu		158	D6	A8
GPIO7	BS-PU	1.0, pu		157	A6	D7
GPIO8	BS-PD	1.0, pd		155	B6	B8
GPIO9	BS-PD	1.0, pd		154	D7	C8
GPIO10	BS-PD	1.0, pd		153	B7	B9
GPIO11	BS-PU	1.0, pu		151	B8	C9
GPIO12	BS-PU	1.0, pu		148	D8	D9
GPIO13	BS-PD	1.0, pd	General-purpose I/O pin which is programmed as an input on RESOUT_N	147	A9	C10
GPIO14	BS-PD	1.0, pd	General-purpose I/O pin	146	B9	A10
GPIO15	BS-PD	1.0, pd	General-purpose I/O pin	145	C9	B11
GPIO16	BS-PD	1.0, pd	General-purpose I/O pin	144	D9	D10
GPIO17	BS-PD	1.0, pd	General-purpose I/O pin	55	P6	N5
GPIO18	BS-PD	1.0, pd	General-purpose I/O pin	56	L6	M6

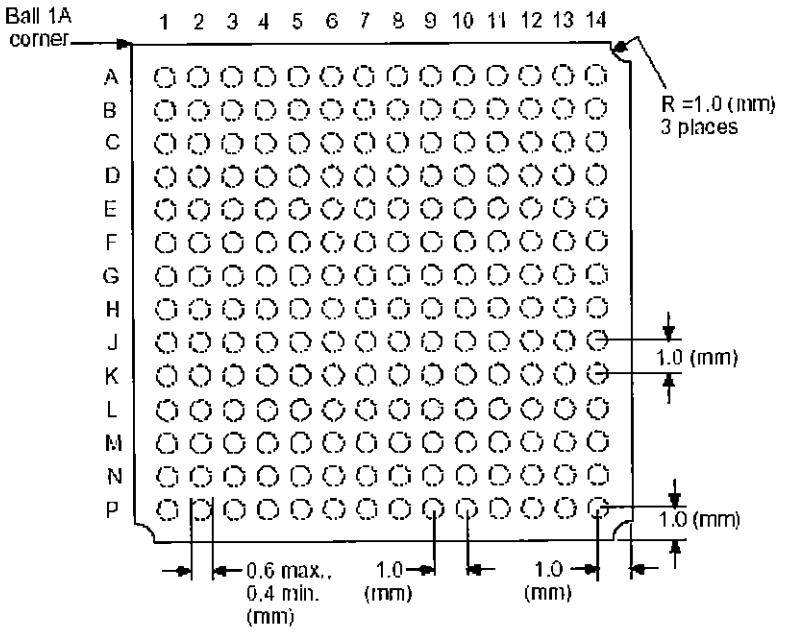
Pin Name	Type	I_O[a] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
GPIO19	BS-PD	1.0, pd	General-purpose I/O pins which are programmed as inputs on RESOUT_N	57	M6	P5
GPIO20	BS-PD	1.0, pd		58	N6	R5
GPIO21	BS-PD	1.0, pd		59	P6	N6
GPIO22	BS-PD	1.0, pd		60	L7	M7
GPIO23	BS-PD	1.0, pd		61	M7	P6
GPIO24	BS-PD	1.0, pd		63	N7	N7
GPIO25	BS-PD	1.0, pd		64	P7	M8
GPIO26	BS-PD	5.0, pd		65	N8	P7
GPIO27	BS-PD	5.0, pd		66	L8	N8
GPIO28	BS-PD	5.0, pd		67	P8	N9
GPIO29	BS	5.0	This pin can be configured to output the signal WSYM_CLK. See the description for the GPIO_FUNCTION_SEL register.	68	N9	P8
GPIO30	BS	5.0	This pin can be configured to output MASK_DATA, VOC_FR_REF, SYNC80M or WDOBSTB_PCMSCS. See the description for the GPIO_FUNCTION_SEL register.	37	K5	M4
GPIO_INT0	BS-PU	1.0, pu	General-purpose I/O pins. The GPIO_INT[4:0] pins can cause an interrupt to the microprocessor. These pins are maskable, level-sensitive, and have programmable polarity. GPIO_INT[4:2] can be configured to output the latched peripheral address bits A[22:20]. See the description for the GPIO_INT_ADDR_SEL register.	69	P9	M9
GPIO_INT1	BS-PU	1.0, pu		70	M8	N10
GPIO_INT2	BS-PD	3.0, pd		71	L9	R8
GPIO_INT3	BS-PD	3.0, pd		72	P10	P9
GPIO_INT4	BS-PD	3.0, pd		73	N10	M10
User Interface Pins						
KEYSENSE0_N	IS-PU	pu	Can be used to sense key contact closure when connected to an external keypad. These pins require an active-low level-sensitive input signal. Can cause interrupt to the microprocessor.	173	A2	A4
KEYSENSE1_N	IS-PU	pu		172	C4	B4
KEYSENSE2_N	IS-PU	pu		170	B3	C3
KEYSENSE3_N	IS-PU	pu		169	E5	D4
KEYSENSE4_N	IS-PU	pu		168	A3	A6
LCD_CS_N	O	3.0	LCD chip select output	143	A10	C11
LCD_E	O	3.0	Parallel LCD interface enable strobe	85	P13	R12

Pin Name	Type	I_O[a] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
RINGER	O	5.0	The signal on the RINGER output comes from the MSM3000 DTMF tone generator. The DTMF generator selects the pitch and cadence of the subscriber unit's ring. RINGER drives the sound transducer.	49	N4	P3
RF Interface Pins						
I_OFFSET	Z-PD	2.0, pd	PDM output from the I-channel offset correction loop. I_OFFSET reduces offset errors on I-channel data.	4	D3	C1
IDLE_N	BS-PD	5.0, pd	Low when subscriber unit is in IDLE mode. IDLE_N can be used to disable unused circuits in the subscriber unit. IDLE_N is an input on RESOUT_N.	38	M 2	N3
LNA_GAIN	Z-PD	5.0	PDM output from the RX AGC subsystem in the MSM3000. This signal, when filtered with a simple RC lowpass filter, is useful for controlling the gain of a variable gain low-noise amplifier (LNA). Additionally, this pin can be configured as a third general-purpose PDM.	89	M13	R15
LNA_RANGE	Z-OD	2.0, od	Digital output from the CDMA Rx AGC loop. Can be used to alter low-noise amplifier characteristics or other stages in the subscriber unit's Rx signal path. This output pin has an open-drain structure. An external pull-up resistor is required.	42	N2	N1
PA_ON	O	5.0	Control signal that controls the subscriber unit's RF power amplifier. PA_ON is high only when the RF power amplifier is needed for transmission.	44	L4	P1
PA_ON2	O	5.0	Control signal for a second power amplifier	87	M12	P13
PA_R0	Z-OD	2.0, od	Digital output from the CDMA Tx AGC loop. Can be used to alter subscriber unit's RF power amplifier characteristics. This output pin has an open-drain structure. An external pull-up resistor is required.	40	L3	M2
PA_R1	Z-OD	2.0, od		41	N1	M1
PDM1	Z-PD	5.0, pd	General-purpose PDM outputs clocked by TCXO and under microprocessor control	46	P2	P2
PDM2	Z-PD	5.0, pd		47	P3	R2
Q_OFFSET	Z-PD	2.0, pd	PDM output from the Q-channel offset correction loop. Q_OFFSET reduces offset errors on Q-channel data.	5	D2	C2

Pin Name	Type	I_O[a] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
RX_AGC_ADJ	Z-PD	5.0, pd	PDM output from the Rx AGC subsystem in MSM5000. RX_AGC_ADJ sets the Rx signal level in the MSM5000.	36	M1	K1
SLEEP_N	O	5.0	This output is low when the subscriber unit is in SLEEP mode. SLEEP_N can be used to disable unused circuits in the subscriber unit.	6	D1	D1
SYNTH_LOCK	IS	—	Indicates the lock status of UHF and IF frequency synthesizers. SYNTH_LOCK normally comes from the BBA and other frequency synthesizers in the subscriber unit's RF section.	33	K4	L4
TCXO	I-PD	pd	TCXO clock input	34	L2	M3
TRK_LO_ADJ	Z	5.0	PDM output from the frequency tracking subsystem in MSM5000. TRK_LO_ADJ sets the subscriber unit's IF and UHF frequencies.	45	N3	R1
TX_AGC_ADJ	Z-PD	5.0, pd	PDM output from the Tx AGC subsystem in MSM5000. TX_AGC_ADJ controls the Tx output power.	35	K3	L2
Microprocessor and Control Pins						
MODE0	IS-PU	pu	MODE[1:0] determine the operating mode for the MSM3000. IF MODE[1:0] = 10, selects MOUSE mode. IF MODE[1:0] = 11, selects NATIVE mode. IF MODE[1:0] = 01, selects HI-Z mode. MODE[1:0] = 00 is reserved. DO NOT USE. If unconnected, MODE[1:0] are pulled high selecting NATIVE mode.	174	B2	A3
MODE1	IS-PU	pu		175	C3	B3
RESIN_N	IS	—	Hardware reset input to the system	75	M9	R9
RESOUT_N	BS	3.0	Reset output from the microprocessor	76	P11	P10
SLEEP_XTAL_IN	IA	—	Low-power sleep controller crystal oscillator input	78	N11	N12
SLEEP_XTAL_OUT	OA	—	Sleep controller crystal oscillator output	81	K10	M12
WDOG_EN	IS-PU	pu	Watchdog Timer enable input	77	L10	M11
WDOGSTB_PCMSCS	O	2.0	Serial PCM control select	133	B12	A15
XTAL_IN	IA	—	Input connection point for an external quartz crystal or ceramic resonator. If an external oscillator is used, the output of the oscillator must be connected to this pin.	79	M10	P11

Pin Name	Type	I_O[a] (mA)	Pin Description	Pin Number		
				176-TQFP	196-PBGA	176-FBGA
XTAL_OUT	OA	—	Feedback connection for an external quartz oscillator or ceramic resonator. If an external oscillator is used, this pin must be unconnected.	80	P12	R10
JTAG Interface Pins						
TCK	IS-PU	pu	JTAG port clock input	158	C7	C6
TDI	IS-PU	pu	JTAG port data input	152	A8	D8
TDO	Z	3.0	JTAG port data output	155	A7	C7
TMODE	IS-PU	pu	IEEE 1149.1A-1993 standard compliant enable input. When set (1), the MSM3000 JTAG ports are selected. when clear (0) the ARM JTAG ports are selected.	176	D4	A2
TMS	IS-PU	pu	JTAG port mode select input	161	B5	D6
TRST_N	IS-PU	pu	JTAG port reset input	149	C8	B10
Power and Ground Pins						
V_{DD}	V	—	Power Supply Voltage	18, 39, 62, 83, 106, 127, 150, 171	E6, E9, F5, F10, J5, J10, K6, K9	A5, A9, E15, G1, J15, L1, R7, R11
GND	V	—	Ground	9, 30, 53, 74, 97, 118, 141, 162	E7, E8, F6, F7, F8, F9, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J6, J7, J8, J9, K7, K8	A11, C5, E1, E13, L3, L15, N11, R5
N/C	—	—	No connection	-	A1, P1, A14, P14	-

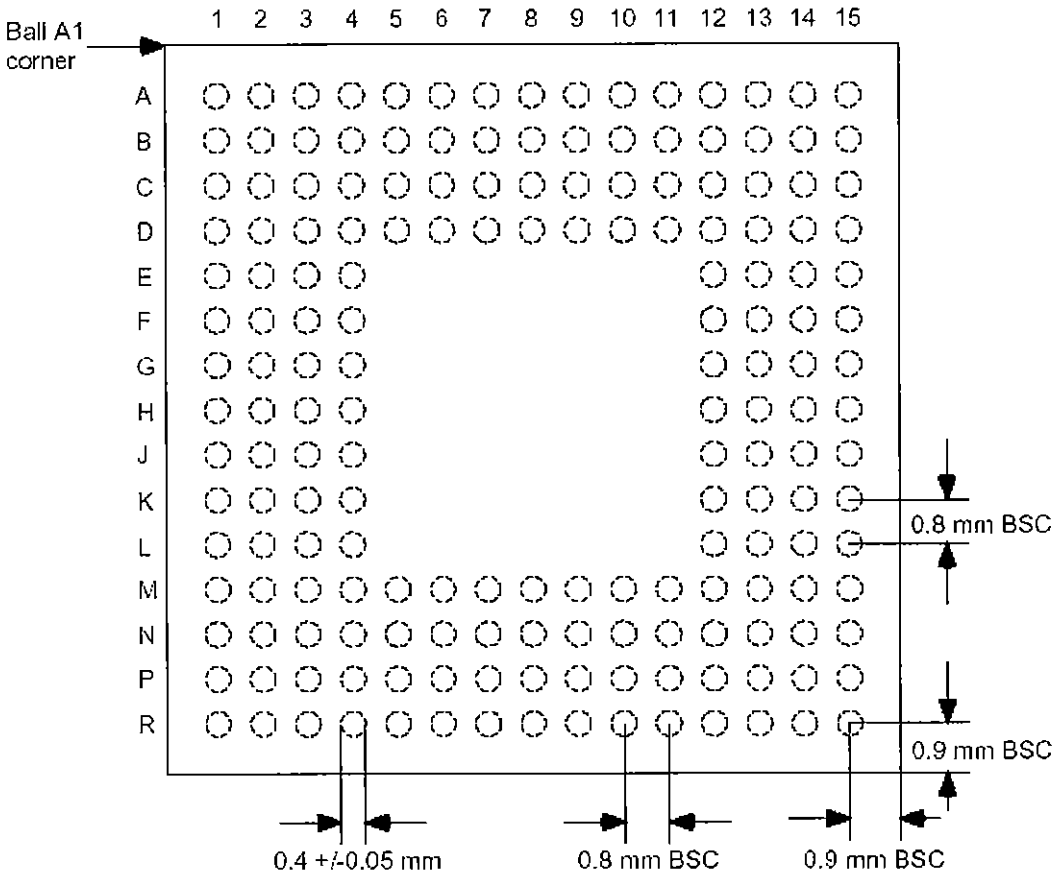
[a] Values 1.0, 2.0, 3.0, and 5.0 are the ± maximum current drive levels in mA for output pins. pd = internal pull-down resistor on input pin. pu = internal pull up resistor on input pin. od = open drain. In = no pull-up or pull-down resistor present when used as an input



Solderball Material is 63% Sn / 37% Pb

TOP VIEW
(balls hidden below package body)
(All dimensions in mm)

MSM5000 **196-Ball PBGA Pinout**



TOP VIEW
(Solder balls hidden below package)

MSM5000 **176-Ball FBGA Pinout**

	1	2	3	4	5	6	7
A	NC	KEYSENSE0_N	KEYSENSE4_N	GPIO3	GPIO5	GPIO7	TDO
B	ADC_DATA_SBDT	MODE0	KEYSENSE2_N	GPIO1	TMS	GPIO8	GPIO10
C	ADC_CLK_SBCK	ADC_ENA_SBST	MODE1	KEYSENSE1_N	GPIO0	GPIO4	TCK
D	SLEEP_N	Q_OFFSET	I_OFFSET	TMODE	GPIO2	GPIO6	GPIO9
E	FM_RX_STB	FM_RX_CLK	FM_RX_QDATA	FM_RX_IDATA	KEYSENSE3_N	VDD	GND
F	C_RX_QDATA0	C_RX_QDATA1	C_RX_QDATA2	C_RX_QDATA3	VDD	GND	GND
G	C_RX_IDATA0	C_RX_IDATA1	C_RX_IDATA2	C_RX_IDATA3	GND	GND	GND
H	TX_CLK	CHIPX8	TX_IQDATA5	TX_CLK_N	GND	GND	GND
J	TX_IQDATA6	TX_IQDATA7	TX_IQDATA1	TX_IQDATA4	VDD	GND	GND
K	TX_IQDATA3	TX_IQDATA2	TX_AGC_ADJ	SYNTH_LOCK	GPIO30	VDD	GND
L	TX_IQDATA0	TCXO	PA_R0	PA_ON	DP_RX_DATA	GPIO18	GPIO22
M	RX_AGC_ADJ	IDLE_N	GP_CS_N	YAMN1	CTS_N	GPIO19	GPIO23
N	PA_R1	LNA_RANGE	TRK_LO_ADJ	RINGER	RFR_N	GPIO20	GPIO24
P	NC	PDM1	PDM2	DP_TX_DATA	GPIO17	GPIO21	GPIO25

	8	9	10	11	12	13	14
A	TDI	GPIO13	LCD_CS_N	AUX_PCM_DOUT	PCM_DIN	PCM_DOUT	NC
B	GPIO11	GPIO14	AUX_PCM_CLK	PCM_CLK	WDOGSTB_PCMSCS	A17	A16
C	TRST_N	GPIO15	AUX_PCM_SYNC	PCM_SYNC	A18	A14	A12
D	GPIO12	GPIO16	AUX_PCM_DIN	A19	A15	A10	A8
E	GND	VDD	A13	A9	A11	A6	A5
F	GND	GND	VDD	A4	A7	A1	A2
G	GND	GND	GND	D15	A3	D14	A0
H	GND	GND	GND	D10	D11	D12	D13
J	GND	GND	VDD	D6	D7	D8	D9
K	GND	VDD	SLEEP_XTAL_OUT	D2	D3	D4	D5
L	GPIO27	GPIO_INT2	WDOG_EN	RAM_CS2_N	RAM_CS1_N	D0	D1
M	GPIO_INT1	RESIN_N	XTAL_IN	RD_N	PA_ON2	LNA_GAIN	ROM_CS1_N
N	GPIO26	GPIO29	GPIO_INT4	SLEEP_XTAL_IN	LWR_N	HWR_N	ROM_CS2_N
P	GPIO28	GPIO_INT0	GPIO_INT3	RESOUT_N	XTAL_OUT	LCD_E	NC

196-Ball PBGA Pinout for the MSM5000 (Top View)

	1	2	3	4	5	6	7	8
A	ADC_ENA_SBST	TMODE	MODE0	KEYSENSE0_N	VDD	KEYSENSE4_N	GPIO4	GPIO6
B	ADC_CLK_SBCK	ADC_DATA_SBDT	MODE1	KEYSENSE1_N	GPIO0	GPIO3	GPIO5	GPIO8
C	I_OFFSET	Q_OFFSET	KEYSENSE2_N	GPIO1	GND	TCK	TDO	GPIO9
D	SLEEP_N	FM_RX_CLK	FM_RX_IDATA	KEYSENSE3_N	GPIO2	TMS	GPIO7	TDI
E	GND	C_RX_QDATA2	FM_RX_STB	FM_RX_QDATA				
F	C_RX_QDATA1	C_RX_IDATA2	C_RX_QDATA0	C_RX_QDATA3				
G	VDD	CHIPX8	C_RX_IDATA1	C_RX_IDATA3				
H	TX_IQDATA4	TX_IQDATA7	TX_CLK_N	C_RX_IDATA0				
J	TX_IQDATA1	TX_IQDATA3	TX_CLK	TX_IQDATA6				
K	RX_AGC_ADJ	TX_IQDATA0	TX_IQDATA5	TX_IQDATA2				
L	VDD	TX_AGC_ADJ	GND	SYNTH_LOCK				
M	PA_R1	PA_R0	TCXO	GPIO30	CTS_N	GPIO18	GPIO22	GPIO25
N	LNA_RANGE	GP_CS_N	IDLE_N	DP_RX_DATA	GPIO17	GPIO21	GPIO24	GPIO27
P	PA_ON	PDM1	RINGER	RFR_N	GPIO19	GPIO23	GPIO26	GPIO29
R	TRK_LO_ADJ	PDM2	YAMN1	DP_TX_DATA	GND	GPIO20	VDD	GPIO_INT2

	9	10	11	12	13	14	15
A	VDD	GPIO14	GND	AUX_PCM_DOUT	PCM_SYNC	PCM_DIN	WDOGSTB_PCMSCS
B	GPIO10	TRST_N	GPIO15	AUX_PCM_CLK	PCM_CLK	PCM_DOUT	A19
C	GPIO11	GPIO13	LCD_CS_N	AUX_PCM_DIN	A14	A18	A17
D	GPIO12	GPIO16	AUX_PCM_SYNC	A13	A10	A15	A16
E				A9	GND	A11	VDD
F				A6	A3	A8	A12
G				A2	A0	A5	A7
H				D13	D15	A1	A4
J				D10	D12	D14	VDD
K				D6	D9	D11	D8
L				D3	D5	D7	GND
M	GPIO_INT0	GPIO_INT4	WDOG_EN	SLEEP_XTAL_OUT	D2	D4	D1
N	GPIO28	GPIO_INT1	GND	SLEEP_XTAL_IN	LWR_N	D0	RAM_CS1_N
P	GPIO_INT3	RESOUT_N	XTAL_IN	RD_N	PA_ON2	ROM_CS2_N	ROM_CS1_N
R	RESIN_N	XTAL_OUT	VDD	LCD_E	HWR_N	RAM_CS2_N	LNA_GAIN

176-Ball FBGA Pinout for the MSM5000 (Top View)

5.3 AUDIO unit

The audio unit consist of codec ic and buzzer part.

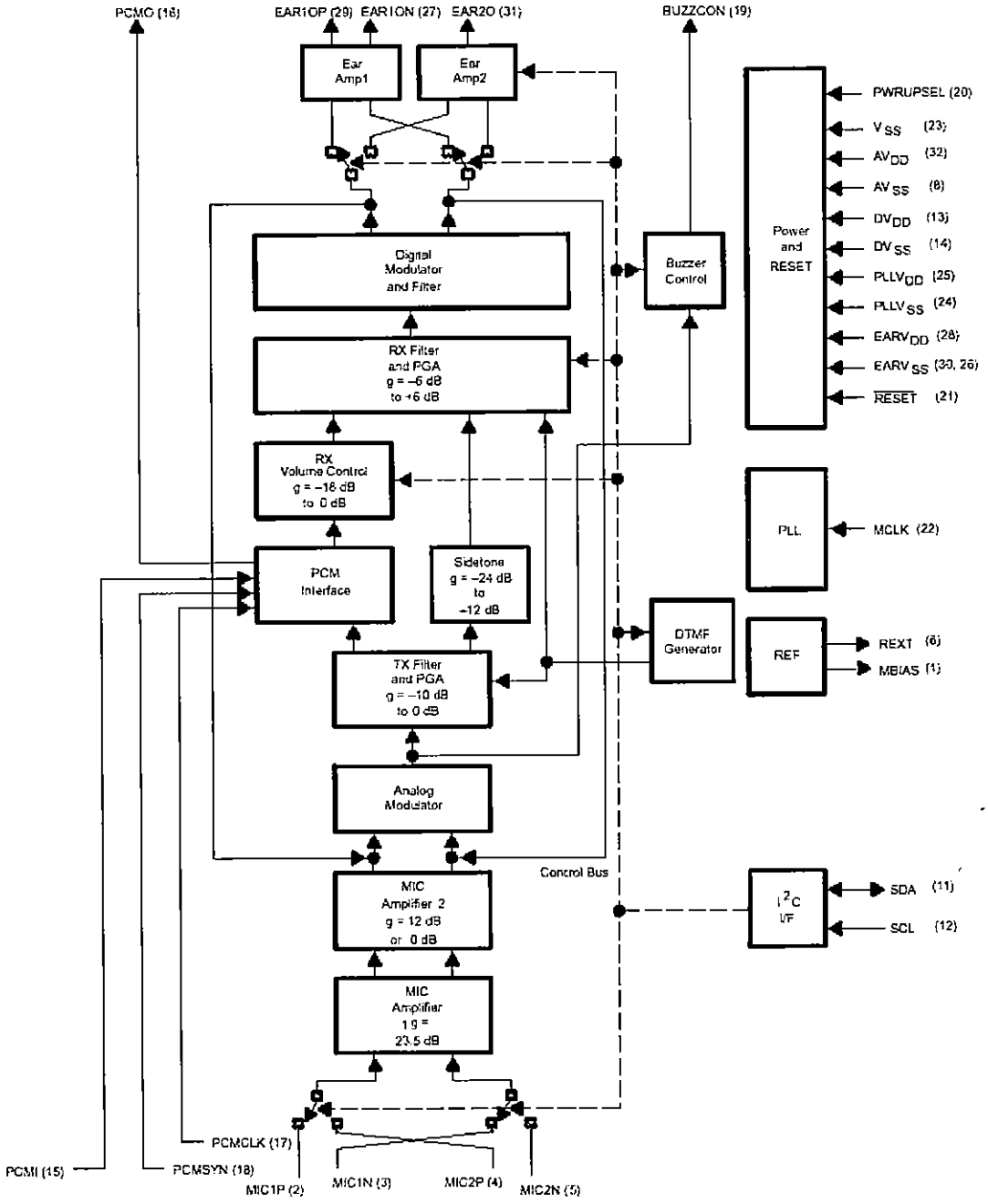


Figure 4. Audio unit configuration diagram

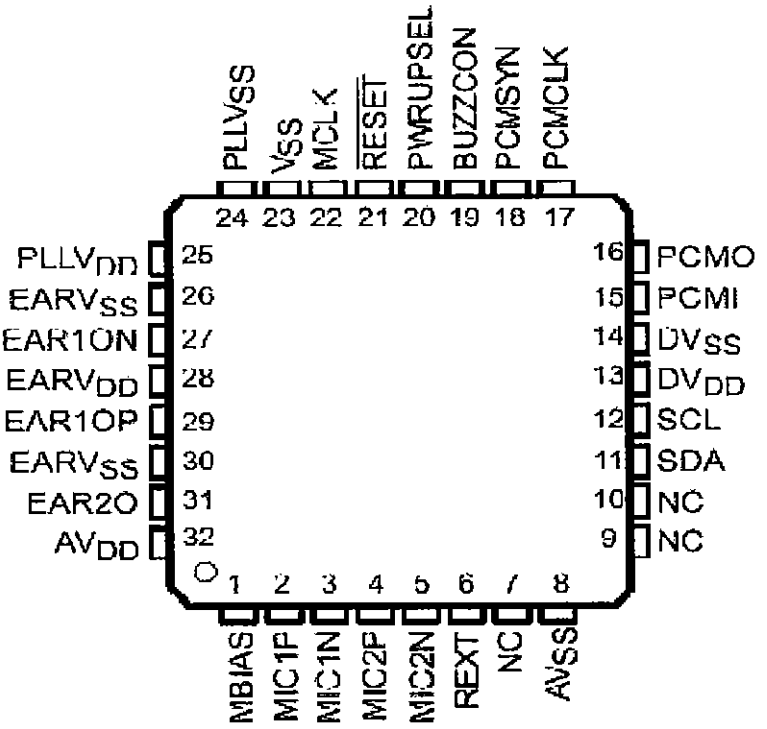
In the figure 4, the input voice signal goes to PCM CODEC. It is amplified to appropriate level in the PCM CODEC

amplification circuit and sent to transmit filter circuit.

PCM CODEC filter receives PCM_CLK (2.048MHz) and PCM_SYNC (8KHz) from MSM and samples the input voice signal at 8KHz, converts to 64Kbps digital signal (PCM_IN) and input to MSM.

In receive mode, itconverts the 64Kbps digital signal (PCM_OUT) coming from MSM to D/A at CODEC IC.

It is then amplified to an appropriate level by the differential amplifier in PCM CODEC and the output signal is sent to SLIC IC which allows it to be heard on an ordinary phone through TEL LINE.

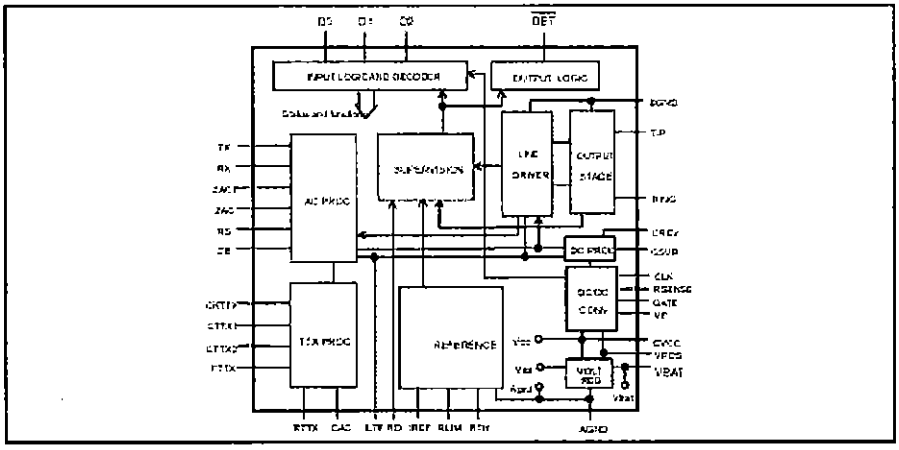


Terminal Functions

TERMINAL NAME	NO. µBGA	NO. PBS	I/O	DESCRIPTION
AV_{DD}	A1	32	I	Analog positive power supply
AV_{SS}	J1	8	I	Analog negative power supply
BUZZCON	F9	19	O	Buzzer output, a pulse-density modulated signal to apply to external buzzer driver
DV_{DD}	J6	13	I	Digital positive power supply
DV_{SS}	J7	14	I	Digital negative power supply
EAR1ON	A6	27	O	Earphone 1 amplifier output (–)
EAR1OP	A4	29	O	Earphone 1 amplifier output (+)
EAR2O	A2	31	O	Earphone 2 amplifier output
$EARV_{DD}$	A5	28	I	Analog positive power supply for the earphone amplifiers
$EARV_{SS}$	A3, A7	30, 26	I	Analog negative power supply for the earphone amplifiers
MBIAS	B1	1	O	Microphone bias supply output, no decoupling capacitors
MCLK	C9	22	I	Master system clock input (2.048 MHz) (digital)
MIC1P	C1	2	I	MIC1 input (+)
MIC1N	D1	3	I	MIC1 input (–)
MIC2P	E1	4	I	MIC2 input (+)
MIC2N	F1	5	I	MIC2 input (–)
PCM	J8	15	I	Receive PCM input
PCMO	J9	16	O	Transmit PCM output
PCMSYN	G9	18	I	PCM frame synchronization
PCMCLK	H9	17	I	PCM data clock
$PLLV_{SS}$	A9	24	I	PLL negative power supply
$PLLV_{DD}$	A8	25	I	PLL digital power supply
PWRUPSEL	E9	20	I	Selects the power-up default mode
REXT	G1	6	I/O	Internal reference current setting terminal—use precision 100-kΩ resistor and no filtering capacitors
$\overline{RESET}$	D9	21	I	Active low reset
SCL	J5	12	I	I^2C-bus serial clock—this input is used to synchronize the data transfer from and to the VBAP
SDA	J4	11	I/O	I^2C-bus serial address/data input/output—this is a bidirectional terminal used to transfer register control addresses and data into and out of the CODEC. It is an open-drain terminal and therefore requires a pullup resistor to V_{DD} (typical 10 kΩ for 100 kHz)
V_{SS}	B9	23	I	Ground return for bandgap internal reference

5.4 SLIC and Caller id unit

BLOCK DIAGRAM



. SLIC IC BLOCK

It has the function of connecting WLL terminal and standard telephone.

SLIC IC (U902) operates on control signal from MSM, and the internal DC-DC converter generates power to operate standard telephone.

The built-in hook detector monitors the on/off hook of the ordinary telephone and sends signals to MSM.

The voice signal coming out of CODEC is amplified to an appropriate level and sent to the ordinary telephone via tip ring end after going through SLIC IC. Reversely, the voice signal from an ordinary telephone is sent to MIC input of CODEC IC after going through SLIC IC.

U903 generates the metering pulse clock (12/16 kHz).

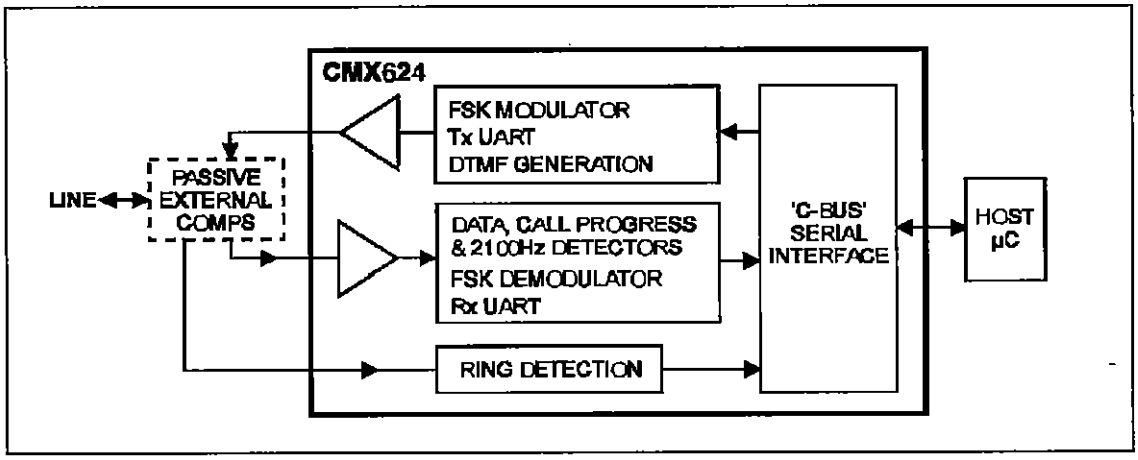
When a number is pressed on standard telephone to dial a number, U901 (DTMF receiver IC) analyses the signal coming out of SLIC IC an determines the pressed number and sends it to MSM.

Pin description (STLC3055)

Pin No.	Name	Function
25	VPOS	Positive supply input range from 5.5V ~ 15.8V
34	BGND	Battery Ground. must be short AGND
27	AGND	Analog Ground. must be short BGND
16	ZAC	AC impedance synthesis.
15	ZAC1	RX buffer output, the AC impedance IC connected form this node ti ZAC
17	RS	Protection resistors image (the image resistor is connected from this node to ZAC)
18	ZB	Balance Network for 2 or 4 wire conversion (the balance impedance ZB is connected from this node to AGND. ZA impedance is connected from this node to ZAC1)

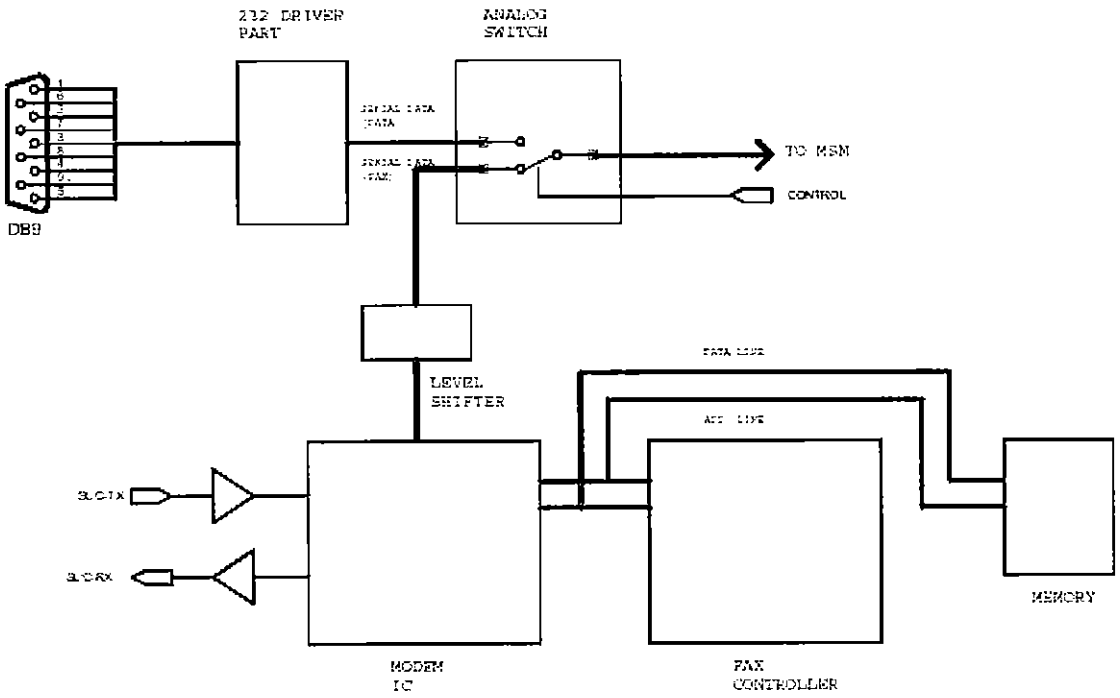
20	TX	4 wire output port (TX output). The signal is referred to AGND. If connected to signal supply CODEC input it must be DC decoupled with proper capacitor.
14	RX	4 wire input port (RX input); 300KΩ input impedance. This signal is referred to AGND. If connected to signal supply CODEC output it must be DC decoupled with proper capacitor.
19	CAC	AC feed back input. AC/DC split capacitor (CAC)
32	ILTF	Transversal line current image output
41	TIP	2 wire port; TIP wire (Ia is the current sourced from this pin)
37	RING	2 wire port; RING wire (Ib is the sunk into this pin)
c28	RLIM	Constant current feed programming pin (via RLIM). RLIM should be connected close to this pin and PCB layout should avoid noise injection on this pin.
30	RTH	Off-hook threshold programming port (via RTH). RTH should be connected close to this pin and PCB layout should avoid noise injection on this pin.
29	IREF	Internal bias current setting pin. IREF should be connected close to this pin and PCB layout should avoid noise injection on this pin.
43	CREV	Reverse polarity transition time control. One proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. This is the transition time used to shapethe "trapezoidal ringing" during ringing injection
31	RD	DC feedback and ring trip input. RD should be connected close to this pin and PCB layout should avoid noise injection on this pin.
4	PD	Power Down input. Normally connected to CVCC(or to logic level high). Can be used to set TIP and Ring terminal in open circuit setting PD=0 and D0=D1=0.
26	CVCC	Internal positive voltage supply filter.
35	VBAT	Regulated battery voltage self granted by the device via DC/DC converter. Must be should to VBAT1.
23	GATE	Driver to external Power MOD transistor
21	VF	Feedback input DC/DC converter controller
22	CLK	Power Switch Control Clock (typ. 125KHz)
24	RSENSE	Voltage input for current sensing. RSENSE should be connected close this pin and VOP pin. The PCB layout should minimize the extra resistance introduced by the copper tracks.
1	D0	Control interface: input bit 0.
2	D1	Control interface: input bit 1.
3	D2	Control interface: input bit 2.
8	DET/	Logic interface output of the supervision detector (active low).
33	CSVR	Battery supply filter capacitor.
12	RTTX	Metering pulse cancellation buffer output. TTX filter network should be connected to this point. If nit used should be left open

13	FTTX	Metering pulse buffer input this signal is sent to the line and perform TTX filtering
10	CTTX1	Metering burst shapingexternal capacitor.
11	CTTX2	Metering burst shapingexternal capacitor
9	CKTTX	Metering pulse clock input (12KHz or 16KHz square wave).
33	VBAT1	Frame connection. Must be should to VBAT
5	RES	Reserved, must be connected to AGND.
6,7,36,38,39 ,40,42	NC	Not connected



Caller id unit generate FSK signal . This FSK signal has caller's information.

5.5 DATA SVC unit/ FAX unit



Data SVC / FAX configuration diagram

This unit composes the data service and G3 fax of WLL terminal and uses the MSM serial port.

The data service is accessed by connecting the DB9 connector to a PC (Personal Computer).

Only 1:1 9 pin cable can be used for this purpose.

The signal input through Jack 801 goes through RS232 driving part (Q801~Q808) to be converted to logic level data and input to MSM serial data port through analog switch IC (U802). At this time, data service or fax is selected by MSM control.

When using G3 fax, an identification number (e.g.: *00) must be prefixed in front of the telephone number in order to differentiate from data communication. At this time MSM delivers an enable signal to regulator (U005), and operation starts with power supply to fax unit.

During fax transmission, the fax input signal, having gone through SLIC unit, is amplified by AMP (U902) and input to fax modem IC (U901). This signal is converted to data by fax controller (U900) and temporarily stored in RAM.

The data stored in RAM is converted to serial data by fax controller and delivered to MSM. At this time, in order to make adjustments to the voltage difference between the fax power of 5V and MSM power of 3.3V, it goes through the level shifter (U910).

It is the reverse of the above in case of fax reception. Serial data sent by MSM are temporarily stored in RAM, then sent to fax modem IC. This is converted to an analog signal by fax modem IC, then goes through AMP(U902), SLIC

and then analog G3 fax.

FC100-M

Pin name	Pin No.	I/O	Pin description
MIRQN	135	I	Modem interrupt active low
SYSCLK	133	I	System clock
TSTCLK	130	O	Test clock
A[23:0]	[1:6][8:13][15:20] [22:27]	O	Address bus
D[7:0]	[136:139][141:144]	I/O	Data bus
RDN	128	O	Read strobe
WRN	127	O	Write strobe
ROMCSN	120	O	ROM Chip select
CS1N	122	O	I/O chip select
CS0N	57	O	SRAM chip select
MCSN	121	O	Modem chip select
SYNC	126	O	Indicates CPU op code fetch cycle
REGDMA	124	O	Indicates REGSEI cycle and cycle
WAITN	125	O	Indicates current TSTCLK cycle is a wait state or a halt state
RASN	113	O	DRAM row address select
CAS[1:0]N	[111:112]	O	DRAM column address select
DWRN	109	O	DRAM write
DEBUGN	129	I	External non-maskable input
RESETN	131	I/O	EC100/200 Reset
TEST	58	I	Sets Test mode
XIN	59	I	Crystal oscillator input pin
XOUT	60	O	Crystal oscillator output pin
PWRDWNN	62	I	Used by external system to indicate-to FC100/200-loss of prime power
BATRSTN	61	I	Battery power reset input
WRPROTN	110	O	Write protect during loss of VDD power
START	101	O	Scanner shift gate control
CLK1	100	O	Scanner clock
CLK1N	99	O	Scanner clock-inverted
CLK2	98	O	Scanner reset gate control

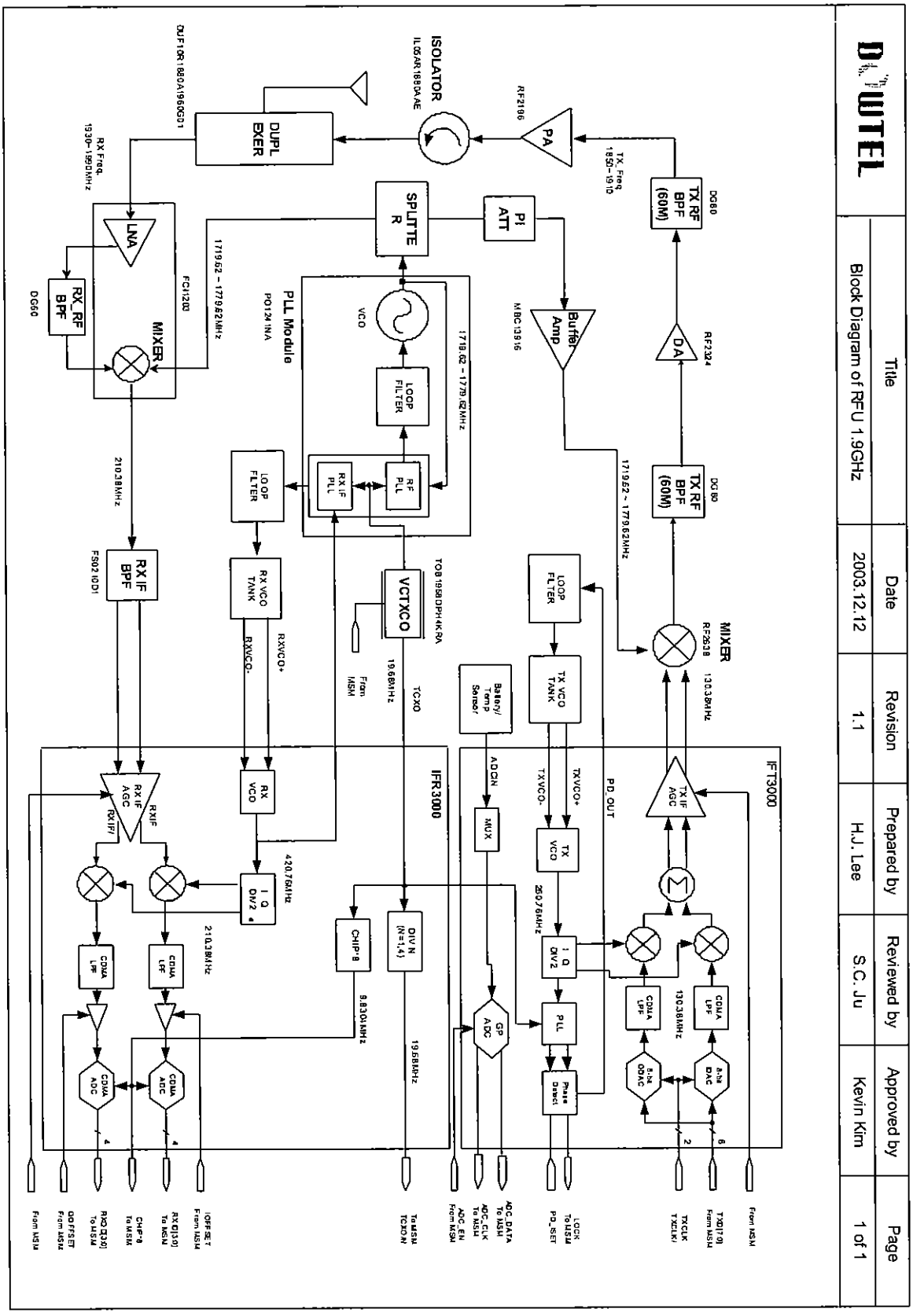
ECS1N/VIDCTL0	96	O	Flash memory chip select or Video Control signal
ECS2N/VIDCTL1	97	O	Flash memory chip select or Video Control signal
PCLK/DMAACK	29	O	Thermal Print Head clock or external DMAACK
PDAT	30	O	Serial printing data
PLAT	31	O	TPH data latch
STRB[3:0]	[33:36]	O	Strobe signals for the TPH
STRBPOL/DMAREQ	37	I	Sets strobe polarity active high/low
OPO[5] / GPO[13]	40	O	Keyboard / LED strobe[5] or GPO[13]
OPO[6] / GPO[14]	39	O	Keyboard / LED strobe[6] or GPO[14]
OPO[7] / GPO[15]	38	O	Keyboard / LED strobe[7] or GPO[15]
OPI[0]/GPIO[21]/SSRXD1	52	I / O	Keyboard return [0] or GPIO[21] or SSRXD1
OPI[1]/GPIO[22]/SSSTAT1	51	I / O	Keyboard return [1] or GPIO[22] or SSSTAT1
OPI[2]/GPIO[23]/SSCLK1	50	I / O	Keyboard return [2] or GPIO[23] or SSCLK1
OPI[3]/GPIO[24]	49	I / O	Keyboard return [3] or GPIO[24]
LEDCTI	55	O	Indicates outputs OPO[7:0] are for LEDS
LCDCS	54	O	LCD chip select
GPIO[0]	94	I / O	GPIO[0]
GPIO[1]/SASTXD	93	I / O	GPIO[1] or SASTXD
GPIO[2]/SASRXD	92	I / O	GPIO[2] or SASRXD
GPIO[3]/SASCLK	91	I / O	GPIO[3] or SASCLK
GPIO[4]/CPCIN	90	I / O	GPIO[4] or Calling Party Control input
GPIO[5]/SSCLK2	89	I / O	GPIO[5] or SSCLK2
GPIO[6]/SSTXD2	87	I / O	GPIO[6] or SSTXD2
GPIO[7]/SSRXD2	86	I / O	GPIO[7] or SSRXD2
GPIO[8]/FWRN	85	I / O	GPIO[8] or flash write enable signal for NAND-type flash memory
GPIO[9]/FRDN	84	I / O	GPIO[9] or flash read enable signal for NAND-type flash memory
GPIO[10]/SSSTAT2	83	I / O	GPIO[10] or SSSTAT2
GPIO[11]/SERINP	82	I / O	GPIO[11] or bus enable or serial port data input for autobaud detection

GPIO[12]/CS[2]N	80	I / O	GPIO[12] or I/O chip select[2]
GPIO[13]/CS[3]N	79	I / O	GPIO[13] or I/O chip select[3]
GPIO[14]/CS[4]N	78	I / O	GPIO[14] or I/O chip select[4]
GPIO[15]/CS[5]N	77	I / O	GPIO[15] or I/O chip select[5]
GPIO[16]/IRQ[8]	76	I / O	GPIO[16] or external interrupt 8
GPIO[17] GPIO[18]/IRQ[9]N	75 74	I / O I / O	GPIO[17] GPIO[18] or external interrupt 9
GPIO[19]/RDY/SEROUT	73	I / O	GPIO[19] or ready signal or Serial port data output for autobaud detection
GPIO[20]/ALTTONE	107	I / O	GPIO[20] or ALTTONE
SM[3:0]/GPO[7:4]	[103:106]	O	Programmable scan motor control pins or GPO pins
PM[3;0]/GPO[3;0]	[115:118]	O	Programmable print motor control pins or GPO pins
TONE	119	O	Tone output signal
-Vref/CLREF	66	I	Negative Reference Voltage for Video A/D or Reference Voltage for the Clamp Circuit
ADXG	68	I	A/D internal GND
ADGA	69		A/D Analog Ground
ADVA	70		A/D Analog Power
ADGD	72		A/D Digital Ground
+Vref	71	I	Positive Reference Voltage for Video A/D
VIN THADI	67 65	I I	Analog Video A/D input Analog Thermal A/D input
VSS(12)	7,21,28,45,53,56,64,88,95,108,132,134		Digital Ground
VDD(8)	14,32,41,48,81,102,123,140		Digital Power
VBAT	63		Battery Power
VDRAM	114		DRAM Battery Power

6. Circuit Description of RF Part

RFU Board consist of RX & TX IF/Baseband processor part(IFR3000 & IFT3000), Trasmitter part which convert the IF signal from IFT3000 to RF signal and amplify the signal, Receiver part which amplify the received RF signal from antenna and transmit to IFR3000 and PLL part which generate the LO frequency.

Figure 1 1900MHz RFU Block Diagram



6.1 RX & TX IF/Baseband Processors (IFR3000 & IFT3000)

6.1.1 IFR3000 (U202)

The IFR3000 spans the intermediate-frequency section and the digital processing circuitry of the telephone.

The IFR3000 is consists of a receive signal path, clock synthesis, buffering circuits, and mode control logic.

The circuit functions of the IFR3000 circuit functions include the RX AGC amplifier with 90dB dynamic range, quadrature IF Mixer and low-pass filters for down-converting IF to analog baseband, and analog-to digital converters (ADC) for converting to digital baseband. The IFR3000 includes clock generators that drive the telephone휠 digital processor and a voltage controlled oscillator (VCO) which generates the local frequency for IF to baseband down-conversions.

Figure 2 shows a functional block diagram of the IFR3000 Rx IF/Baseband Processor.

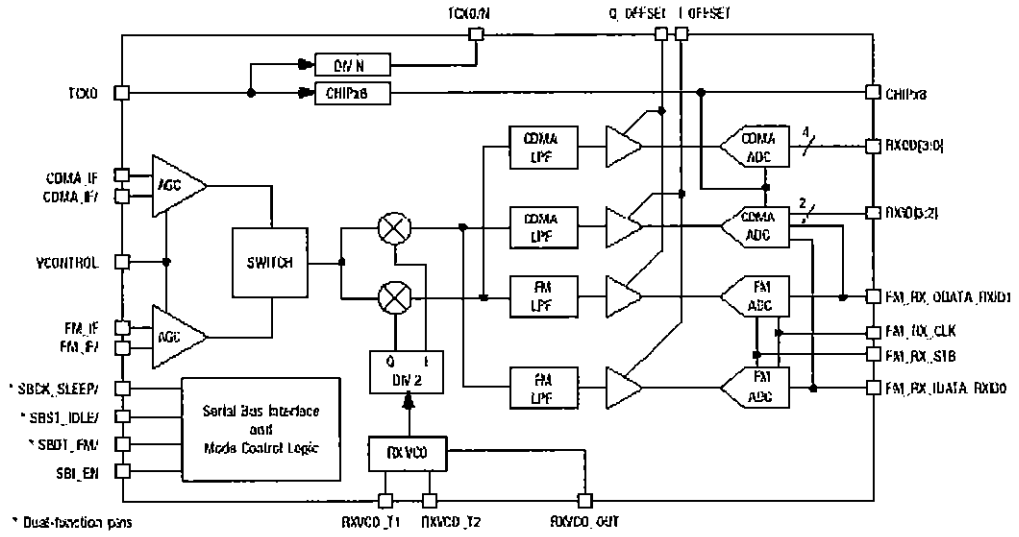
IFR3000 is designed to accept a differential IF signal with CDMA spread spectrum modulation extending □630KHz from the IF center frequency(210.38MHz). The RX AGC Amplifier either amplifies or attenuates the received CDMA IF signal to provide a constantamplitude signal to the I/Q downconverter. The AGC gain is controlled by varying the DC voltage on the Vcontrol pin.

The IF output of the RX AGC amplifier is separated into Ichannel and Q-channel baseband components and downconverted by mixing with quadrature local oscillator signals. Local oscillator signals(210.38MHz) are generated by a voltage controlled oscillator onboard the IFR3000 and frequency stabilized by external varactor-tuned tank circuitry. (L216, C242, C243, C244, D201, D202)

External PLL Module (U302) and Loop filter(R214, R215, C245, C246, C247) supply the feedback control voltage to the varactor for oscillation of internal VCO of IFR3000.

- CDMA A/D conversion (ADC)

CDMA analog I and Q baseband components are converted to digital signals by two identical 4-bit ADCs. The CDMA ADCs output a new 4-bit parallel digital value on each rising edge of the ADC? s synchronous clock input signal, CHIPx8 ADC. The CDMAx8 ADC clock frequency of 9.8304MHz is developed in the IFR3000 by multiplying the 19.68MHz system crystal oscillator frequency by 512/1025. The IFR3000 also allows the use of an external CHIPx8 input signal for use with systems relying on 19.2 and 19.68MHz TCXO reference oscillators.



[Figure 2] Functional Block Diagram of IFR3000

6.1.2 IFT3000 (U101)

The IFT3000 spans the intermediate-frequency section and the digital processing circuitry of the telephone.

The IFR3000 is consists of a receive signal path, clock synthesis, buffering circuits, andmode control logic.

The circuit functions of the IFT3000 include digital-to-analog converters (DAC) for converting digital baseband to analog baseband, low-pass filters and a quadrature IF mixer for up-convert to the IF frequency range and an 84 dB dynamic range Tx AGC amplifier. The IFT3000 includes a fully programmable phase-locked loop (PLL) for generating Tx LO and IF frequencies. The IFT3000 also has an 8-bit general purpose ADC with three selectable inputs for monitoring battery level, RF signal strength and phone temperature. Figure 2 shows a functional block diagram of the IFT3000 Tx IF/Baseband Processor.

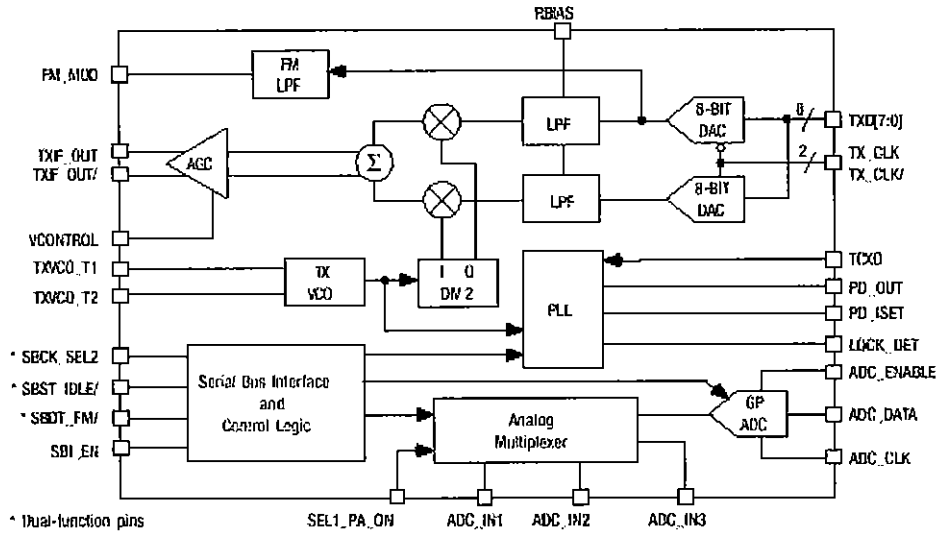
IFT3000 convert the digital I and Q baseband signals which is received signals from MSM5000 to analog I and Q baseband signals. And then analog I and Q baseband signals are mixed in quadrature with the TX IF frequency to generate a modulated waveform centered at TX IF frequency. The IFT3000 includes a programmable TX PLL for synthesizing the TX IF frequency. The TX VCO oscillates at twice the TX IF frequency. Precision quadrature mixing signals at the TX IF frequency are derived from the TX VCO. Local oscillator signals(130.38MHz) are generated by a voltage controlled oscillator onboard the IFT3000 and frequency stabilized by external varactor tuned tank circuitry. (L102, C109, C110, C111, D105, D106)

Internal PLL and external Loop filter(R103, C107, C108) supply the feedback control voltage to the

varactor for oscillation of internal VCO of IFT3000.

This signal is amplified or attenuated at TX AGC amplifier with 84dB gain range. The transmit output power level of subscriber unit is directly controlled by varying the gain of this TX AGC amplifier. A DC input voltage from the MSM3000 linearly controls the gain of the TX AGC amplifier. Differenti al outputs (TXIF_OUT, TXIF_OUT/) are provided by the TX AGC for simple interfacing to down-stream transmit IF circuits.

The IFT3000? s8 -bits GP ADC is normally used to moniter analog functions such as battery voltage, temperature. A three-input analog multiplexer on the IFT3000 allows transducers to be connected to the input of the GP ADC. The conversion time of the GP ADC is programmable and conversion cycles are initiated by the MSM5000.



[Figure 3] Functional Block Diagram of IFT3000

6.2 TX Part

Transmit unit consists of a mixer which converts IF frequencies(130.38MHz) to transmit frequency range(1850 ~ 1910MHz) by receiving IF signals from IFT3000 an amplifier that amplifies the signal output by the mixer, and filters to remove unwanted signals

6.2.1 Up Converter (U102)

The Up-converter(RF2638) mixes 130.38MHz IF frequency and LO frequency to convert them to RF

transmit frequency in 1850 ~ 1910MHz band. This mixer consists of an internal doublebalanced mix and output end buffer amp. The OIP3 of this mixer is 11dBm.typ, and conversion gain is ? 1.5dB.typ
C125 is a coupling capacitor for LO signals input, and C124, C127 are by-pass capacitor. And C128, C129, C130 are by pass capacitor to reduce noise at power end.

6.2.2 RF SAW Filter (FIL101) and Attenuator(R121,R122,R123)

RF SAW Filter (DG80TH) is a band pass filter (BPF) that center frequency is 1880MHz, bandwidth is 60MHz, insertion loss is 3.3dB typical, in-band ripple is 2dB typical, in-band VSWR is 2.0
This eliminates out-of-band spurious signal output by the mixer, and LO component and spurious signals generated during amplification.
C143, L119 provides impedance matching between FIL101 and Attnuator.
π-Attenuator(R121,R122,R123) attenuates RF signals which is received from TX RF filter, for adjust the transmit power level to the Drive amplifier input and impedance matching. And the attenuation value is about 2dB.

6.2.3 Drive Amplifier (U103)

RF2324 is an drive amplifier that gain is 22dB.typ, output 1dB compression point is 14.5dBm.typ, OIP3 is 26dBm.typ, Noise Figure 1.8dB.typ and current consumption is 31mA.
2.8V is supplied to #1 and 3.0V is supplied to #7 C146, C147, C148, C149 are bypass capacitors. C145 provides impedance matching between Attenuator and U103.
L121, C150, C151 are provide impedance matching between U103 and FIL102.

6.2.4 RF SAW Filter (FIL102)

RF SAW Filter (DG80TH) is a band pass filter (BPF) that center frequency is 1880MHz, bandwidth is 60MHz, insertion loss is 3.3dB typical, in-band ripple is 2dB typical, in band VSWR is 2.0.
This eliminates out-of-band spurious signal generated by Drive Amp.

6.2.5 Power Amplifier (U305)

Power amplifier(RF2196) has a typical gain of 27dB and a maximum output of 29dBm. About 3.9V is supplied to VCC (#10) and VCC1 (#11, 12) depending on switching which activates Q501 by control signal of PA_ON.
About 2.85V is supplied to VPD1(#2), VPD2(#4) pass through R119.
PA_ON signal is controlled by MSM.

L123, C158 activates Power Amp between 1850MHz and 1910MHz by parallel resonance structure.
The role of this L124 is to decrease the mutual interference between power end and power module.
C158 make frequency response character generate maximum output power in 1850MHz~ 1910MHz

C153, C154 provide impedance matching between FIL102 output and U305 input.
C165,C166, C167 are used for impedance matching of isolator input end U305 output.
C155, C157, C160, C162, C163, C164 are by pass capacitors for power end noise reduction.

6.2.6 Isolator (U106)

U106(IL05AR1880AAE) is an isolator with an insertion loss of 0.65dB, isolation of 15dB. This is a circuit component, which allows a low loss transmission from, transmits power amplifier output towards the antenna and prohibits transmission of reverse signals by big attenuation.

6.2.7 Duplexer (DPX1)

DPX1(DUF10R1880A1960G01) is a Duplexer. The insertion loss of transmitting end is 3.6dB Max and the insertion loss of receiving end is 4.2dB Max.
The role of this duplexer is to protect the transmitting unit from transmitting output and supply echo signal to receiving unit during reception to share a single antenna for both transmission and reception.

6.3 Receive unit

The receiving unit consists of an amplifying unit to amplify the input RF signal from antenna end , filter to remove spurious signals, a mixer to convert received RF frequency to IF frequency band.

6.3.1 LNA & DOWN CONVERTER (U201 : FCI1203)

6.3.1.1 LNA(Low Noise Amplifier)

LNA is used to recover filter losses and increase the sensitivity of receiver U201 is a low noise amplifier whose gain is 16.5dB.typ, Noise Figure is 1.7dB.typ, IIP3 is 8dBm.typ R202,R206,R205 provides bias voltage. C202,L201, C201 provide impedance matching between duplexer(DPX1) output and LNA(U201 : FCI1203) input. L204, C218 provide impedance matching between I NA output and RX RF SAW filter(FIL201). C203, C204, C208, C209 are RF bypass capacitor.

6.3.1.2 DOWNCONVER

The role of mixer is to conver Input RF signal (1930~1990MHz) to 210.38MHz IF signal. The mixer has an IIP3 of +5dBm .typ and a conversion gain of 13dB.typ, Noise Figure 6.5dB.typ

Pin nubmer 12 of FC1203(U201) is LO input pin, Pin number 21 is RF signal input pin, and Pin number 14 & 15 are IF output pin.

L202,C206,C207 provide impedance matching between mixer input and RF SAW Filter

6.3.2 RF SAW Filter (FIL201)

FIl 201(DG60GH) is a band pass filter (BPF) whose center frequency is 1960MHz, Bandwidth is 60MHz, insertion loss is 2.8Db typ, in-band ripple is 1.5dB typ, in-band Return Loss is 10dB typ.

This eliminates out-of-band spurious signal and spurious signals generated during amplification.

6.3.3 RX IF SAW Filter (FIL202)

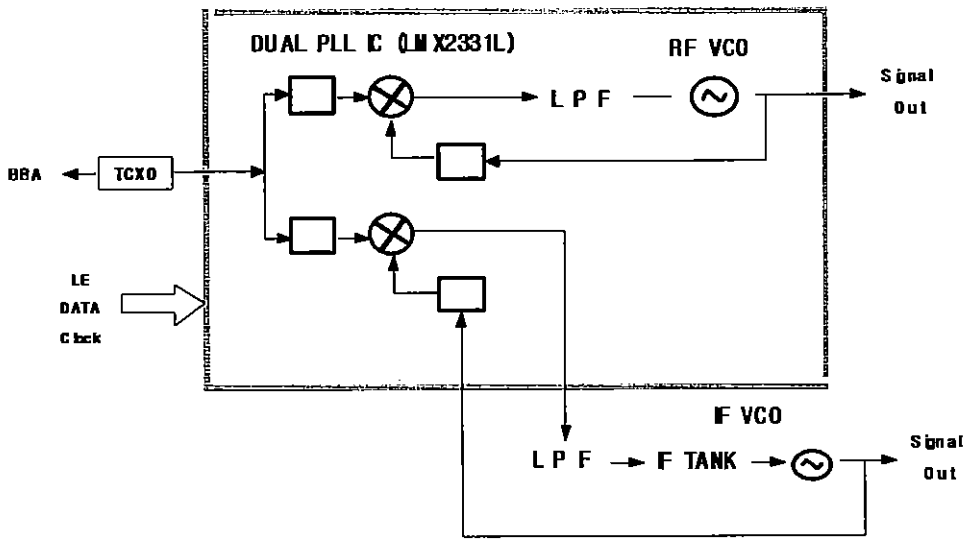
FIL202(FS0210D1) is a IF SAW Filter. The center frequency of this filter is 210.38MHz and it has an insertion loss of 10.5dB max. It eliminates unwanted signals from the mixer output. The impedance interface between filter output and IFR3000 input is adjusted using L213, C241, C239, C240, and R210.

6.4 PLL (Phase Lock Look)

This terminal is designed to operate on 1200 channels of US PCS frequency range. The transmitting frequency range is 1850 MHz ~ 1910 MHz, where as the receiving frequency range is 1930 MHz ~ 1990 MHz.

The IF frequency oscillation of the terminal are managed by IFR3000 and IFT3000, and LO frequency by a PLL module are shared in transmission and reception. The frequencies generated by each oscillation end of this terminal are as follows:

- TX IF LO : 260.76MHz
- RX IF LO : 420.76MHz
- RF LO : 1719.62 MHz~1779.57 MHz



[Figure 4] Block diagram of PLL module

6.4.1 PLL Module(U302)

U302(PO1241NA) is a PLL Module. The PLL module consists of PLL IC(LMX2331L), VCO, Loop filter and Buffer Amp. If the reference frequency of 19.68MHz is input to pin number 12, it generates and amplifies the LO frequency according to PLL_CLK, PLL_EN, PLL_DATA signal. And then, it send the LO frequency to the discrite splitter.

Figure 4 shows the block diagram of PLL module which is included PLL IC.

6.4.2 Loop Filter(R214,R215,C245,C246,C247)

The error voltage output from PLL module pin number 2 goes through the loop filter(R214, R215,C245,C246,C247) and VCO tank circuit and then get to input of the RXVCO pin (#21, #22) of IFR3000. Loop filter eliminates noises generated during the phase comparison in frequency synthesizer.

6.4.3 LO buffer Amplifier (Q301)

Q301(MBC13916) is an amplifier whose gain is 10Db.typ, noise figure is 1.9dB.typ, OIP3 is 17dBm.typ. This circuit transfers the frequency which is oscillated by PLL module, to mixer(Upconverter). L303, C318 are used for impedance matching of AMP input. C319, C322 are bypass capacitors.

6.4.4 Discrite Splitter (L307,L308,C323,C324,C325,R308)

This part is a discrite power divider that splits the input signal into 2 signals. Each insertion loss is about 3dB. The split signals are used as local frequency of downconverter and Upconverter

6.4.5 VCTCXO (U301)

U301(TOB1968DPH4KRA) provides reference frequencies. This terminal is designed for MSM to control the oscillation frequency. MSM can control the oscillation frequency by modifying TRK LO ADJ voltage. R313,C305,C306 are low pass filters that eliminates noise in the control voltage coming from MSM and supply it to the oscillation control end of VCTCXO.

C301~ C304, L301 are usedfor noise elimination in power supply. R315 is used for reduce the voltage. The oscillated frequency is output through pin number 3, and supplied as base frequency to PLL Module and IFT3000.

6.5 Other circuits

6.5.1 Regulator (U501, U503, U504)

RFU includes 3 regulators. U504 supplies a voltage of 3.0V to IFT3000, IFR3000, VCTCXO according to the control signal of RFU_PWR. U501 supplies a voltage of 3.0 V to TX Part according to the control signal of IDLE/. U503 supplies a voltage of 3.3V to PLL and RX part according to the control signal of SLEEP/.

The input voltage of these regulators is a 3.8V(VDC) supplied from the logic board through a 52pin connector.

6.5.2 Load Switch (Q501)

U305(FDC6329L) is a load switch. During CDMA transmit, if ? PA ON ? is ? High? then the internal transistor of Q501 is turned on. At this time 3.8Vdc power (VDC) is input to the Power Amplifier for amplify the CDMA transmit power.

Figure 5 shows the internal block diagram of Load Switch

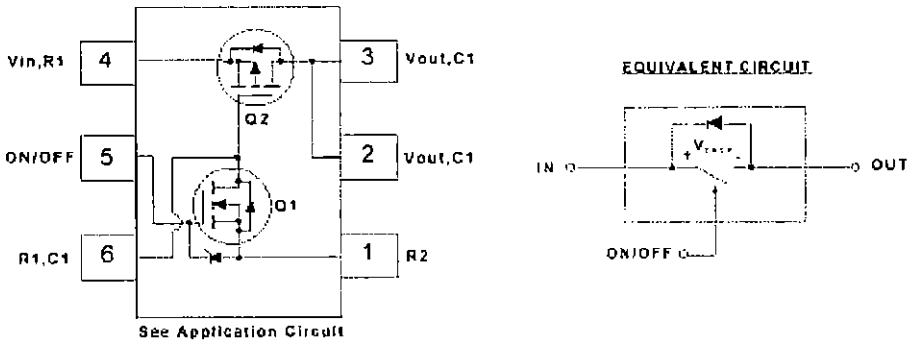


Fig. 5 Internal block diagram of Load Switch

6.5.3 Temperature & Battery Voltage Sensing(U502 & R505,R506,C510)

This terminal senses the temperature and compensates for output changes due to temperature. It is designed to monitor the battery current and stop operation when it drops to below the operation current. This circuit supplies a current depending on the temperature and battery charge to MSM so it can monitor the temperature and battery charge of RFU board.

U502(S8120AMP) is a temperature sensor which outputs 1.823V at ? 30℃, 1.326V at +30℃ and 0.718V at +100℃. Its linear output voltage is ? 8.5mV/℃.

The output of U101 is supplied to the ADC input pin of IFT3000

Figure 6 shows the internal block diagram of temperature sensor

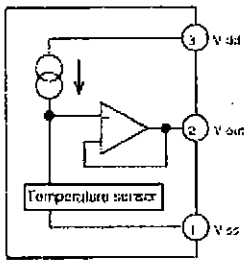


Fig. 6 Internal block diagram of temperature sensor

R505 and R506 are used to split the battery sensing voltage, C510 is used to reduce the Noise.