

# BM620

## Bluetooth Class 2 Stereo Audio Module

### 1. Module Features

- Bluetooth™ V1.2 Compliant
- Dual UART Port
- 16-bit Stereo Audio CODEC



### 2. Specification

- Operating Conditions
  - Supply Voltage: VDD: 2.4V ~3.6V
  - Temperature Range: -20~+70°C
- Radio Characteristics
  - Receiver Sensitivity: -80dBm (Typical)
  - Transmitter Power: +2dBm (Typical)

### 3. Applications

- Stereo Headphones
- Echo cancellation
- Automotive hands free kits
- High Performance Telephony Personal
- Enhanced Audio Applications

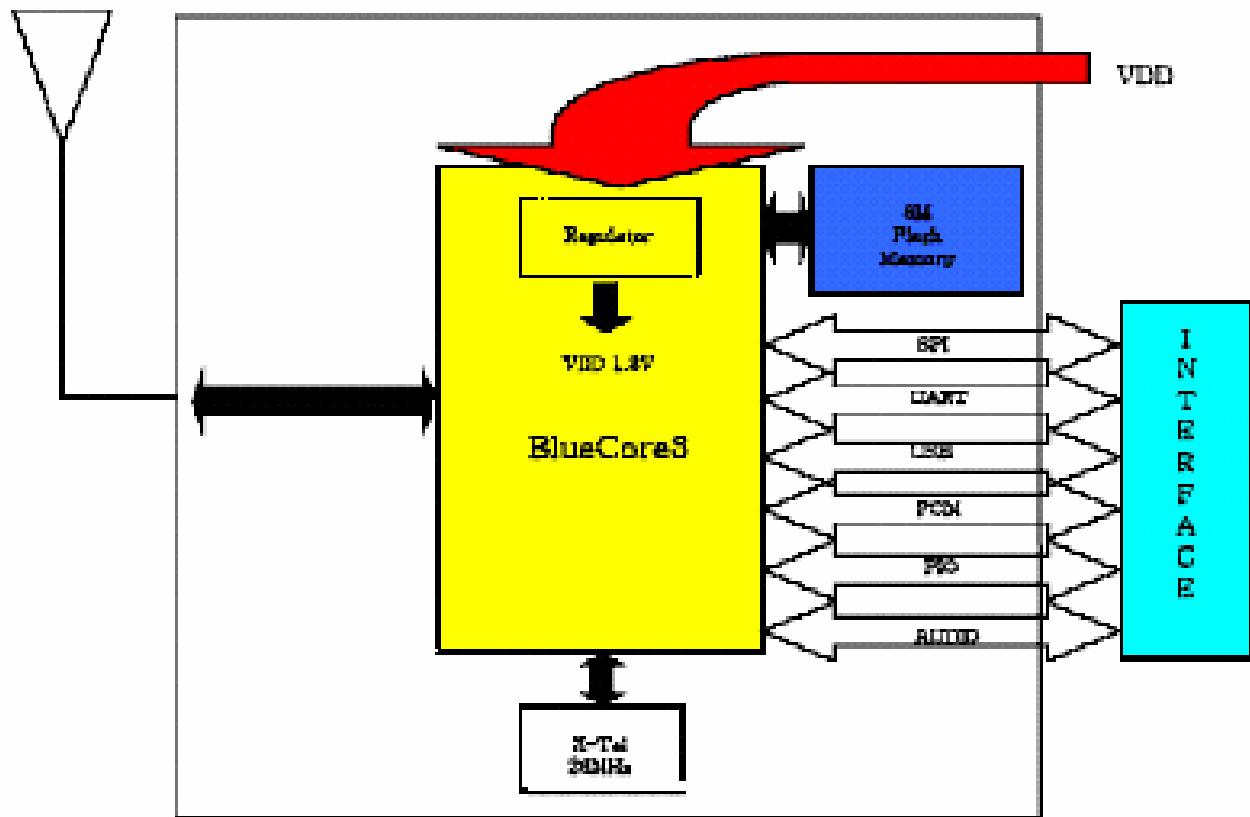
### 4. Features

- Size(12 x 14 x 2.5 mm)
- Surface Mountable
- Support PCM interface for SCO
- 16bit stereo Audio Codec

### 5. Descriptions

The BM620 is Class 2 Bluetooth Stereo Audio Module for PHONE, PDA, PC and MP3 Player, Home Theater applications. It is designed to be used as a universal Bluetooth Module of Bluetooth specification version 1.2 which can be deployed to implement versatile wireless applications such as voice communications.

## 6. Block Diagram



## 7. Electrical Characteristics

Absolute Maximum Ratings			
Parameter	Min	Max	Unit
Temperature	-40	+85	°C
Supply Voltage(V_PA)	3.2	3.4	DCV
Supply Voltage (VDD,V_DIG,V_FL,V_IN,V_OUT)	2.4	3.6	DCV
Recommended Operating Conditions			
Parameter	Min	Max	Unit
Temperature	-20	+70	°C
Supply Voltage(V_PA)	3.3		DCV
Supply Voltage (VDD,V_DIG,V_FL,V_IN,V_OUT)	2.6	3.3	DCV

## 8. RF Specification

Transmitter Performance					
Parameter	Condition	Min	Typ.	Max	Unit
Output Power	Normal/extreme test	-	3	-	dBm
Power Density	Normal/extreme test	-	-	4	dBm
Power Control	Normal/extreme test	2dB ≤ Step size ≥ 8dB			
Frequency Range	Normal/extreme test	2400	-	2483.5	MHz
20dB Bandwidth	Normal/extreme test	-	850	1000	KHz
Adjacent Characteristics	±2MHz	-	-	-20	dBm
	±3MHz	-	-	-40	dBm
	±4MHz	-	-	-40	dBm
Modulation Characteristics	ΔF1avg	140		175	KHz
	ΔF2 max	115			KHz
	ΔF2 avg / ΔF1max			80	%
Initial Carrier Frequency Tolerance		-75		75	KHz
Carrier Frequency Drift	One slot packet(DH1)	-25		25	KHz
	Three slot packet(DH3)	-40		40	KHz
	Five slot packet(DH5)	-40		40	KHz
Transceiver Performance					
Parameter	Condition	Min	Typ.	Max	Unit
Out-of-Band Spurious Emissions	30MHz ~ 1MHz	-	-	-36	dBm
	1GHz ~ 12.75GHz	-	-	-30	dBm
	1.8GHz ~ 5.3GHz	-	-	-47	dBm
	5.1GHz ~ 5.3GHz	-	-	-47	dBm
Receiver Performance					
Parameter	Condition	Min	Typ.	Max	Unit
Sensitivity level	Single slot packets	-	-80	-	dBm
	Multi slot packets	-	-79	-	dBm
C/I performance	C/I co-channel	-	-	11	dB
	C/I 1MHz(Adjacent channel selectivity)	-	-	0	dB
	C/I 2MHz(Adjacent channel selectivity)	-	-	-30	dB
	C/I ≥3MHz(Adjacent channel selectivity)	-	-	-40	dB
Blocking performance	30MHz ~ 2000MHz	-10			dBm
	2000MHz ~ 2400MHz	-27			dBm
	2500MHz ~ 3000MHz	-27			dBm
	3000MHz ~ 12.75MHz	-10			dBm
Inter-modulation Performance	N=5	-39	-		dBm
Maximum Input Level		-20	-10		dBm

## 9. Pin Description & Package Outline

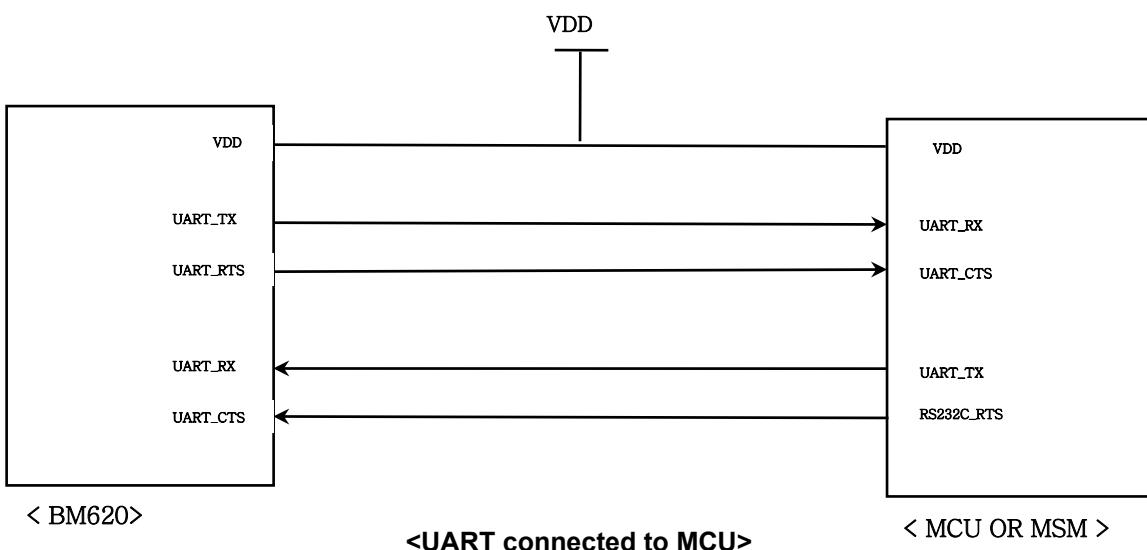
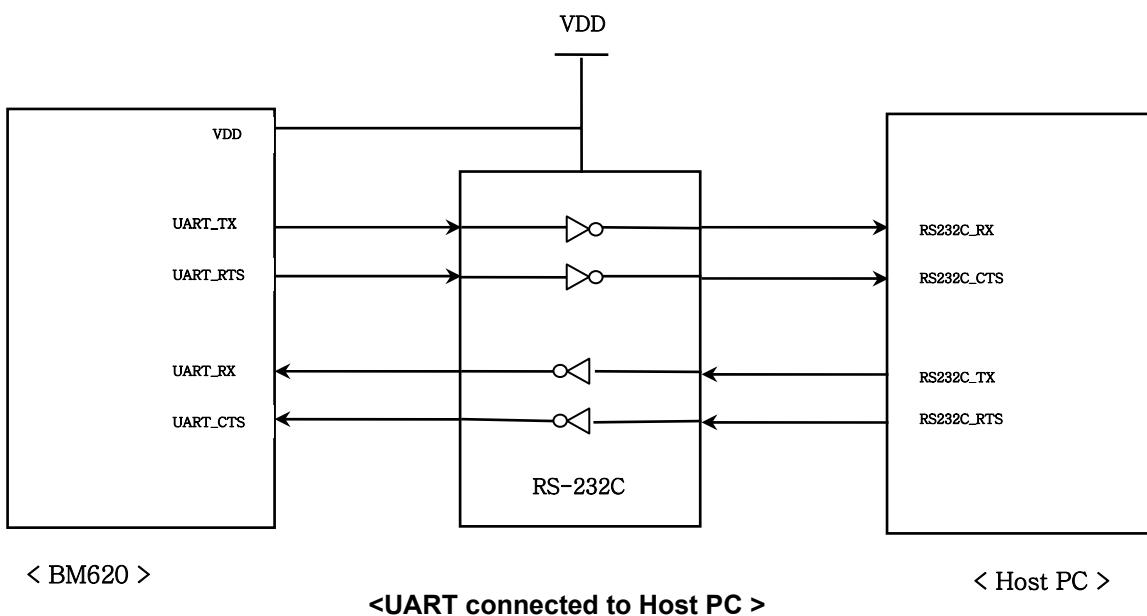
Pin No.	Pin Name	Description
1	GND	Common Ground
2	ANT	Connect to Antenna (RF Signal)
3	GND	Common Ground
4	AUDIO_OUT_P_R	Speaker output positive (Right channel)
5	AUDIO_OUT_N_R	Speaker output negative (Right channel)
6	AUDIO_OUT_P_L	Speaker output positive (Left channel)
7	AUDIO_OUT_N_L	Speaker output negative (Left channel)
8	AUDIO_IN_N_L	Microphone & Audio Signal input negative (Left channel)
9	AUDIO_IN_P_L	Microphone & Audio Signal input positive (Left channel)
10	AUDIO_IN_P_R	Microphone & Audio Signal input positive (Right channel)
11	AUDIO_IN_N_R	Microphone & Audio Signal input negative (Right channel)
12	AIO_0	Programmable input/output line
13	GND	Common Ground
14	AIO_1	Programmable input/output line
15	AIO_3	Programmable input/output line
16	PIO_6	Programmable input/output line
17	PIO_7	Programmable input/output line
18	PIO_5	Programmable input/output line
19	PIO_4	Programmable input/output line
20	USB_DN	USB data minus
21	USB_DP	USB data plus
22	VDD_IN	VDD_IN
23	GND	Common Ground
24	UART_RTS	UART request to send active low
25	UART_CTS	UART clear to send active low
26	UART_TX	UART TX Data
27	UART_RX	UART RX Data
28	PCM_IN	Pulse Code Modulation Synchronous data input
29	PCM_CLK	Pulse Code Modulation Synchronous data clock
30	PCM_SYNC	Pulse Code Modulation Synchronous data sync
31	PCM_OUT	Pulse Code Modulation Synchronous data output
32	RESET	Reset if high. must be high for >5ms to cause a reset
33	SPI_MOSI	Serial Peripheral Interface data input
34	SPI_CLK	Serial Peripheral Interface data clock
35	SPI_MISO	Serial Peripheral Interface data output
36	SPI_CS <sub>B</sub>	Chip select for Synchronous Serial Interface active low
37	PIO_0	Programmable input/output line
38	PIO_1	Programmable input/output line
39	PIO_11	Programmable input/output line
40	PIO_9	Programmable input/output line
41	PIO_10	Programmable input/output line
42	PIO_8	Programmable input/output line
43	PIO_2	Programmable input/output line
44	PIO_3	Programmable input/output line
45	AUX_DAC	Voltage DAC Output
46	GND	Common Ground

## 10. UART Interface

BM620 is Universal Asynchronous Receiver Transmitter(UART) interface provides a simple mechanism for communicating with other serial device using the RS232 standard.

When BM620 is connected to another digital device, UART\_RX and UART\_TX transfer data between the two device. The remaining two signal, UART\_CTS, UART\_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

All UART connections are implemented using CMOS technology and have signaling levels of 0V and VDD.

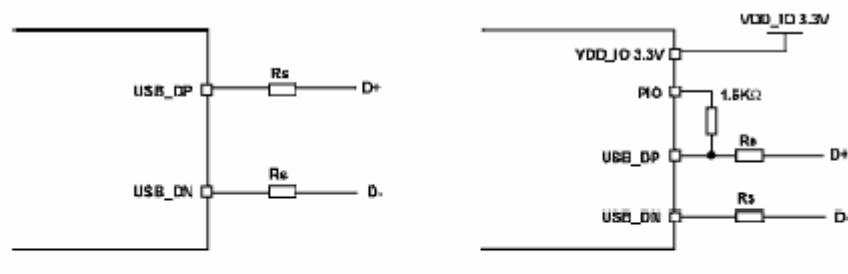


## 11. USB Interface

BM620 USB devices contain a full speed(12Mbit/s) USB interface that is capable of driving of a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC, Both the OHCI and UHCI standards supported. The set of the USB endpoints implemented behave as specification V1.2.

As USB is Master/Slave oriented system) in common with other USB peripherals), BM620 only supports USB slave operation.

BM620 features an internal USB pull-up resistor. This pulls the USB+ pin weakly high when BM620 is ready to enumerate. It signal to the PC that it is a full Speed(12Mbit/s) USB device.



<USB Connections for BUS Power Mode>      <USB Connections for Self Power Mode>

Identifier	Value	Function
Rs	27 nominal	Impedance matching to USB cable

## 12. Audio Interface

The audio interface circuit consists of a stereo audio CODEC, dual audio inputs and outputs, and a PCM, I2S or SPDIF configurable interface. V1.2.

The CODEC supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the CODEC each contain two independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

PCM Interface	SPDIF Interface	I <sup>2</sup> S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

<Alternative Functions of the Digital Audio Bus Interface On the PCM Interface>

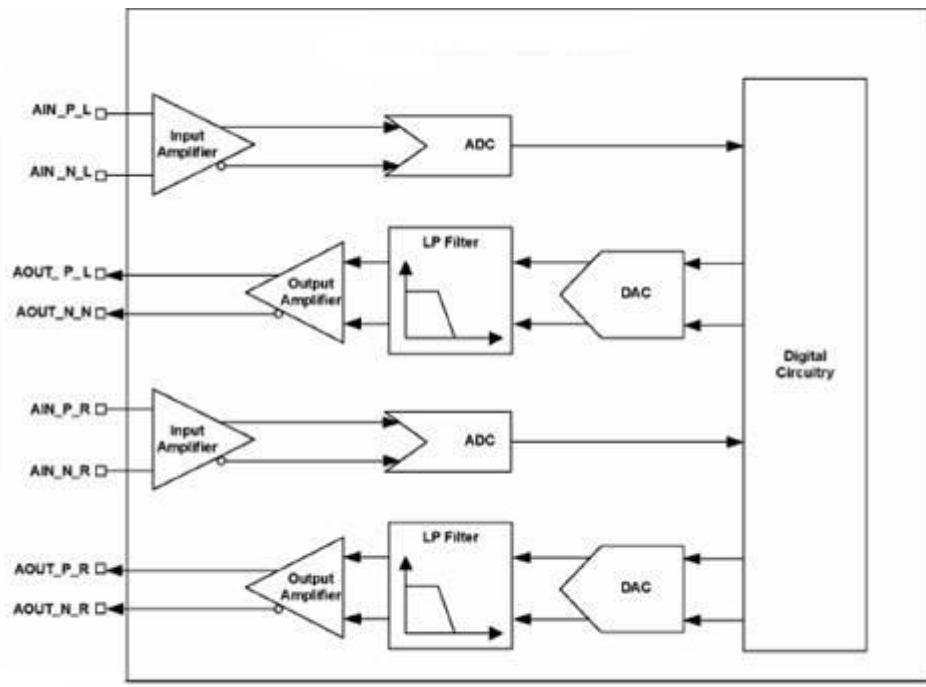
The audio input circuitry consists of a dual audio input that can be configured to be either single ended or fully differential and programmed for either microphone or line input. It has a programmable gain stage for optimization of different microphones.

The digital audio bus supports various digital audio bus standard, which include I2S, and the interfaces contained within the IEC 60958 specification such as SPDIF and AES3.

### 13.1 Stereo Audio Interface

The main features of the interface are:

- 16-bit resolution, standard, sample rates of 8KHz, 11.025KHz, 16KHz, 22.05KHz, 32KHz, 44.1KHz and 48KHz(DAC only)
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving microphone and speakers with minimum external components
- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I2S
- Support for IEC-60958 standard stereo digital audio bus standards i.e. S/PDIF and AES3/EBU
- Support for PCM interfaces including PCM master CODECs that require an external system clock



The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.8V and uses a minimum of external components.

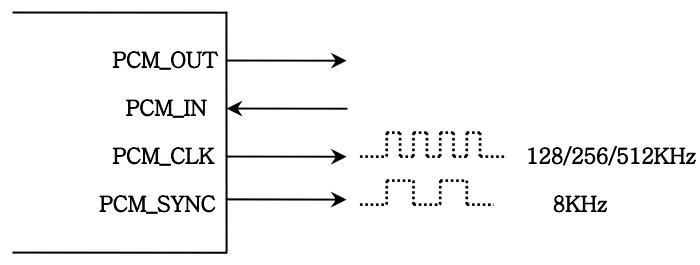
## 13.2 PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitize human voice patterns for transmission over digital communication channel. Through its PCM interface, BM620 has hardware support for continual transmission reception of PCM data, thus reducing processor overhead for wireless application. BM620 offer a bi-directional digital audio interface that routes directly into the baseband layer of the Module firmware. It does not pass through the HCI protocol layer.

Hardware on BM620 allows the data to be sent to the received from a SCO connection.

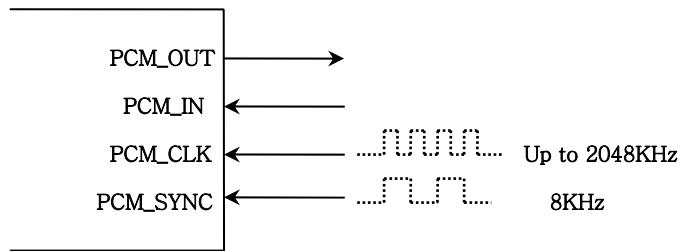
BM620 can be configured as PCM interface Master generating an output clock of 128, 256, or 512KHz. When configured as PCM interface slave it can operated with input clock up to 2048KHz. BM620 is compatible with a variety of clock formats, including Long Frame Sync, Short Frame sync and GCI timing environments.

It supports 13-bit or 16-bit liner, 8-bit u-law or A-law companied sample formats at 8K samples/s. And can receive and transmit on any selection of the first four slots following PCM\_SYNC.



< BM620 >

< BM620 as PCM Interface Master >



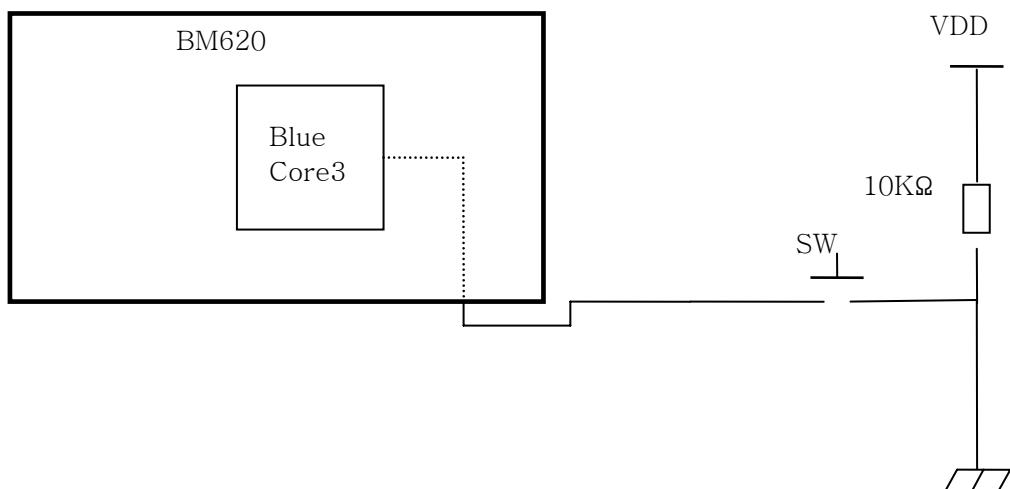
< BM620 >

< BM620 as PCM Interface Slave >

## 14. RESET

BM620 may be reset from several source : RESET pin, power on reset, a UART break character or via a software configured watchdog timer.

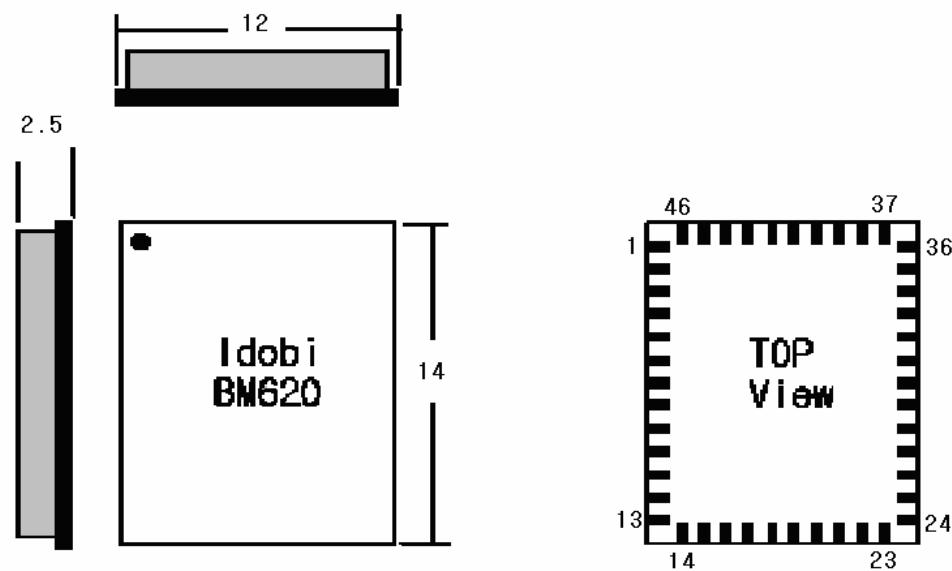
The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET is applied for a period greater than 5ms.



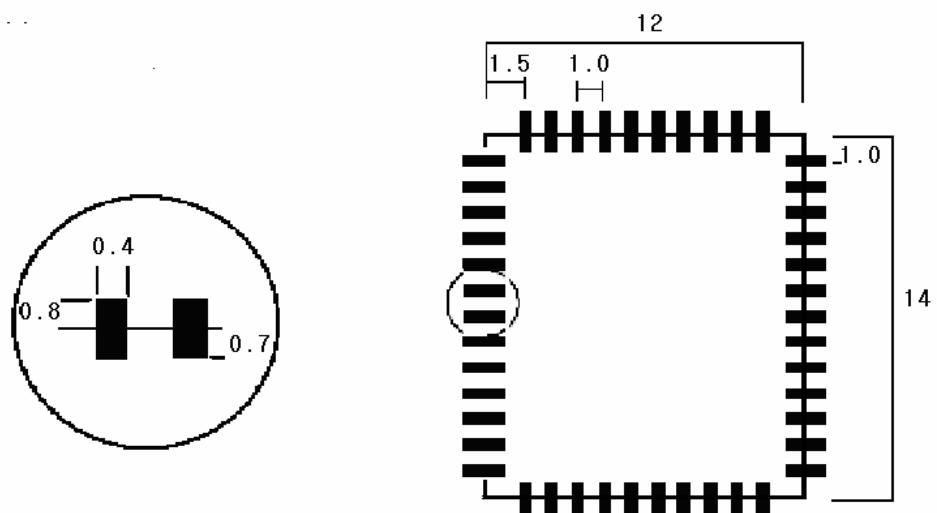
**< BM620 Manual Reset >**

## 15. Dimension

\*Unit : mm



Module Size & Pin Number



PCB Layout (Top View)