# 3. Theory of operation.

## 3.1 Receive path.

Signals received at the antenna are passed to a low noise pre-amplifier and lumped elements filter block via antenna switch composed of L509, L511, L512, L513, D502, D503 and matched capacitors. The antenna switch provides 25dB of isolation between receive path and transmit path with 0.8dB loss on receive path.

The low noise amplifier(LNA) consist of L101, L102, L103, L104, L105, L106, Q101 and matched capacitors, resistors provides approximately 14dB gain at a noise figure of 5.0dB. Also the LNA attenuate unwanted signals such as 1st IF image and 1st down converter local signal by 70dB.

Following the LNA stage, the signal is routed to 1st down converter composed of Q102 and matched R, L, C circuit which provides additional receiver gain and the first down conversion function. The 1st down converter down convert the received and amplified signals from 450 ~ 470Mhz on to 45Mhz of 1st IF signal with 1st local signal that synthesized by PLL circuitry which is 45Mhz lower than receiving signal.

The 1st IF signal is taken to 2 pole 45Mhz monolithic crystal filter to attenuate adjacent signals and 2nd IF image signal by 70dB. The 45Mhz 1st IF filter has 15Khz of 3dB pass band characteristic and 70dB attenuation at 910Khz away from it's center frequency. The filtered 1st IF signal is fed to Q102 1st IF amplifier and amplified by 18dB than fed to U101 FM IF IC.

U101 FM IF IC down converts 1st IF signal on to 455Khz of 2nd IF signal with 20dB of gain utilize Y101 44.545Mhz crystal and internal oscillation circuit than the signal passes through either 2nd IF filter F102 for 8.5Khz bandwidth or F105 for16Khz bandwidth depend on programmed bandwidth. The signal passes through 2nd IF filter is than amplified and limited again and FM demodulated at U101.
R122, D104, Q104 damp the FM demodulated upon programming to adjust sensitivity of the FM demodulation circuit when a signal with 8.5Khz bandwidth has to be demodulated.

Overall frequency stability of receiver circuit is tied on the 1st local oscillator signal from PLL circuit which has +-2.5PPM over -30°C and +60°C of operating temperature range.

## 3.2 Transmit path

Audio Amplifier : Audio signals fed into J102 DB-9 female connector terminal #4 is amplified 26dB and amplitude limited at 4Volts peak to peak with U102A OP amplifier than selectively attenuated by U201, U202 analog switches for support 8.5Khz and 16Khz occupied transmit bandwidth depending on program. The limited audio signal is taken to RV201 for FM deviation adjustment and passes through U203B 3Khz Low Pass Filter(LPF) for attenuate harmonics of the limited audio signals and an audio frequency higher than 3Khz.

The 3Khz LPF is capable to attenuate more than 19dB/Oct. at above 3Khz so that transmit occupied bandwidth can be maintained.

Transmit RF signal : The transmit RF signal is generated by PLL system composed of Q602, Q603 voltage controlled oscillator(VCO), U401 Phase Locked Loop(PLL) IC and TCXO1A Temperature Controlled Crystal Oscillator(TCXO)
The generated transmit RF signal by the PLL system is taken to Q501 buffer amplifier for better stability when turn on the transmit circuits. The buffered transmit signal is amplified by 14dB with Q503 pre-drive amplifier and than amplified again with Q504 drive amplifier to actuate Q506 power amplifier.
A 2Watts of output power from output of Q506 is fed into R/Tx antenna switch circuit composed of L509, L510, L511, L512, L513, D502, D503 and matched R,C, components to feed transmit power to antenna port without loosing the power to receiver circuit(receiver LNA). One other function of the R/Tx antenna switch is to attenuate transmit spurious such as harmonics more than 40dB for transmit signal harmonics.

Frequency stability of the transmit circuit is maintained by TCXO1A TCXO and U401 PLL IC by +-2.5PPM over -30°C and +60°C and output transmit power is maintained by an Automatic Power Control circuit(APC) which composed of D504 power sampler, Q507, Q508 power comparator and Q509, Q510, Q511 power controller and power enabler.

3.3 PLL(Phase Locked Loop)

PLL system is composed of following three sub part.
TCXO : The TCXO generate 12.8Mhz of clipped sine wave with +-2.5PPM over -30°C and +60°C of frequency stability. TCXO1A is also capable of accept modulation signals through its terminal #1 for low frequency FM modulation.

PLL IC : U401 PLL IC divide 12.8Mhz of reference signal from TCXO1A in to either 12.5Khz or 10Khz depending on programming and also divide VCO signal to same 12.5Khz or 10Khz to compare with.
Frequency division ratio for VCO signal is programmed by U402 microprocessor and U402 EEPROM.

VCO : The VCO oscillate transmit frequency when the radio is in transmit mode and oscillate 45Mhz below transmit frequency the radio is in receive mode and the oscillate frequency is precisely monitored and controlled by U401 PLL IC.