Technical Description

The Equipment Under Test (EUT) is a 2.4GHz Pure Transmitting Controller for RC Robot operated at 2415-2465MHz with 1MHz Channel Spacing. The EUT is powered by 3 X 1.5V AAA batteries. After switch on the EUT and paired with RC Robot, the RC Robot can be controlled to move forward, backward, turn right/left by the controller. For the Infrared portion, it is for follow me function.

The brief circuit description is listed as below:

1) **U24 acts as MCU (GPCE2P064A_DIES).**
2) **X1 is 32.768kHz crystal oscillator providing clock for U24.**
3) **U2 acts as 2.4GHz RF Module Circuit (ITR245L).**
4) **Y1 is 16MHz crystal oscillator providing clock for U2.**
5) **U4 acts as Voltage Regulator (G5125).**
6) **U3 acts as Voltage Regulator (LC1218C 3.3V).**

Antenna Type: Internal antenna
Antenna Gain: 0dBi
Nominal rated field strength: 91.8dBμV/m at 3m
Maximum allowed field strength of production tolerance: +/- 3dB

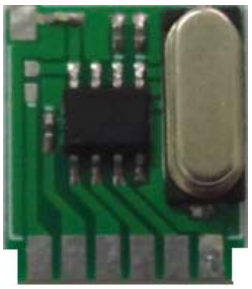
ITR245L

Low Power High Performance 2.4 GHz GFSK Transceiver

Features

- 2400-2483.5 MHz ISM band operation
- Support 250kbps,1Mbps and 2 Mbps air data rate
- Programmable output power
- Low power consumption
- Tolerate +/- 60ppm 16 MHz crystal
- Variable payload length from 1 to 32bytes
- Automatic packet processing
- 6 data pipes for 1:6 star networks
- 2.3V to 3.6V power supply
- 3-pin SPI interface with maximum 6 MHz clock rate
- Compact size

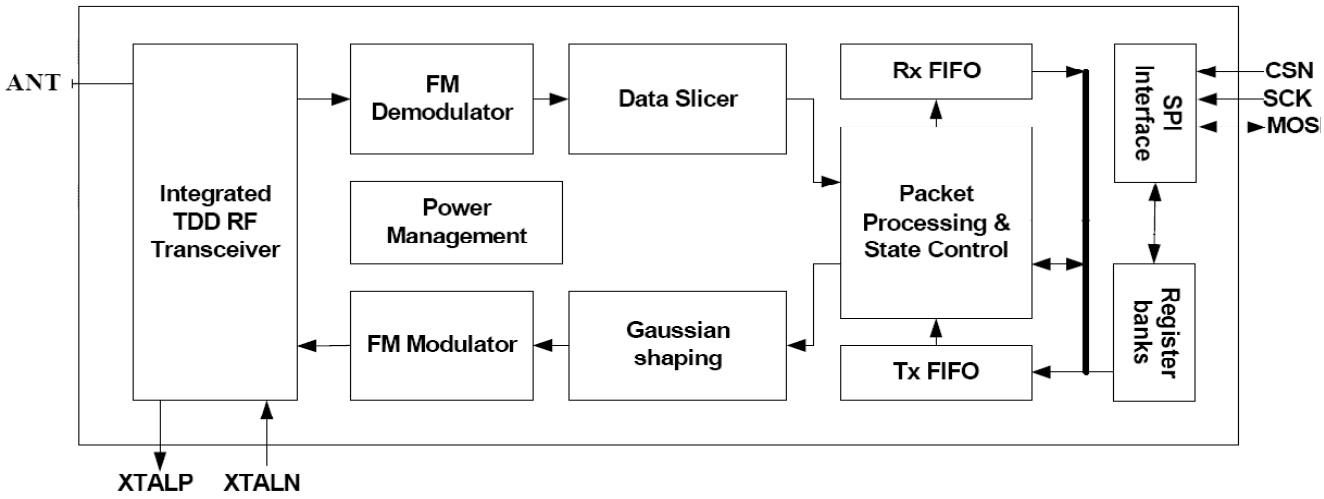
Pin Assignments



Applications

- Wireless PC peripherals
- Wireless mice and keyboards
- Wireless gamepads
- Wireless audio
- VOIP and wireless headsets

Block Diagram



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2 Abbreviations

ACK	Acknowledgement
ARC	Auto Retransmission Count
ARD	Auto Retransmission Delay
CD	Carrier Detection
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select Not
DPL	Dynamic Payload Length
FIFO	First-In-First-Out
GFSK	Gaussian Frequency Shift Keying
GHz	Gigahertz
LNA	Low Noise Amplifier
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
MAX_RT	Maximum Retransmit
Mbps	Megabit per second
MCU	Microcontroller Unit
MHz	Megahertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
PA	Power Amplifier
PID	Packet Identity Bits
PLD	Payload
PRX	Primary RX
PTX	Primary TX
PWD_DWN	Power Down
PWD_UP	Power Up
RF_CH	Radio Frequency Channel
RSSI	Received Signal Strength Indicator
RX	Receive
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
TX	Transmit
TX_DS	Transmit Data Sent
XTAL	Crystal

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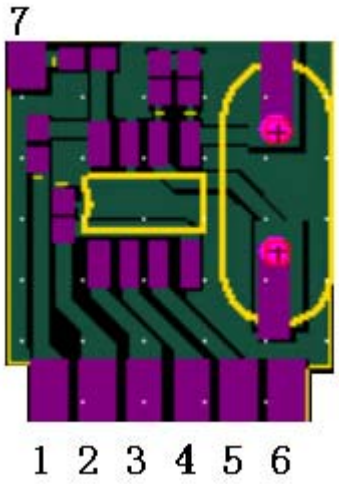
3 Pin Information



PIN	Name	Pin Function	Description
1	ANT_I	Antenna	Antenna connect to main PCB
2	VDD	Power	Power
3	I	CSN	Chip select signal
4	I	SCK	SPI clock
5	I/O	DATA	Data in/out
6	GND	GND	System ground
7	ANT	Antenna	Connect to external antenna

Table 1 ITR245L pin functions

4 State Control

4.1 State Control Diagram

- Pin signal: VDD, CE
- SPI register: PWR_UP, PRIM_RX, EN_AA, NO_ACK, ARC, ARD
- System information: Time out, ACK received, ARD elapsed, ARC_CNT, TX FIFO empty, ACK packet transmitted, Packet received

ITR245RC has built-in state machines control the state transition between different modes.

When auto acknowledge feature is disabled, state transition will be fully controlled by MCU.

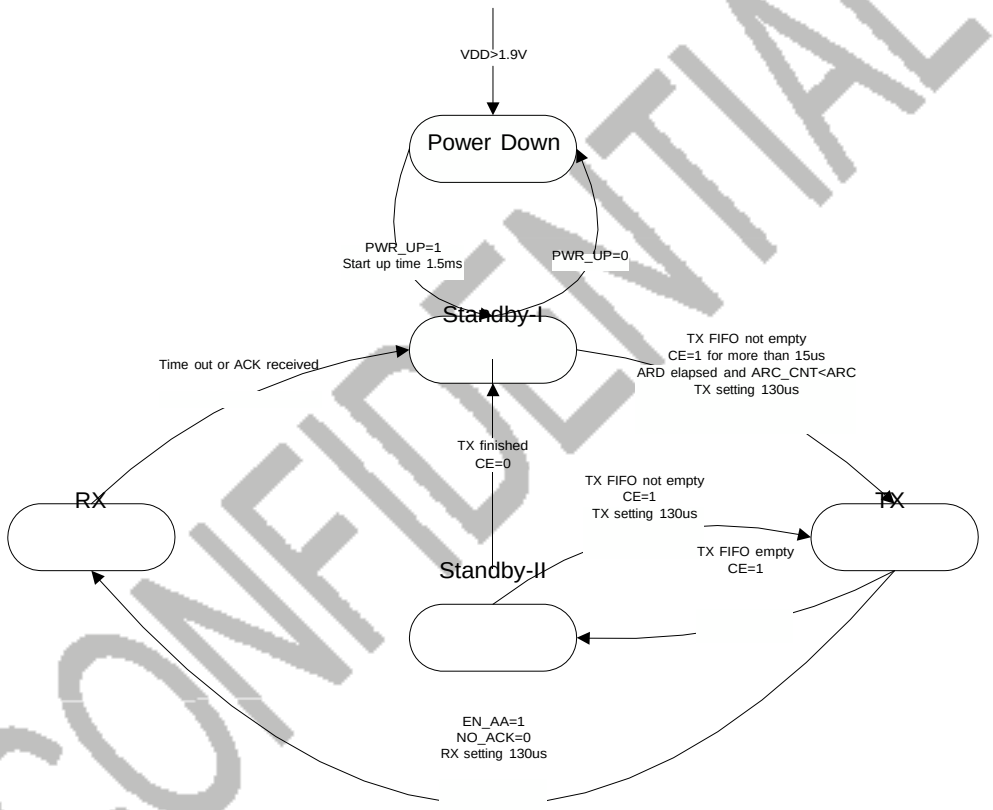


Figure 3 PTX (PRIM_RX=0) state control diagram

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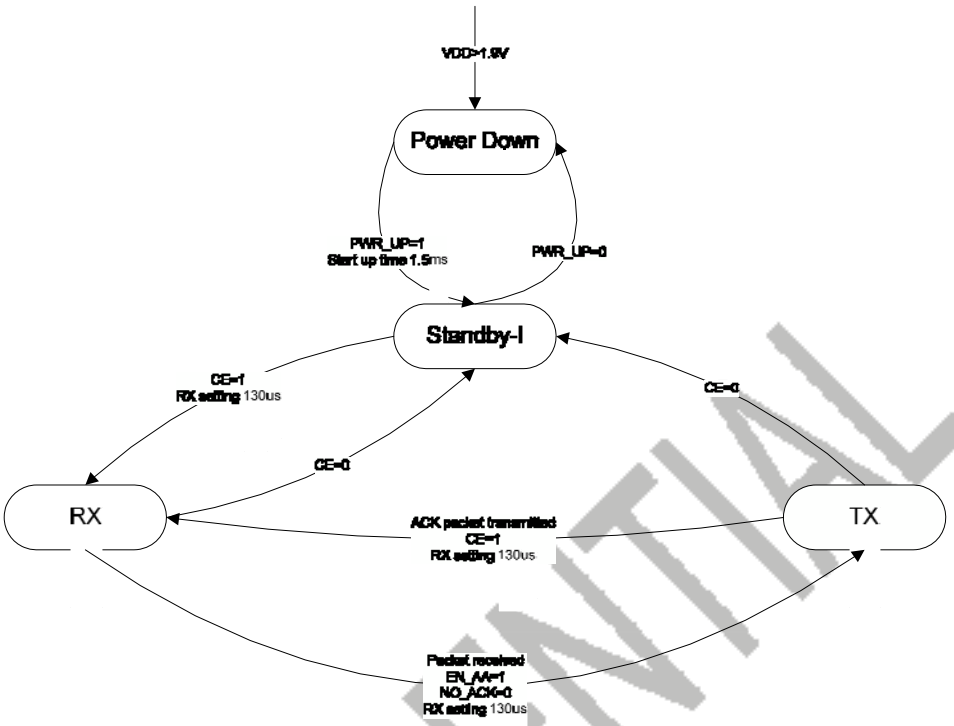

Figure 4 PRX (PRIM_RX=1) state control diagram

4.2 Power Down Mode

In power down mode ITR245RC is in sleep mode with minimal current consumption. SPI interface is still active in this mode, and all register values are available by SPI.
Power down mode is entered by setting the PWR_UP bit in the CONFIG register to low.

4.3 Standby-I Mode

By setting the PWR_UP bit in the CONFIG register to 1 and de-asserting CE to 0, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start-up time. In this mode, part of the crystal oscillator is active. This is also the mode which the ITR245RC3 returns to from TX or RX mode when
CE is set low.

4.4 Standby-II Mode

In standby-II mode more clock buffers are active than in standby-I mode and much more current is used. Standby-II occurs when CE is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO in this mode, the device will automatically enter TX mode and the packet is transmitted.

4.5 TX Mode

,, PTX device (PRIM_RX=0)

The TX mode is an active mode where the PTX device transmits a packet. To enter this mode from power down mode, the PTX device must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO, and a high pulse on the CE for more than 10µs.

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The PTX device stays in TX mode until it finishes transmitting the current packet. If CE = 0 it returns to standby-I mode. If CE = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the PTX device remains in TX mode, transmitting the next packet. If the TX FIFO is empty the PTX device goes into standby-II mode. It is important to never stay in TX mode for more than 4ms at one time.

If the auto retransmit is enabled (EN_AA=1) and auto acknowledge is required (NO_ACK=0), the PTX device will enter TX mode from standby-I mode when ARD elapsed and number of retried is less than ARC.

„ PRX device (PRIM_RX=1)

The PRX device will enter TX mode from RX mode only when EN_AA=1 and NO_ACK=0 in received packet to transmit acknowledge packet with pending payload in TX FIFO.

4.6 RX Mode

„ PRX device (PRIM_RX=1)

The RX mode is an active mode where the ITR242C radio is configured to be a receiver. To enter this mode from standby-I mode, the PRX device must have the PWR_UP bit set high, PRIM_RX bit set high and the CE pin set high. Or PRX device can enter this mode from TX mode after transmitting an acknowledge packet when EN_AA=1 and NO_ACK=0 in received packet.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the packet processing engine. The packet processing engine continuously searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The PRX device remains in RX mode until the MCU configures it to standby-I mode or power down mode.

In RX mode a carrier detection (CD) signal is available. The CD is set to high when a RF signal is detected inside the receiving frequency channel. The internal CD signal is filtered before presented to CD register. The RF signal must be present for at least 128 µs before the CD is set high.

„ PTX device (PRIM_RX=0)

The PTX device will enter RX mode from TX mode only when EN_AA=1 and NO_ACK=0 to receive acknowledge packet.

5 Packet Processing

5.1 Packet Format

The packet format has a preamble, address, packet control, payload and CRC field.

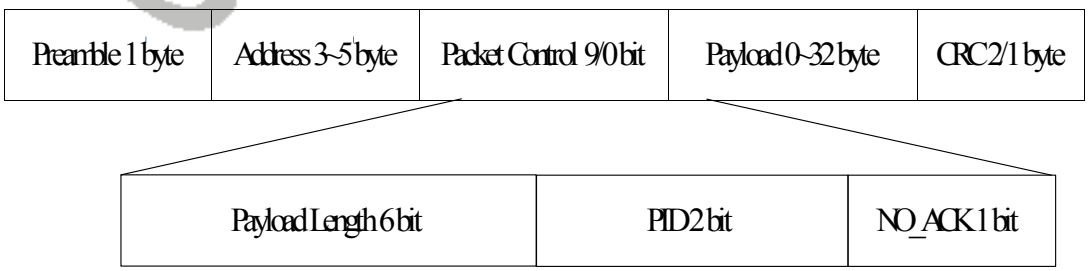

Figure 5 Packet Format

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5.1.1 Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

5.1.2 Address

This is the address for the receiver. An address ensures that the packet is detected by the target receiver. The address field can be configured to be 3, 4, or 5 bytes long by the AW register.

The PRX device can open up to six data pipes to support up to six PTX devices with unique addresses. All six PTX device addresses are searched simultaneously. In PRX side, the data pipes are enabled with the bits in the EN_RXADDR register. By default only data pipe 0 and 1 are enabled.

Each data pipe address is configured in the RX_ADDR_PX registers.

Each pipe can have up to 5 bytes configurable address. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the 4 most significant address bytes. The LSB byte must be unique for all 6 pipes.

To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet.

On the PRX, the RX_ADDR_Pn, defined as the pipe address, must be unique. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 on the PTX, and as the pipe address for the designated pipe on the PRX.

No other data pipe can receive data until a complete packet is received by a data pipe that has detected its address. When multiple PTX devices are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

5.1.3 Packet Control

When Dynamic Payload Length function is enabled, the packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit NO_ACK flag.

,, Payload length
The payload length field is only used if the Dynamic Payload Length function is enabled.

,, PID
The 2 bit PID field is used to detect whether the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields are used by the PRX device to determine whether a packet is old or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, ITR242C compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

,, NO_ACK
The NO_ACK flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

The PTX can set the NO_ACK flag bit in the Packet Control Field with the command: W_TX_PAYLOAD_NOACK. However, the function must first be enabled in the FEATURE register by setting the

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EN_DYN_ACK bit. When you use this option, the PTX goes directly to standby-I mode after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet.

5.1.4 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide, and it is transmitted on-air as it is uploaded (unmodified) to the device.

The ITR242C provides two alternatives for handling payload lengths, static and dynamic payload length. The static payload length of each of six data pipes can be individually set.

The default alternative is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side. Each pipe has its own payload length.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With DPL feature the ITR242C can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the command: R_RX_PL_WID.

In order to enable DPL the EN_DPL bit in the FEATURE register must be set. In RX mode the DYNPD register has to be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

5.1.5 CRC

The CRC is the error detection mechanism in the packet. The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. It may be either 1 or 2 bytes and is calculated over the address, Packet Control Field, and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value is 0xFF.
The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value is 0xFFFF.

No packet is accepted by receiver side if the CRC fails.

5.2 Packet Handling

ITR242C uses burst mode for payload transmission and receive.

The transmitter fetches payload from TX FIFO, automatically assembles it into packet and transmits the packet in a very short burst period with 1Mbps or 2Mbps air data rate.

After transmission, if the PTX packet has the NO_ACK flag set, ITR242C sets TX_DS and gives an active low interrupt IRQ to MCU. If the PTX is ACK packet, the PTX needs receive ACK from the PRX and then asserts the TX_DS IRQ.

The receiver automatically validates and disassembles received packet, if there is a valid packet within the new payload, it will write the payload into RX FIFO, set RX_DR and give an active low interrupt IRQ to MCU.

When auto acknowledge is enabled (EN_AA=1), the PTX device will automatically wait for acknowledge packet after transmission, and re-transmit original packet with the delay of ARD until an acknowledge packet is received or the number of re-transmission exceeds a threshold ARC. If the later one happens, ITR242C will set MAX_RT and give an active low interrupt

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IRQ to MCU. Two packet loss counters (ARC_CNT and PLOS_CNT) are incremented each time a packet is lost. The ARC_CNT counts the number of retransmissions for the current transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. ARC_CNT is reset by initiating a new transaction. PLOS_CNT is reset by writing to the RF_CH register. It is possible to use the information in the OBSERVE_TX register to make an overall assessment of the channel quality.

The PTX device will retransmit if its RX FIFO is full but received ACK frame has payload.

As an alternative for PTX device to auto retransmit it is possible to manually set the ITR242C to retransmit a packet a number of times. This is done by the REUSE_TX_PL command.

When auto acknowledge is enabled, the PRX device will automatically check the NO_ACK field in received packet, and if NO_ACK=0, it will automatically send an acknowledge packet to PTX device. If EN_ACK_PAY is set, and the acknowledge packet can also include pending payload in TX FIFO.

6 Data and Control Interface

6.1 TX/RX FIFO

The data FIFOs are used to store payload that is to be transmitted (TX FIFO) or payload that is received and ready to be clocked out (RX FIFO). The FIFO is accessible in both PTX mode and PRX mode.

There are three levels 32 bytes FIFO for both TX and RX, supporting both acknowledge mode or no acknowledge mode with up to six pipes.

- TX three levels, 32 byte FIFO
- RX three levels, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payload for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the FLUSH_TX command.

The RX FIFO in PRX may contain payload from up to three different PTX devices.
.
A TX FIFO in PTX can have up to three payloads stored.

The TX FIFO can be written to by three commands, W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commands give access to the TX_PLD register.

The RX FIFO can be read by the command R_RX_PAYLOAD in both PTX and PRX mode. This command gives access to the RX_PLD register.

The payload in TX FIFO in a PTX is NOT removed if the MAX_RT IRQ is asserted.

In the FIFO_STATUS register it is possible to read if the TX and RX FIFO are full or empty. The TX_REUSE bit is also available in the FIFO_STATUS register. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI command: W_TX_PAYLOAD or FLUSH TX.

6.2 Interrupt

In ITR242C there is an active low interrupt (IRQ) pin, which is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The IRQ pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG

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register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

The 3 bit pipe information in the STATUS register is updated during the IRQ pin high to low transition. If the STATUS register is read during an IRQ pin high to low transition, the pipe information is unreliable.

6.3 SPI Interface

6.3.1 SPI Command

The SPI commands are shown in Table 2. Every new command must be started by a high to low transition on CSN.

In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin.

The serial shifting SPI commands is in the following format:

- <Command word: MSB bit to LSB bit (one byte)>
- <Data bytes: LSB byte to MSB byte, MSB bit in each byte first> for all registers at bank 0 and register 9 to register 14 at bank 1
- <Data bytes: MSB byte to LSB byte, MSB bit in each byte first> for register 0 to register 8 at bank 1

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSB byte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSB byte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSB byte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSB byte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission

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ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_ACK_PAYLOAD • W_TX_PAYLOAD_NOACK A new ACTIVATE command with the same data deactivates them again. This is executable in power down or stand by modes only. The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on MISO. To activate these registers, use the ACTIVATE command followed by data 0x73. Then they can be accessed as any other register. Use the same command and data to deactivate the registers again. This write command followed by data 0x53 toggles the register bank, and the current register bank number can be read out from REG7 [7]
R_RX_PL_WID	0110 0000		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	1010 1PPP	1 to 32 LSB byte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32 LSB byte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

Table 2 SPI command

6.3.2 SPI Timing

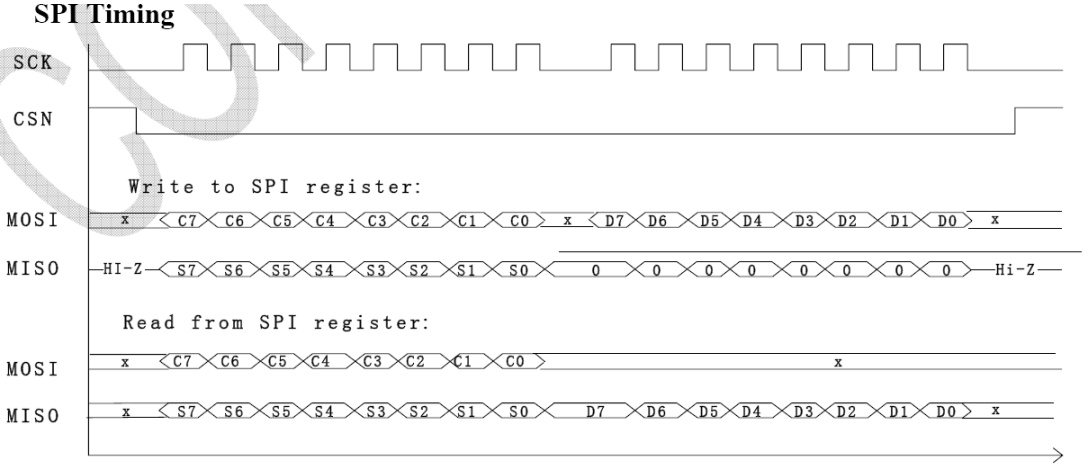


Figure 6 SPI timing

7 Register Map

Address（HEX）	Register	BIT	Recommend	R/W	Description
0	CONFIG				Operation Register
	DATAOUT_SEL	7	0	R/W	
	MASK_RX_DR	6	0	R/W	
	MASK_TX_DS	5	0	R/W	
	MASK_MAX_RT	4	0	R/W	
	EN_CRC	3	1	R/W	CRC Eanble 1: CRC enable，2byte 0: CRC disable，no CRC Checksum
	N/A	2	0	R/W	Reserve
	PWR_UP	1	0	R/W	Chip enable 1: POWER_UP 0: POWER_DOWN
	PRIM_RX	0	0	R/W	RX/TX control 1: PRX 0: PTX

1	EN_AA Enhanced Burst				Auto ACK
	Reserved	7:6	0	R/W	Only 00 allowed
	ENAA_P5	5	0	R/W	Enable pipe5 auto ACK
	ENAA_P4	4	0	R/W	Enable pipe4 auto ACK
	ENAA_P3	3	0	R/W	Enable pipe3 auto ACK
	ENAA_P2	2	0	R/W	Enable pipe2 auto ACK
	ENAA_P1	1	0	R/W	Enable pipe1 auto ACK
	ENAA_P0	0	1	R/W	Enable pipe0 auto ACK
2	EN_RXADDR				Receive channel enable
	Reserved	7:6	0	R/W	Only 00 allowed
	ERX_P5	5	0	R/W	Enable data pipe 5
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3
	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	0	R/W	Enable data pipe 1
	ERX_P0	0	1	R/W	Enable data pipe 0
3	SETUP_AW				Address setting
	Reserved	7:2	0	R/W	Only 000000 allowed
	AW	1:0	11	R/W	RX/TX Address width 00: 01: 3 Byte 10: 4 Byte 11: 5 Byte
4	SETUP_RETR				Auto transmission setting

	ARD	7:4	0	R/W	Auto delay timing 0000 :250μs 0001 :500μs 0010 :750μs …… 1111: 4000μs
	ARC	3:0	11	R/W	Auto retry count

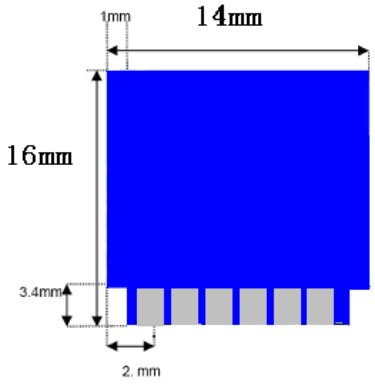
8 Electrical RF characteristic

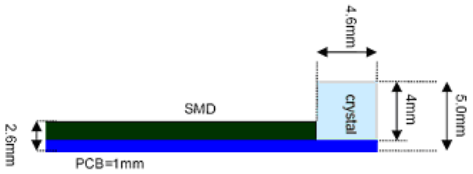
Characteristic	VCC = 3V± 5%， TA=25℃)	Value			Unit
		Min	Typical	Max	
ICC	Sleep		2		uA
	Standby I		50		uA
	Standby Ⅱ		750		uA
	TX (0dBm)		15	16	mA
	TX (8dBm)		23	25	mA
	RX (2Mbps)		15	16	mA
	RX (1Mbps)		14	15	mA
fOP	Operation frequency	2400		2483	MHz
PLLres	Phase lock loop step		1		MHz
f XTAL	Crystal		16		MHz
DR	Bit rate	1		2	Mbps
Δf_{1M}	Frequency Delta@1Mbps		160	250	KHz
Δf_{2M}	Frequency Delt@2Mbps		320	500	KHz
FCH 1M	Channel space @1Mbps		1		MHz
FCH 2 M	Channel space @2Mbps		2		MHz
	TX				
PRF	Typical power 1		8		dBm
PRF	Typical power 2		0		dBm
PRFC	Output power range	-11		11	dBm

PBW 2	CW 20dB bandwidth（2Mbps）		1.8	2.1	MHz
*PBW*1	CW 20dB bandwidth (1Mbps)		0.9	1.1	MHz
RX					
RX max	Bit error rate <0.1%@RX max		0		dBm
RXSENS 2	RX sensistivity（0.1%BER）@2Mbps		-85		dBm
*RXSENS*1	RX sensistivity（0.1%BER）@1Mbps		-88		dBm

C / I *CO*	*C* / I *CO* @2Mbps		13		dBc
C / I1*ST*	*C* / I1*ST* @2Mbps		-8		dBc
C / I2 *ND*	*C* / I2 *ND* @2Mbps		-12		dBc
C / I 3 *RD*	*C* / I 3 *RD* @2Mbps		-20		dBc
C / I4*TH*	*C* / I4*TH* @2Mbps		-28		dBc
C / I *CO*	*C* / I *CO* @1Mbps		13		dBc
C / I1*ST*	*C* / I1*ST* @1Mbps		5		dBc
C / I2 *ND*	*C* / I2 *ND* @1Mbps		-10		dBc
C / I 3 *RD*	*C* / I 3 *RD* @1Mbps		-16		dBc
C / I4*TH*	*C* / I4*TH* @1Mbps		-24		dBc
Operation					
VDD	Supply voltage	2.2	3	3.6	V
VSS	GND		0		V
VOH	High output	VDD-0.3		VDD	V
VOL	Low ouput	VSS		VSS+0.3	V
VIH	High input	2	3	3.6	V
VIL	Low input	VSS		VSS+0.3	V
TOP	Operation temperature	0		70	℃
TSTG	Storage Temperature	-20		85	℃

9 Dimension





PCB SIZE: 14x 16mm

Pitch: 2.00 mm

Tolerence: 0.2mm

10 Order Information .

ITR245XX-V YYYY Z

XX : L

YYYY : Customer code

Z : T = TX , R = RX

Eg. ITR245L

11 Update History

Ver.	Date	Description
1.0	Jan,2014	New Release
1.1	Oct,2014	Update the dimension
1.11	Jan 2015	Update dimension
1.20	AUG2015	New release for SOP8 version

ITR245L

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