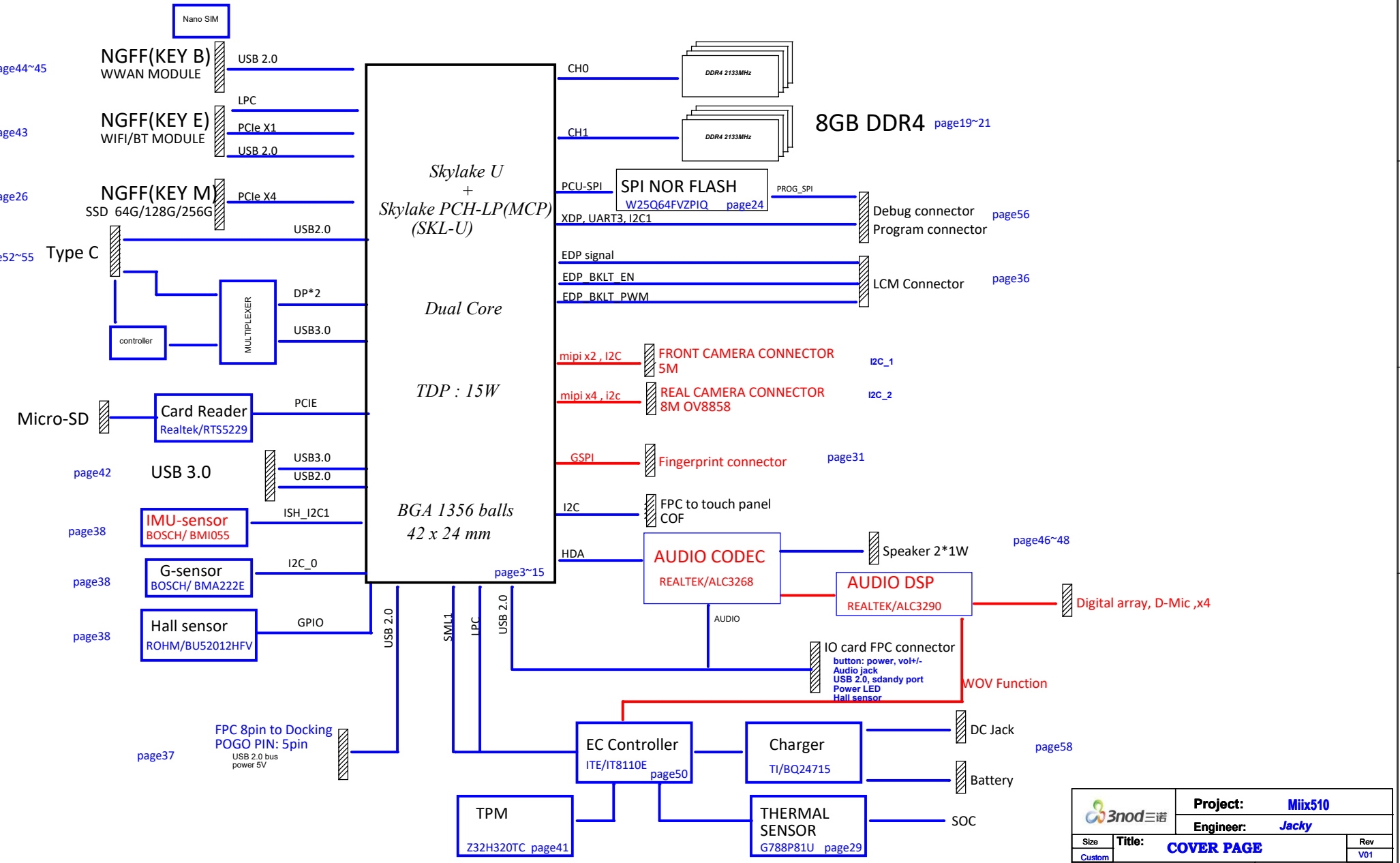
Basing on SKYLAKE-U MRD BASE BOARD
Miix510 for Lenovo



3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: COVER PAGE	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 1 of 69	

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Armour3 12.2" SDV plan

		44	40	40	42
					2017/2/23
Component		SKU1	SKU2	SKU3	SKU4
Color		Sliver	Sliver	Sliver	Sliver
MB	CPU	Intel Core i3-6006U	Intel Core i3-7100U	Intel Core i5-8200U	Intel Core i7-8500U
	RAM	Samsung 4G 4*1GB	Hynix 4G 4*1GB	Samsung 8G 4*2GB	Micron 16G 8*2GB
	TPM	国名技术 HW	Infineon HW	国名技术 HW	Infineon HW
System	SSD	TBD	TBD	TBD	TBD
	LCD Module	国显 12.2-inch, 1920x1200	国显 12.2-inch, 1920x1200	国显 12.2-inch, 1920x1200	国显 12.2-inch, 1920x1200
	Pannel	莱宝 12.2-inch	莱宝 12.2-inch	莱宝 12.2-inch	莱宝 12.2-inch
	active pen	BT Pen	Activer Pen	TBD	TBD
	Adapter	Chicony,45W,20V,2.25A	Delta,45W,20V,2.25A	Liteon,45W,20V,2.25A	Delta,45W,20V,2.25A
	Battery	欣旺达 TI+ATL	欣旺达 TI+ATL	欣旺达 TI+ATL	欣旺达 TI+ATL
	Keyboard	NA	NA	NA	NA
	Camera	OV5670/OV5670	OV5670/OV8858	OV5670/OV5670	OV5670/OV8858
	WLAN module	Intel 3165 1*1 AC	Liteon 1*1	Intel 2*2	Liteon 2*2
	LTE Module	NA	L831	L830	EM7455/TBD
	Speaker	力普斯	尚德铭泰	力普斯	尚德铭泰
Cable	Antenna	TBD	TBD	TBD	TBD
	LCD_FPC	崴旭	崴旭	国日宏	国日宏
	TP_FPC	崴旭	崴旭	国日宏	国日宏
	pogo_pin_FPC	崴旭	崴旭	国日宏	国日宏
	IO FFC	崴旭	崴旭	国日宏	国日宏
Package		NA	NA	NA	NA

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd_

Wed Jun 03 11:22:42 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
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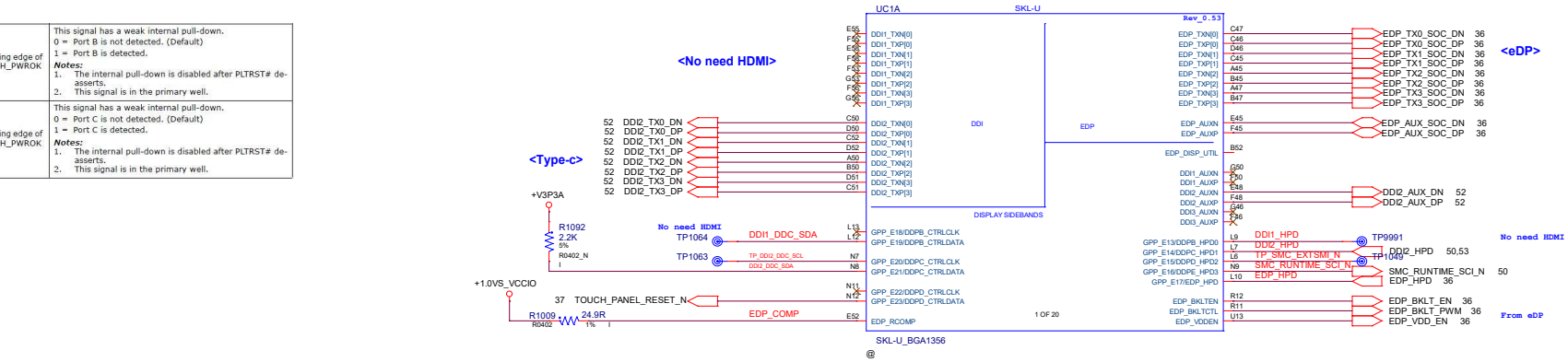
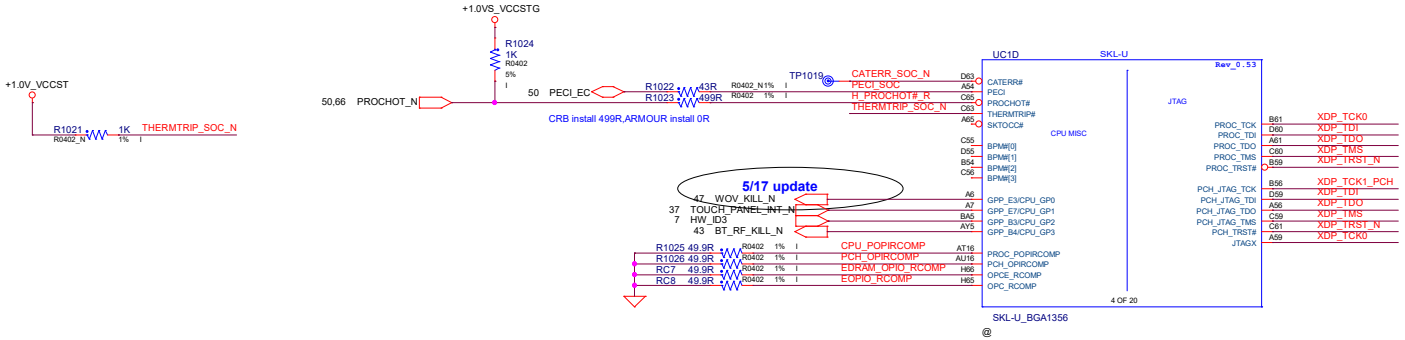
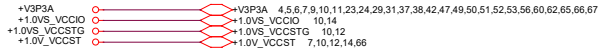
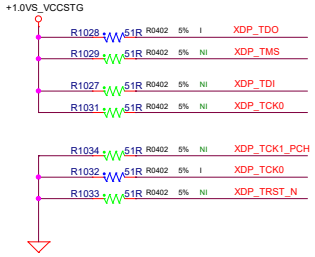
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.









3nod三诺	Project: Miix510		
	Engineer: Jacky		
Size: Custom	Title: SKL-U(1/12)DDI,MISC,XDP,EDP		Rev: V01
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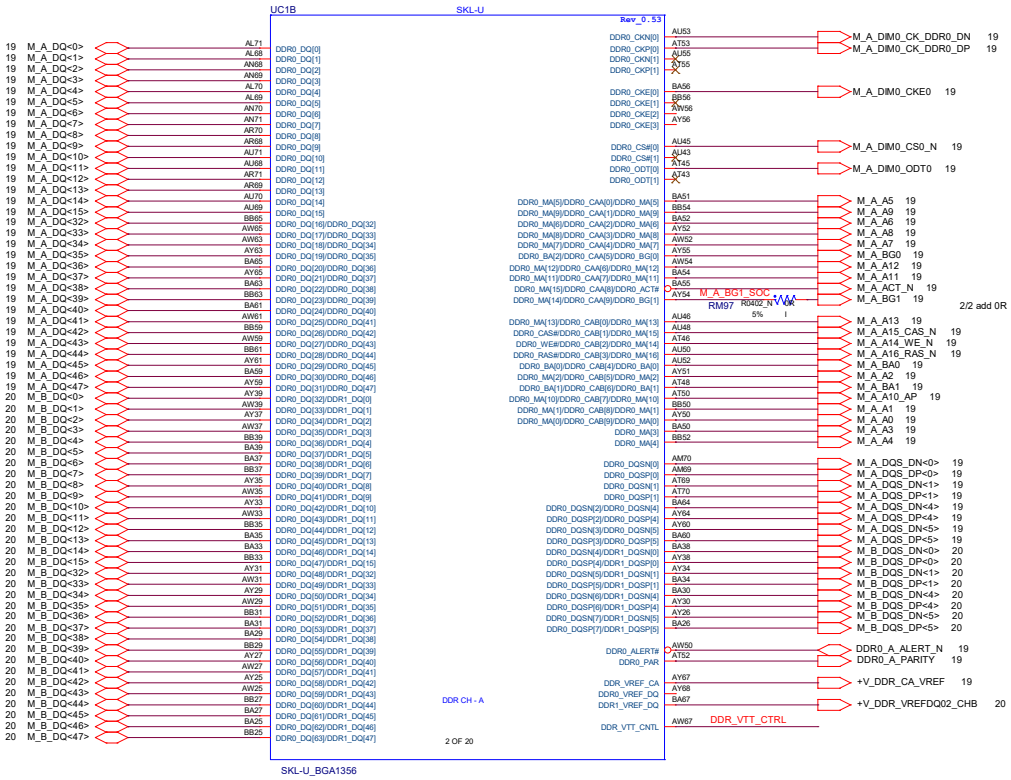
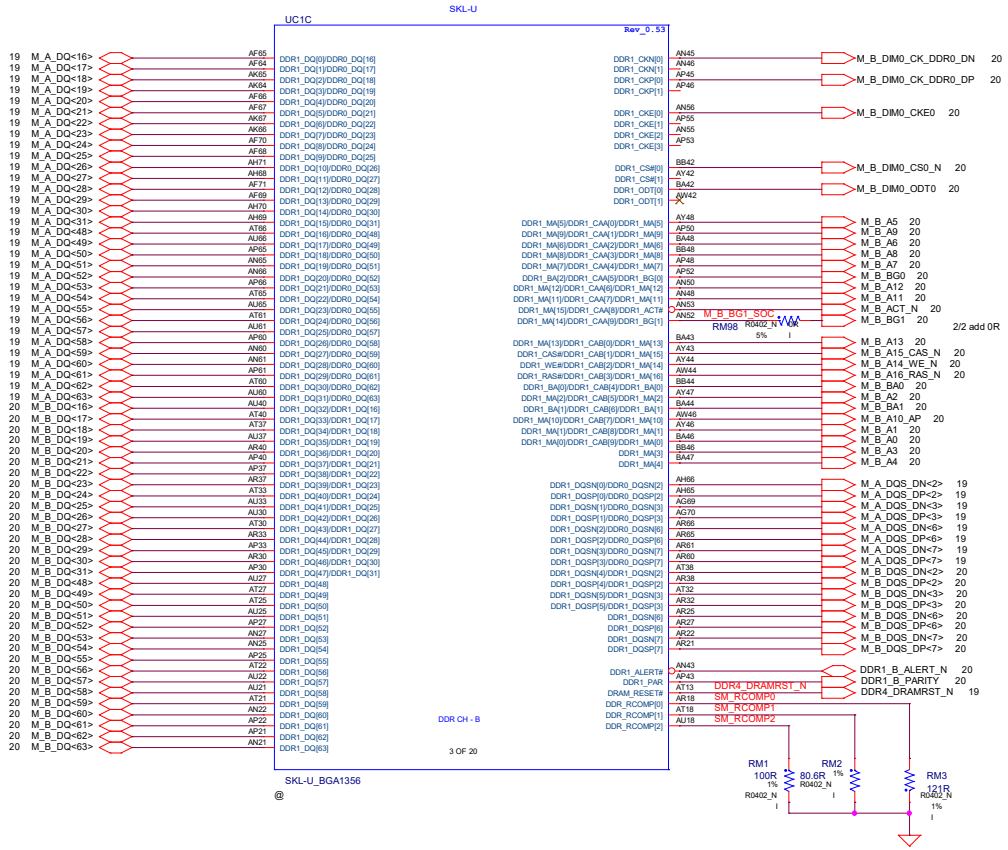
Non-Interleaved



Non-Interleaved

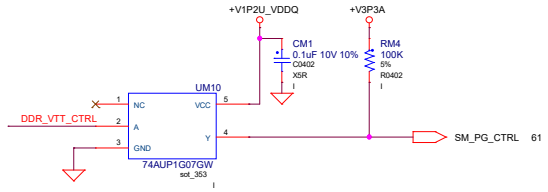


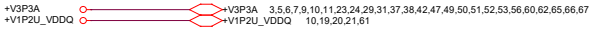
1. To support DDP, need to change two pins on DRAM. You have reserved them. Pls install the BOM.

	X16 SDP	X16 DDP TwinDie
DRAM M9 pin	VSS	Connect to CPU BG1
DRAM E9 Pin	VSS	UZQ

	SDP	DDP	
Memory size	4Gb or 8Gb	16Gb	
DRAM M9 pin	RM95,RM96,RM97,RM98 need uninstall RM99,RM100 need install	RM95,RM96,RM97,RM98 need install RM99,RM100 need uninstall	page4,19,20
DRAM E9 pin	RM79,RM81,RM83,RM85,RM87,RM89,RM91,RM93 need install 0 ohm	RM79,RM81,RM83,RM85,RM87,RM89,RM91,RM93 need install 240 ohm	page19,20
DDR_RCOMP0	RM3 200R need install	RM3 121R need install	page04
		Default	

2/2 Add (4Gb 8Gb) & (16Gb) BOM option table





3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SKL-U(2/12)DDR4	Rev: V01
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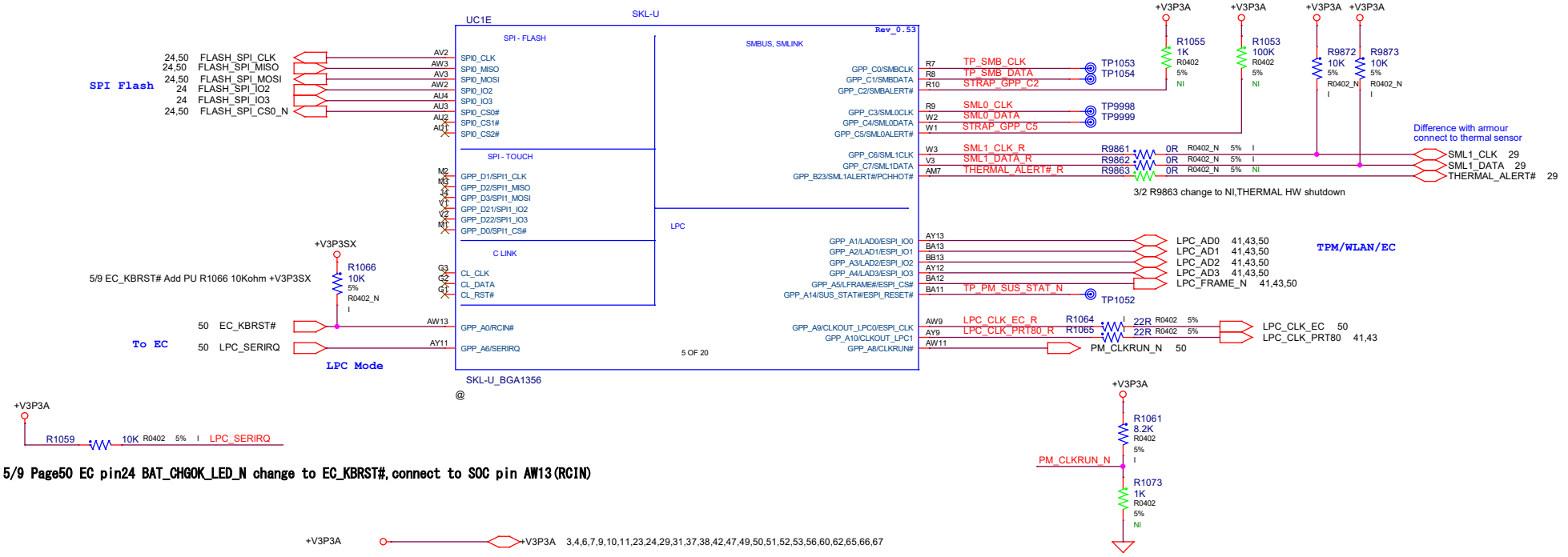

5/9 Page50 EC pin24 BAT_CHGOK_LED_N change to EC_KBRST#,connect to SOC pin AW13(RCIN)

SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SML1ALERT# / PCHHOT#/ GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

3nod三诺	**Project:** Miix510		
	Engineer: *Jacky*		
Size: Custom	**Title:** SKL-U(3/12)SPI,ESPI,SMB,LPC		Rev: V01
Date: Wednesday, May 24, 2017	Sheet 5 of 69		

To Enable ME Override

37,50 ME_Flash_EN — R9848 0R 5% I (R0402_N) — STRAP_HDA_SDO_SOC

Difference with armour
Add EC to enable ME override

5/23 R9848 install,BIOS request

HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.

SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

HDA for AUDIO

46 HDA_SYNC — RC393 33R R0402 5% I — HDA_SYNC_SOC
46 HDA_BCLK_R — R1086 33R R0402 5% I — HDA_BCLK
46 STRAP_HDA_SDO — RC395 33R R0402 5% I — STRAP_HDA_SDO_SOC
46 HDA_RST_N — RC394 33R R0402 5% I — HDA_RST_N_SOC

+V3P3A — R1054 1K R0402 5% NI

UC1G — SKL-U — Rev_0.53

AUDIO

HDA_SYNC_SOC — BA22 HDA_SYNC/I2S0_SFRM
HDA_BCLK — AY22 HDA_BLK/I2S0_SCLK
STRAP_HDA_SDO_SOC — BB22 HDA_SDO/I2S0_TXD
HDA_SDI0 — BA21 HDA_SDI0/I2S0_RXD
HDA_RST_N_SOC — AY21 HDA_SDI1/I2S1_RXD
AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD

46 HDA_SDI0

39 FCAM_RST_N — R10086 0R R0402_N 5% NI — FCAM_RST_N_CPU — RCAM_RST_N
TP10034

AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD

40 FCAM_CLK_EN
40 RCAM_CLK_EN

44 WWAN_DISABLE_N
43 WIFI_DISABLE_N

H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0

46 PCH_AUDIO_PWREN — D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1

+V3P3SX — R1052 100K R0402 5% NI — AW5 GPP_B14/SPKR

46 HDA_SPKR

1/4 Connect codec

SDIO/SDXC

AB11 GPP_G0/SD_CMD
AB13 GPP_G1/SD_DATA0
AB12 GPP_G2/SD_DATA1
W12 GPP_G3/SD_DATA2
W11 GPP_G4/SD_DATA3
W10 GPP_G5/SD_CD#
W8 GPP_G6/SD_CLK
W7 GPP_G7/SD_WP — TP_SD_WP — R9864 0R R0402_N 5% NI

Difference with armour
Add 0ohm NI

BA9 GPP_A17/SD_PWR_EN#/ISH_GP7
BB9 GPP_A16/SD_1P8_SEL

AB7 SD_RCOMP — SDMMC_RCOMP — R1015 200R R0402 1% I

AF13 GPP_F23 — FCAM_PD_N 39

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SKL-U_BGA1356

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Non-Micro SD

+V3P3A — +V3P3A 3,4,5,7,9,10,11,23,24,29,31,37,38,42,47,49,50,51,52,53,56,60,62,65,66,67
+V3P3SX — +V3P3SX 5,7,9,10,23,26,30,31,36,37,38,39,40,41,43,44,45,46

UC1I — SKL_ULT — Rev_0.53

CSI-2

Rear Camera1 8M

39 CSI2_RCAM_DATA0_DN — A36 CSI2_DN0
39 CSI2_RCAM_DATA0_DP — B36 CSI2_DP0
39 CSI2_RCAM_DATA1_DN — C38 CSI2_DN1
39 CSI2_RCAM_DATA1_DP — D38 CSI2_DP1
39 CSI2_RCAM_DATA2_DN — C36 CSI2_DN2
39 CSI2_RCAM_DATA2_DP — D36 CSI2_DP2
39 CSI2_RCAM_DATA3_DN — A38 CSI2_DN3
39 CSI2_RCAM_DATA3_DP — B38 CSI2_DP3

CSI2_CLKN0 — C37 — CSI2_RCAM_CLK_DN 39
CSI2_CLKP0 — D37 — CSI2_RCAM_CLK_DP 39
CSI2_CLKN1 — C32 — CSI2_FCAM_CLK_DN 39
CSI2_CLKP1 — D32 — CSI2_FCAM_CLK_DP 39
CSI2_CLKN2 — C29
CSI2_CLKP2 — D29
CSI2_CLKN3 — B26
CSI2_CLKP3 — A26

Front Camera 5M

39 CSI2_FCAM_DATA0_DN — C31 CSI2_DN4
39 CSI2_FCAM_DATA0_DP — D31 CSI2_DP4
39 CSI2_FCAM_DATA1_DN — C33 CSI2_DN5
39 CSI2_FCAM_DATA1_DP — D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_COMP — E13 — CSI2_COMP — R1013 100R R0402 1% I
GPP_D4/FLASHTRIG — B7 — CSI2_FLASH_STROBE — TP1061

3/18 Add TP1061

EMMC

AP2 GPP_F13/EMMC_DATA0
AP1 GPP_F14/EMMC_DATA1
AP3 GPP_F15/EMMC_DATA2
AN3 GPP_F16/EMMC_DATA3
AN1 GPP_F17/EMMC_DATA4
AN2 GPP_F18/EMMC_DATA5
AM4 GPP_F19/EMMC_DATA6
AM1 GPP_F20/EMMC_DATA7

AM2 GPP_F21/EMMC_RCLK
AM3 GPP_F22/EMMC_CLK
AP4 GPP_F12/EMMC_CMD

AT1 EMMC_RCOMP — EMMC_RCOMP — R1014 200R R0402 1% I

RCAM_PD_N 39
FCAM_ALLPWR_EN 39
RCAM_ALLPWR_EN 40

4/24 update

1/4 check PDG

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SKL-U_BGA1356

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Non-EMMC

Project:	Miix510		
Engineer:	Jacky		
Size: Custom	Title: SKL-U(4/12)HDA,EMMC,SD		Rev: V01
Date: Tuesday, June 06, 2017	Sheet 6 of 69		

	SDV	SIV	SIT	SVT
HW_ID0	0	1	0	1
HW_ID1	0	0	1	1

	TPM U9505	non-TPM U9505	non FP sensor	have FP sensor
HW_ID2	0	1		
HW_ID3			0	1

5/30 HW_ID3 add SAR sensor to decide on,driver request

Difference with armour
Modify HW_ID

2016/10/07

SSD

WLAN

UC1J SKL_ULT Rev_0.53 CLOCK SIGNALS 10 OF 20 SKL-U_BGA1356

3/10 Change C1249,C1250 from 22pF to 8.2pF

3/10 Change Y1000 from seiko to HOSONIC

3/10 Change C1251,C1252 from 18pF to 12pF

3/21 Change C1251,C1252 from 12pF to 15pF, hosonic & seiko share

1/13 Add RTC reset circuit.

UC1K SKL-U SYSTEM POWER MANAGEMENT Rev_0.53 11 OF 20 SKL-U_BGA1356

Difference with armour
SLP_SUS_N open +3V_PRIM

Difference with armour
Del U1201 Low-power buffer(74AUP1G07GW)
and add Dual MOS to change level

to WWAN reset pin

2/24 Add R1042,VR_PWRGD connect to SOC and EC

CHG_ACOK change to ACPRES from Charger IC

Project:	Miix510
Engineer:	Jacky
Size	Custom
Title:	SKL-U(5/12)CLK,GPIO
Rev	V01
Date:	Tuesday, June 06, 2017
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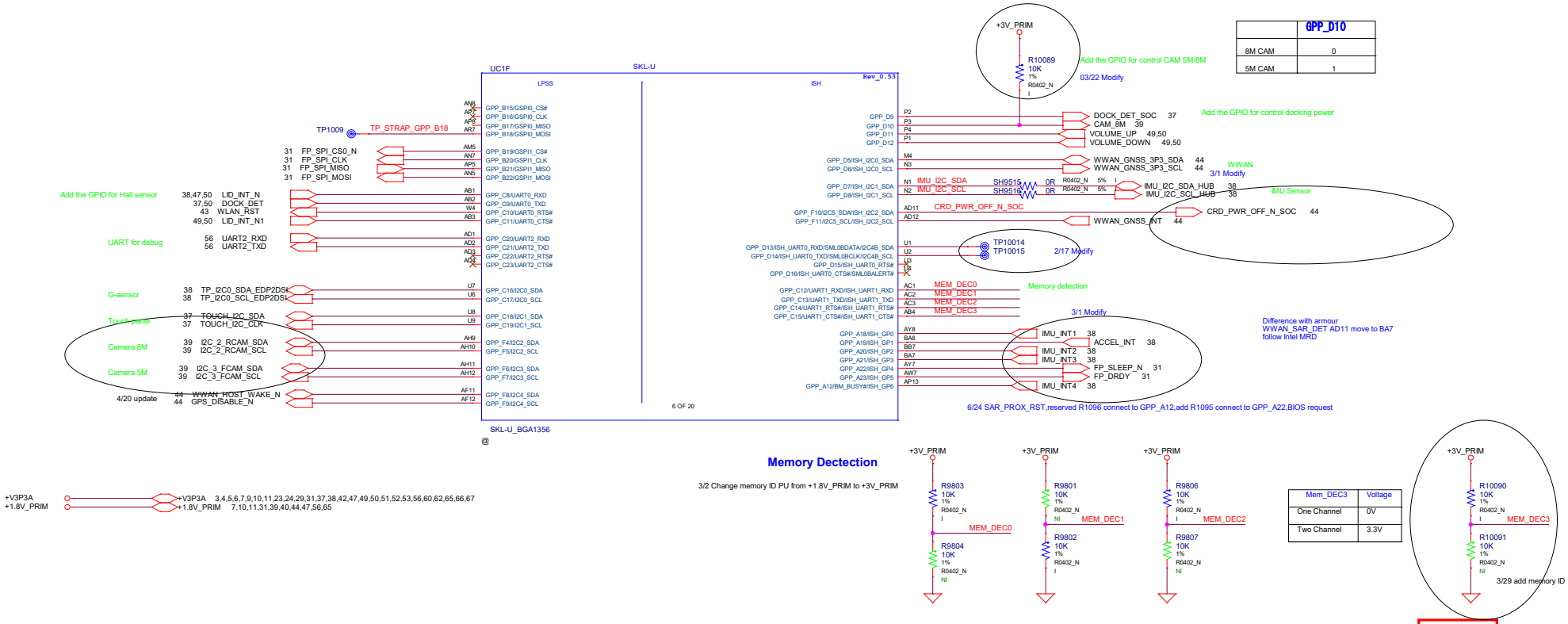


	GPP_D10
8M CAM	0
5M CAM	1

Memory Dectection

3/2 Change memory ID PU from +1.8V_PRIM to +3V_PRIM

Mem_DEC3	Voltage
One Channel	0V
Two Channel	3.3V

	Hynix 4GB SDP	Micron 4GB SDP	Samsung 4GB SDP	Hynix 8GB DDP	Micron 8GB DDP	Samsung 8GB DDP	Hynix 8GB SDP	Micron 8GB SDP	Samsung 8GB SDP	Hynix 16GB DDP	Micron 16GB DDP	Samsung 16GB DDP
MEM_DEC0	0	1	0	1	0	1	0	1	0	1	0	1
MEM_DEC1	0	0	1	1	0	0	0	0	1	1	0	0
MEM_DEC2	0	0	0	0	1	1	0	0	0	0	1	1
MEM_DEC3	0	0	0	0	0	0	1	1	1	1	1	1

Default

MB	CPU	Intel Core i3-6006U	Intel Core i3-7100U	Intel Core i5-8200U	Intel Core i7-8500U	
	RAM	Samsung 4G 4*1GB	Hynix 4G 4*1GB	Samsung 8G 4*2GB	Micron 16G 8*2GB	
	TPM	国名技术 HW	Infineon HW	国名技术 HW	Infineon HW	

RAM	8Gbx16 DDR4 2400 SDRAM (单颗容量 1GB)	Samsung	K4A8G165WC-BCRC	BS	1	(C/8Gb /18nm/SDP)		SM30N71798
		Micron 2666	MT40A512M16LY-075:H	BS	2	(1xnm/Z11C/8Gbx16/SDP)		SM30K25300
		Hynix	H5AN8G6NAFR-UHC	BS	3			SM30L08875
	16Gb*16 DDR4 2400 SDRAM(单颗容量 2GB)	Samsung	K4AAG165WB-MCRC	BS	1	(B/8Gb /20nm/DDP)		SM30L08872
		Hynix	H5ANAG6NAMR-UHC	BS	3	(A/8Gb /2znm/DDP)		SM30N07785
		Micron	MT40A1G16WBU-083E:B	BS	2	(Z01A/8Gb/20nm/DDP)		SM30L08873

GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Project:	Miix510	
Engineer:	Jacky	
Size: Custom	Title: SKL-U(6/12)GPIO	Rev: V01
Date: Tuesday, June 06, 2017	Sheet 8 of 69	

Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

UC1H — SKL-U — Rev_0.53

PCIE/USB3/SATA

NGFF WIFI Module

43 PCIE_WLAN_LN0_RX_SOC_DN
43 PCIE_WLAN_LN0_RX_SOC_DP
43 PCIE_WLAN_LN0_TX_SOC_DN
43 PCIE_WLAN_LN0_TX_SOC_DP

5/4 WIFI PCIE port 8 change to port 4,because PCH HSIO 8 can use PCIe interface (for Base-U)

45 PCIE_SD_LN0_RX_SOC_DN
45 PCIE_SD_LN0_RX_SOC_DP
45 PCIE_SD_LN0_TX_SOC_DN
45 PCIE_SD_LN0_TX_SOC_DP

C9586 0.22uF 10V 10% C0402_NX5R — CPU_SD_TX_DN
C9587 0.22uF 10V 10% C0402_NX5R — CPU_SD_TX_DP

2016/10/07

NGFF SSD

26 PCIE9_SSD_RX_DN
26 PCIE9_SSD_RX_DP
26 PCIE9_SSD_TX_DN_C
26 PCIE9_SSD_TX_DP_C

C0600 0.22uF 10V 10% C0402_NX5R — PCIE9_SSD_TX_DN
C0601 0.22uF 10V 10% C0402_NX5R — PCIE9_SSD_TX_DP

26 PCIE10_SSD_RX_DN
26 PCIE10_SSD_RX_DP
26 PCIE10_SSD_TX_DN_C
26 PCIE10_SSD_TX_DP_C

C0602 0.22uF 10V 10% C0402_NX5R — PCIE10_SSD_TX_DN
C0603 0.22uF 10V 10% C0402_NX5R — PCIE10_SSD_TX_DP

R1063 100R 1% R0402 — PCIE_RCOMP_N / PCIE_RCOMP_P

TP1051 XDP_PRDY_N
TP1062 XDP_PREQ_N
TP1050 TP_EC_CS_WAKE

26 PCIE11_SSD_RX_DN
26 PCIE11_SSD_RX_DP
26 PCIE11_SSD_TX_DN_C
26 PCIE11_SSD_TX_DP_C
26 PCIE12_SSD_RX_DN
26 PCIE12_SSD_RX_DP
26 PCIE12_SSD_TX_DN_C
26 PCIE12_SSD_TX_DP_C

C0604 0.22uF 10V 10% C0402_NX5R — PCIE11_SSD_TX_DN
C0605 0.22uF 10V 10% C0402_NX5R — PCIE11_SSD_TX_DP
C0606 0.22uF 10V 10% C0402_NX5R — PCIE12_SSD_TX_DN
C0607 0.22uF 10V 10% C0402_NX5R — PCIE12_SSD_TX_DP

Difference with armour
SSD interface SATA change to PCIE
SATA1A change to PCIE port 9,10,11,12

Checklist
Gen1 and Gen2=100nF
Gen3=220nF

SSIC / USB3

USB3_1_RXN H8 — USB3_P1_RX_DN 42
USB3_1_RXP G8 — USB3_P1_RX_DP 42
USB3_1_TXN C13 — USB3_P1_TX_DN 42
USB3_1_TXP D13 — USB3_P1_TX_DP 42

USB3.0 CONN

USB3_2_RXN/SSIC_1_RXN J6 — USB3_P2_WP2_RX_DN 52
USB3_2_RXP/SSIC_1_RXP H6 — USB3_P2_WP2_RX_DP 52
USB3_2_TXN/SSIC_1_TXN B13 — USB3_P2_WP2_TX_DN 52
USB3_2_TXP/SSIC_1_TXP A13 — USB3_P2_WP2_TX_DP 52

Type-c

USB3_3_RXN/SSIC_2_RXN J10 — USB3_P3_WWAN_SSIC_RX_DN 44
USB3_3_RXP/SSIC_2_RXP H10 — USB3_P3_WWAN_SSIC_RX_DP 44
USB3_3_TXN/SSIC_2_TXN B15 — USB3_P3_WWAN_SSIC_TX_DN 44
USB3_3_TXP/SSIC_2_TXP A15 — USB3_P3_WWAN_SSIC_TX_DP 44

WWAN

USB3_4_RXN E10
USB3_4_RXP E10
USB3_4_TXN D15
USB3_4_TXP D15

USB2

USB2N_1 / USB2P_1 — AB9 / AB10 — USB2_P1_WP1_DN 42 / USB2_P1_WP1_DP 42
USB2N_2 / USB2P_2 — AD6 / AD7 — USB2_P2_WP2_DN 55 / USB2_P2_WP2_DP 55
USB2N_3 / USB2P_3 — AH3 / AJ3 — USB2_P3_WWAN_DN 44 / USB2_P3_WWAN_DP 44
USB2N_4 / USB2P_4 — AD9 / AD10 — USB2_P4_BT_DN 43 / USB2_P4_BT_DP 43
USB2N_5 / USB2P_5 — AJ1 / AJ2 — USB2_P5_DOCK_DN 37 / USB2_P5_DOCK_DP 37
USB2N_6 / USB2P_6 — AF6 / AF7
USB2N_7 / USB2P_7 — AH1 / AH2
USB2N_8 / USB2P_8 — AF8 / AF9
USB2N_9 / USB2P_9 — AG1 / AG2
USB2N_10 / USB2P_10 — AH7 / AH8

USB3.0 connector
Type-c
NGFF WWAN Module
BT
USB 2.0 docking

USB2_COMP AB6 — USB2_COMP — R1012 113R R0402 1% I
USB2_ID AG3 — USB2_P1_WP1_OTG_ID — R1084 1K R0402_N 5% I
USB2_VBUSSENSE AG4 — USB2_VBUSSENSE — R1085 1K R0402_N 5% I

GPP_E9/USB2_OC0# A9 — USB2_P1_WP1_OC_N 42
GPP_E10/USB2_OC1# C9 — USB2_P2_WP2_OC_N 53
GPP_E11/USB2_OC2# D9 — WWAN_PWR_ON 44
GPP_E12/USB2_OC3# B9 — USB2_P2_WP3_OC_N

Difference with armour
B9 modify to WWAN_PWR_ON

GPP_E4/DEVSLP0 J1 — TP_SATA0_DEVSLP — TP1079
GPP_E5/DEVSLP1 J2 — SATA1_DEVSLP — TP8201
GPP_E6/DEVSLP2 J3 — SATA2_DEVSLP 26

Difference with armour
modify SATA2_DEVSLP

GPP_E0/SATAXPCIE0/SATAGP0 H2 — TP_SSD_SATA0_PCIE_DET_N — TP1080
GPP_E1/SATAXPCIE1/SATAGP1 H3 — TP1082
GPP_E2/SATAXPCIE2/SATAGP2 G4 — SSD_SATA_PCIE_DET_N

Difference with armour
SSD_SATA_PCIE_DET_N connect to G4 pin

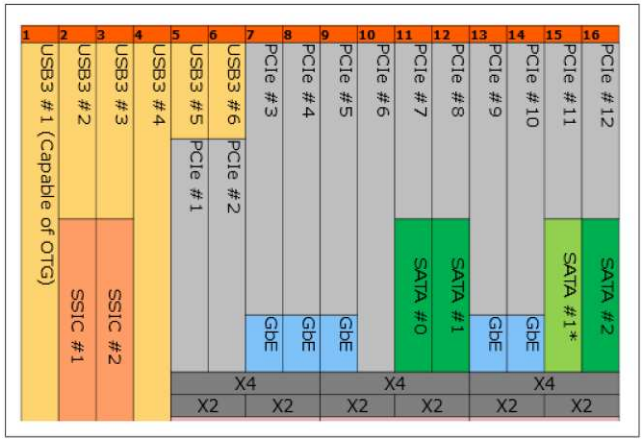
GPP_E8/SATALED# H1 — TP_EDP2DSI_CORE_PWR_EN — TP8213

8 OF 20

SKL-U_BGA1356

@

High Speed I/O (HSIO) Lane Multiplexing in SKL U



GPIO	DEVICE CONTROL
USB_OC0#	Type C
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	WWAN_PWR_ON
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NGFF SSD KEY M
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD_SATA_PCIE_DET_N

+V3P3A — R9882 10K 5% R0402_N I — USB2_P2_WP3_OC_N

1/7 Add PU +V3P3A

Difference with armour
R1050 install,R1087 uninstall

+V3P3SX — R1087 100K 5% R0402_N NI — SSD_SATA_PCIE_DET_N — R1050 10K 5% R0402_N I

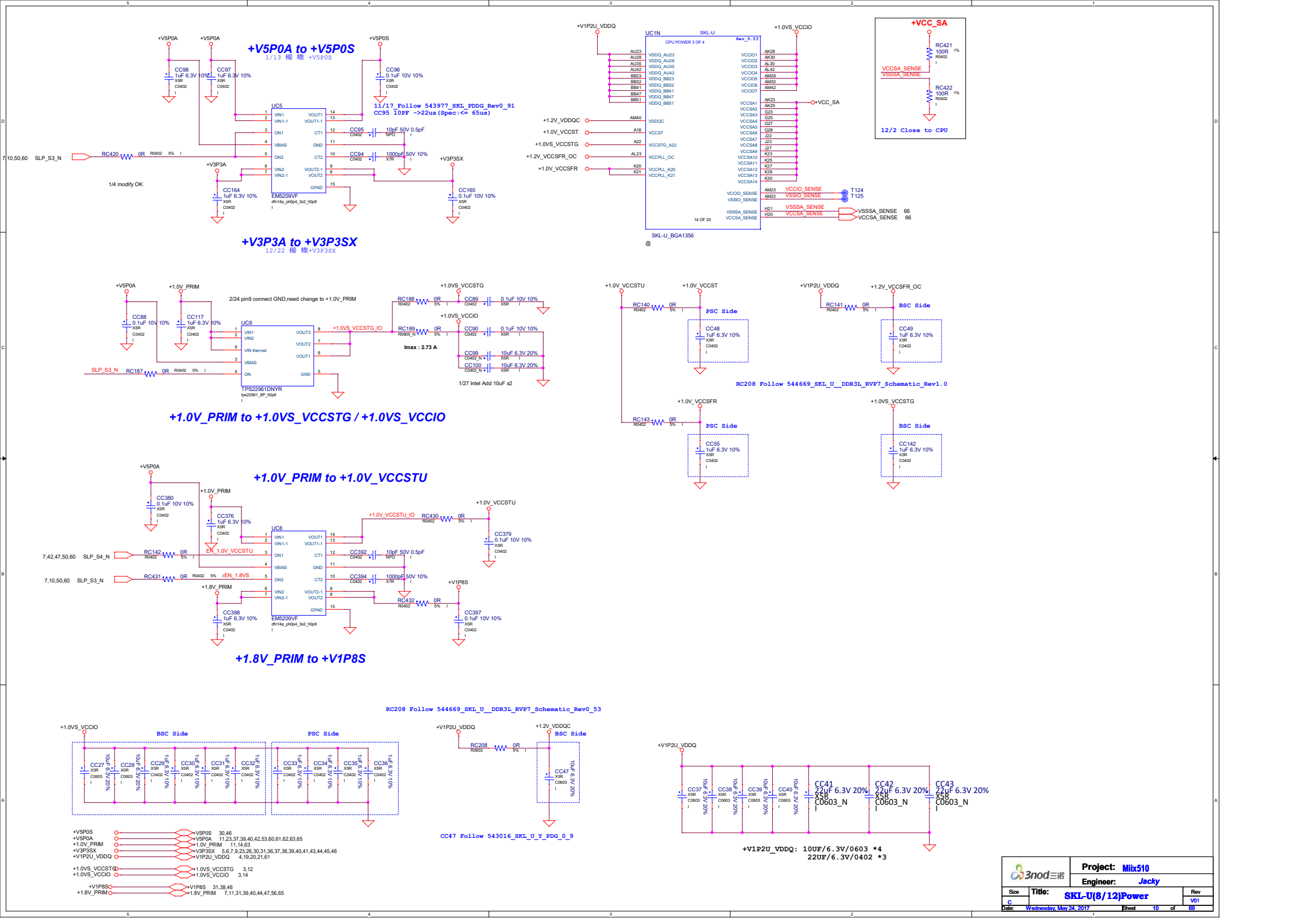
NOTE:
USE FITC TO ALLOW SELECTION OF
PCIE VS SATA BASED ON STRAPPING:

GPP_E_2 FOR SATA2/PCIE:
1 - SATA2, 0 - PCIE P9,P10,P11,P12

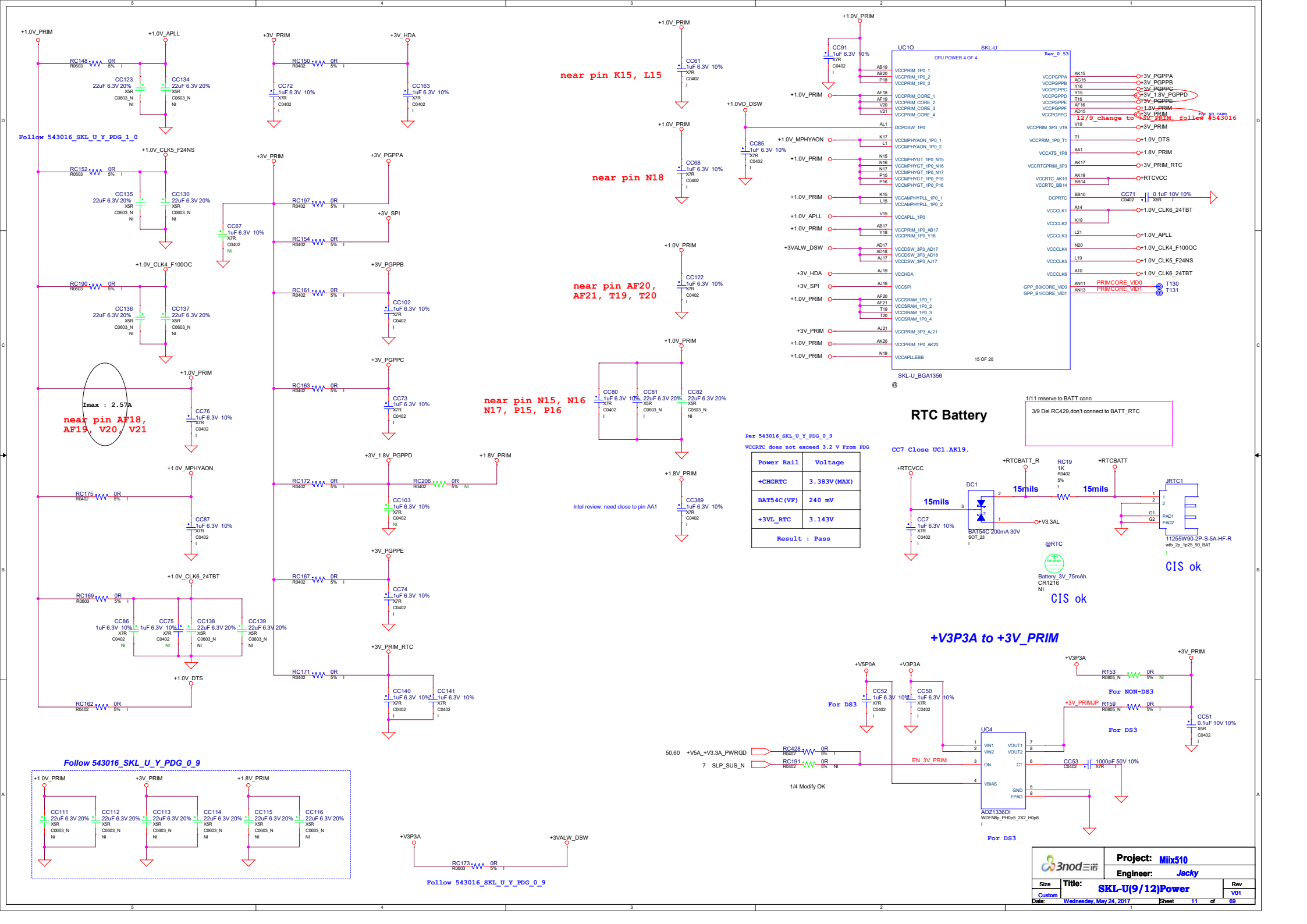
+V3P3A
+V3P3SX

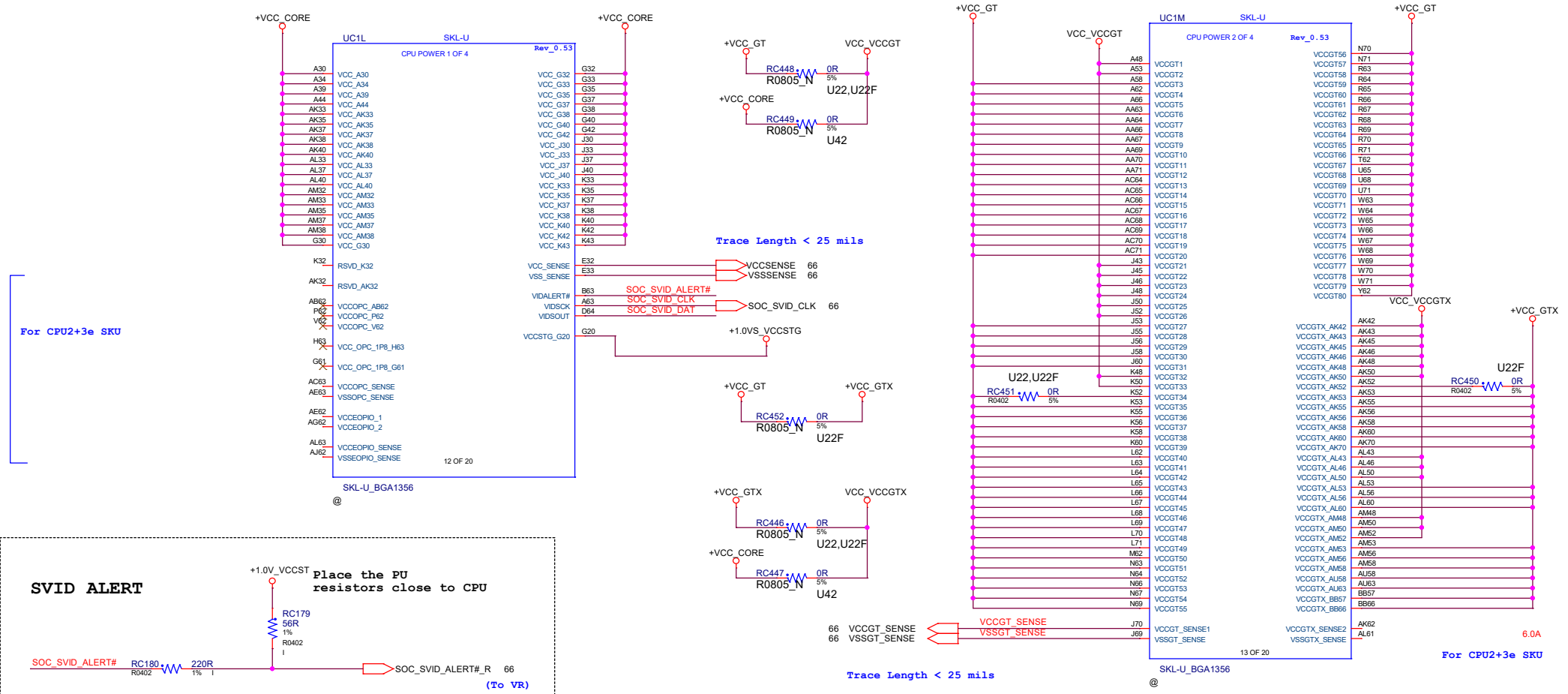
+V3P3A 3,4,5,6,7,10,11,23,24,29,31,37,38,42,47,49,50,51,52,53,56,60,62,65,66,67
+V3P3SX 5,6,7,10,23,26,30,31,36,37,38,39,40,41,43,44,45,46

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SKL-U(7/12)PCIE,USB,SATA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 9 of 69	



Project:	Miix510
Engineer:	Jacky
Size	C
Title:	SKL-U(8/12)Power
Rev	V01
Date:	Wednesday, May 24, 2017
Sheet	10 of 69


+1.0V_PRIM
+1.0V_APLL
RC148 0R
CC123 22uF 6.3V 20%
CC134 22uF 6.3V 20%
Follow 543016_SKL_U_Y_PDG_1_0
+1.0V_CLK5_F24NS
RC152 0R
CC135 22uF 6.3V 20%
CC130 22uF 6.3V 20%
+1.0V_CLK4_F100OC
RC190 0R
CC136 22uF 6.3V 20%
CC137 22uF 6.3V 20%
Imax : 2.57A
near pin AF18, AF19, V20, V21
CC76 1uF 6.3V 10%
+1.0V_MPHYAON
RC175 0R
CC87 1uF 6.3V 10%
+1.0V_CLK6_24TBT
RC169 0R
CC86 1uF 6.3V 10%
CC75 1uF 6.3V 10%
CC138 22uF 6.3V 20%
CC139 22uF 6.3V 20%
+1.0V_DTS
RC162 0R
+3V_PRIM
RC150 0R
CC72 1uF 6.3V 10%
+3V_HDA
CC163 1uF 6.3V 10%
RC197 0R
CC67 1uF 6.3V 10%
+3V_PGPPA
+3V_SPI
RC154 0R
RC161 0R
+3V_PGPPB
CC102 1uF 6.3V 10%
RC163 0R
+3V_PGPPC
CC73 1uF 6.3V 10%
+3V_1.8V_PGPPD
+1.8V_PRIM
RC172 0R
RC206 0R
CC103 1uF 6.3V 10%
RC167 0R
+3V_PGPPE
CC74 1uF 6.3V 10%
RC171 0R
+3V_PRIM_RTC
CC140 1uF 6.3V 10%
CC141 1uF 6.3V 10%
Follow 543016_SKL_U_Y_PDG_0_9
+1.0V_PRIM
+3V_PRIM
+1.8V_PRIM
CC111 22uF 6.3V 20%
CC112 22uF 6.3V 20%
CC113 22uF 6.3V 20%
CC114 22uF 6.3V 20%
CC115 22uF 6.3V 20%
CC116 22uF 6.3V 20%
+V3P3A
+3VALW_DSW
RC173 0R
Follow 543016_SKL_U_Y_PDG_0_9
near pin K15, L15
CC61 1uF 6.3V 10%
near pin N18
CC68 1uF 6.3V 10%
near pin AF20, AF21, T19, T20
CC122 1uF 6.3V 10%
near pin N15, N16 N17, P15, P16
CC80 1uF 6.3V 10%
CC81 22uF 6.3V 20%
CC82 22uF 6.3V 20%
Intel review: need close to pin AA1
CC389 1uF 6.3V 10%
+1.0VO_DSW
CC85 1uF 6.3V 10%
CC91 1uF 6.3V 10%
UC1O SKL-U
CPU POWER 4 OF 4
Rev_0.53
VCCPRIM_1P0_1
VCCPRIM_1P0_2
VCCPRIM_1P0_3
VCCPRIM_CORE_1
VCCPRIM_CORE_2
VCCPRIM_CORE_3
VCCPRIM_CORE_4
DCPDSW_1P0
VCCMPHYAON_1P0_1
VCCMPHYAON_1P0_2
VCCMPHYGT_1P0_N15
VCCMPHYGT_1P0_N16
VCCMPHYGT_1P0_N17
VCCMPHYGT_1P0_P15
VCCMPHYGT_1P0_P16
VCCAMPHYPLL_1P0_1
VCCAMPHYPLL_1P0_2
VCCAPLL_1P0
VCCPRIM_1P0_AB17
VCCPRIM_1P0_Y18
VCCDSW_3P3_AD17
VCCDSW_3P3_AD18
VCCDSW_3P3_AJ17
VCCHDA
VCCSPI
VCCSRAM_1P0_1
VCCSRAM_1P0_2
VCCSRAM_1P0_3
VCCSRAM_1P0_4
VCCPRIM_3P3_AJ21
VCCPRIM_1P0_AK20
VCCAPLLEBB
15 OF 20
SKL-U_BGA1356
VCCPGPPA
VCCPGPPB
VCCPGPPC
VCCPGPPD
VCCPGPPE
VCCPGPPF
VCCPGPPG
VCCPRIM_3P3_V19
VCCPRIM_1P0_T1
VCCATS_1P8
VCCRTCPRIM_3P3
VCCRTC_AK19
VCCRTC_BB14
DCPRTC
VCCCLK1
VCCCLK2
VCCCLK3
VCCCLK4
VCCCLK5
VCCCLK6
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
+3V_PGPPA
+3V_PGPPB
+3V_PGPPC
+3V_1.8V_PGPPD
+3V_PGPPE
+1.8V_PRIM
+3V_PRIM
12/9_change to +3V_PRIM, follow #543016
+3V_PRIM
+1.0V_DTS
+1.8V_PRIM
+3V_PRIM_RTC
+RTCVCC
0.1uF 10V 10%
+1.0V_CLK6_24TBT
+1.0V_APLL
+1.0V_CLK4_F100OC
+1.0V_CLK5_F24NS
+1.0V_CLK6_24TBT
PRIMCORE_VID0
PRIMCORE_VID1
T130
T131
Per 543016_SKL_U_Y_PDG_0_9
VCCRTC does not exceed 3.2 V From PDG
Power Rail | Voltage
+CHGRTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
+3VL_RTC | 3.143V
Result : Pass
RTC Battery
1/11 reserve to BATT conn
3/9 Del RC429,don't connect to BATT_RTC
CC7 Close UC1.AK19.
+RTCVCC
+RTCBATT_R
RC19 1K
+RTCBATT
15mils
15mils
15mils
DC1
CC7 1uF 6.3V 10%
BAT54C 200mA 30V
SOT_23
+V3.3AL
@RTC
Battery_3V_75mAh
CR1216
NI
JRTC1
11255W90-2P-S-5A-HF-R
wtb_2p_1p25_90_BAT
CIS ok
CIS ok
+V3P3A to +3V_PRIM
+V5P0A
+V3P3A
CC52 1uF 6.3V 10%
CC50 1uF 6.3V 10%
For DS3
50,60 +V5A_+V3.3A_PWRGD
7 SLP_SUS_N
RC428 0R
RC191 0R
EN_3V_PRIM
UC4
VIN1
VIN2
VOUT1
VOUT2
ON
CT
VBIAS
GND
EPAD
AOZ1336DI
WDFN8p_PH0p5_2X2_H0p8
CC53 1000pF 50V 10%
+3V_PRIMJP
R159 0R
For DS3
R153 0R
For NON-DS3
CC51 0.1uF 10V 10%
1/4 Modify OK
For DS3
3nod三诺
Project: Miix510
Engineer: Jacky
Size: Custom
Title: SKL-U(9/12)Power
Rev: V01
Date: Wednesday, May 24, 2017
Sheet 11 of 69

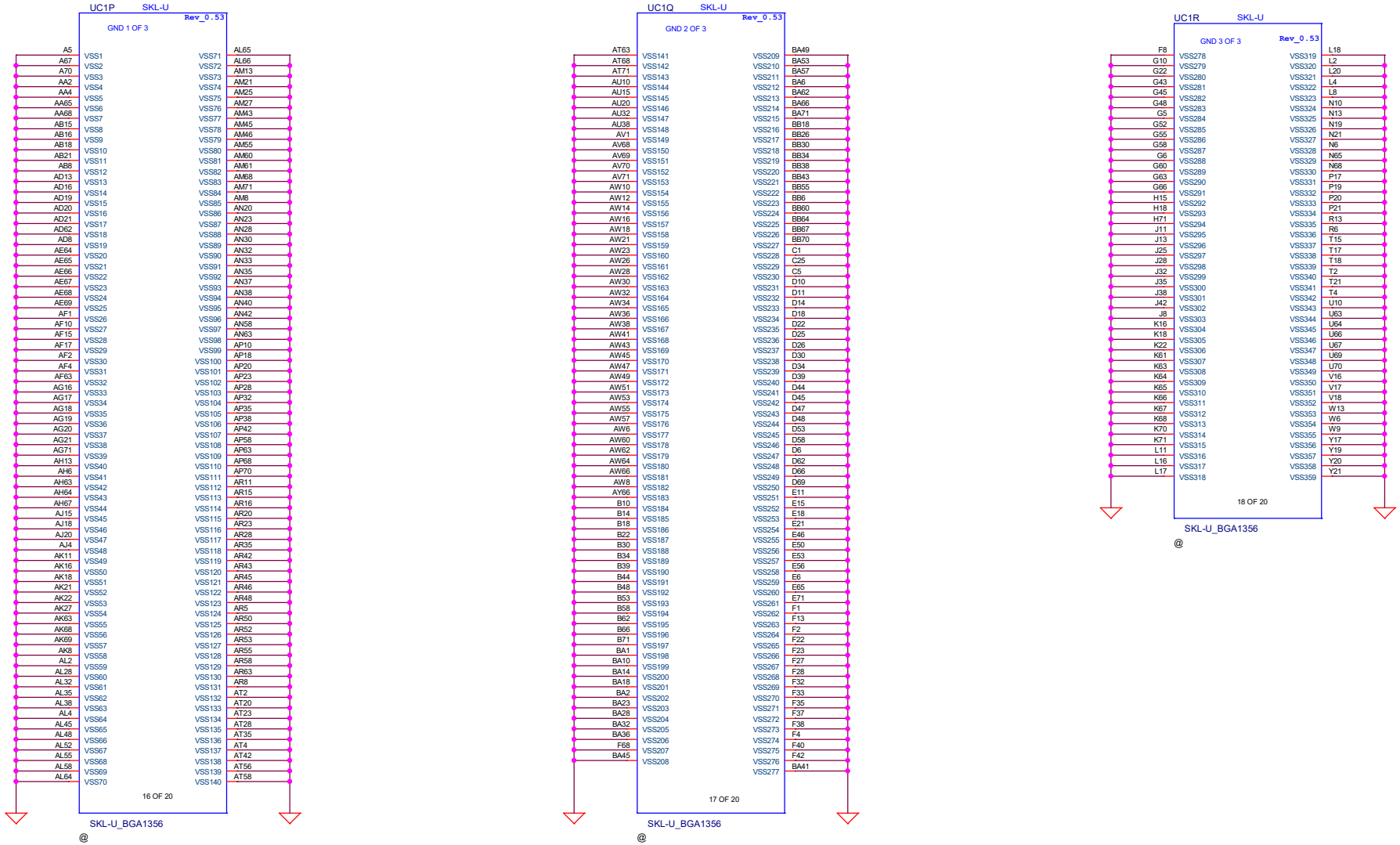


Package Sensing Recommendations

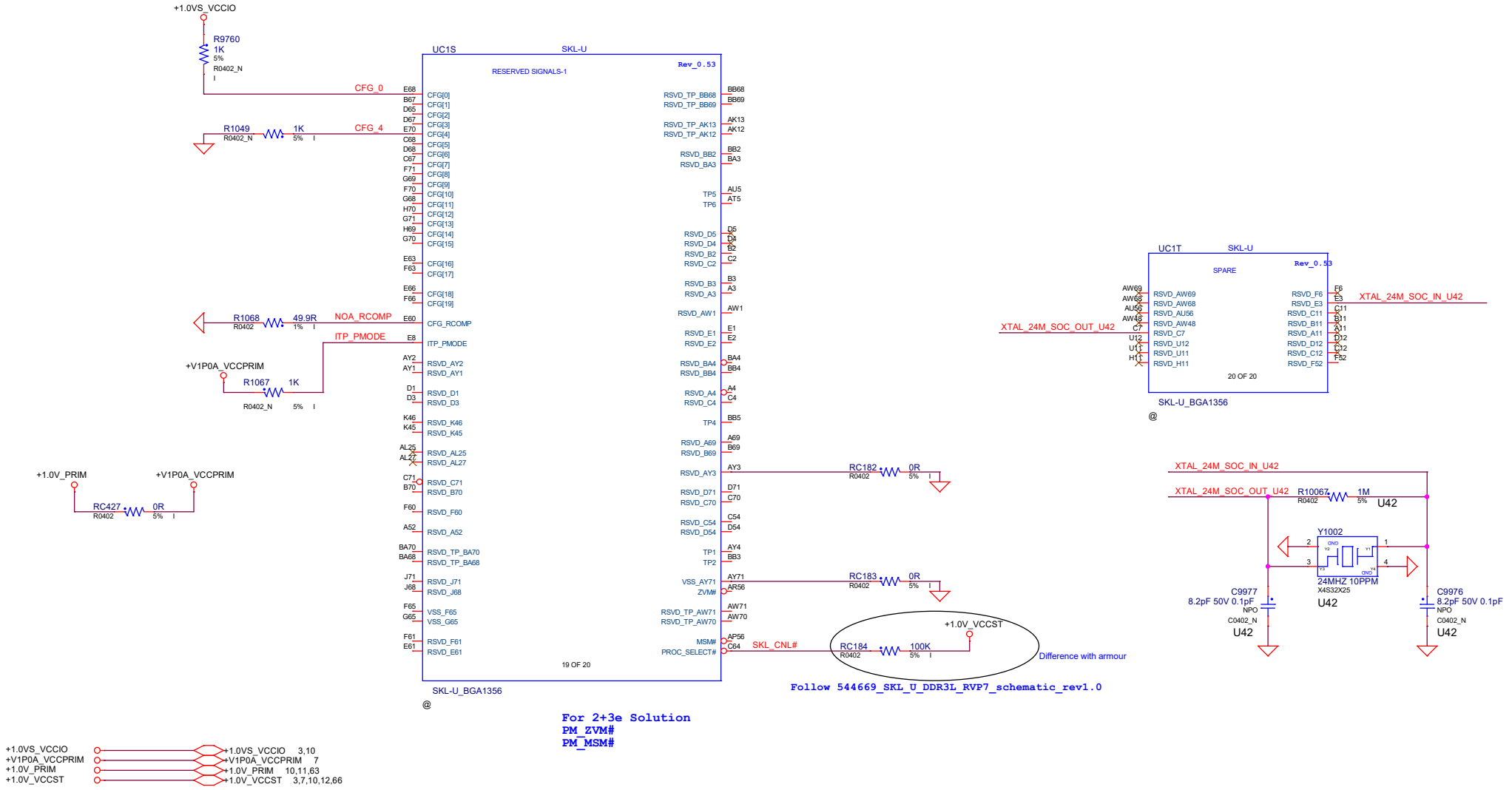
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
V_{CC}_SENSE / V_{SS}_SENSE	100Ω	50Ω	<25 mils
V_{CCGT}_SENSE / V_{SSGT}_SENSE			
V_{CCGTX}_SENSE / V_{SSGTX}_SENSE			
V_{CCSA}_SENSE / V_{SSSA}_SENSE			
V_{CCIO}_SENSE / V_{SSIO}_SENSE[1]		NA	

Note: [1] Does not apply when rails are merged.

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SKL-U(10/12)Power,SVID	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 12 of 69	

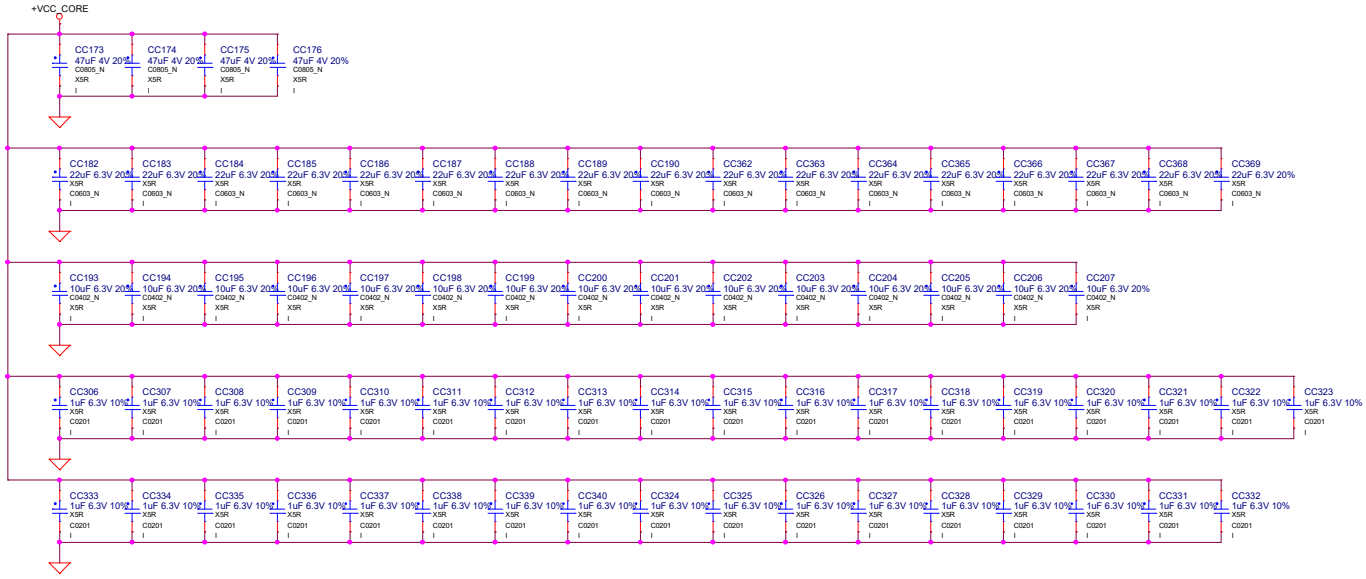


3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SKL-U(11/12)GND	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 13 of 69	



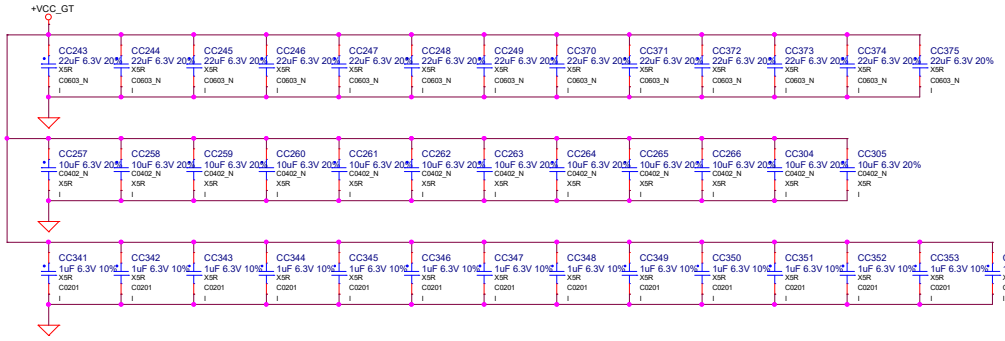
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

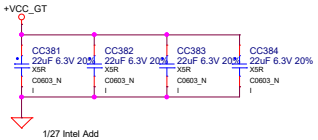
3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SKL-U(12/12)RSVD	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 14 of 69	

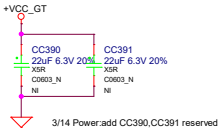


12/30 check PDG
& 220uF pull power side

+VCC_CORE
47uF x8 change 47uF x4
22uF x9 cgange 22uF x17
10uF x15
1uF x35

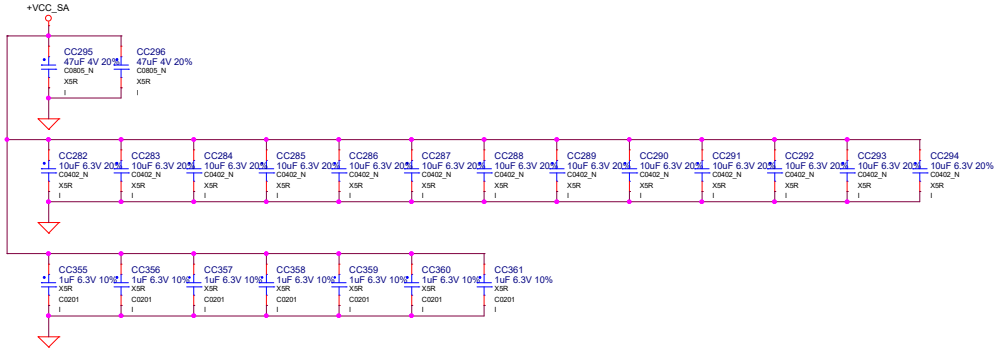


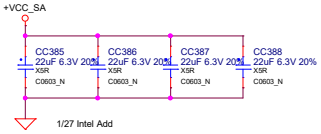




12/30 check PDG
& 220uF pull power side

+VCC_GT
47uF x3 change 47uF x0
22uF x7 cgange 22uF x13
10uF x12
1uF x14





+VCC_SA
47uF x2
10uF x13
1uF x7

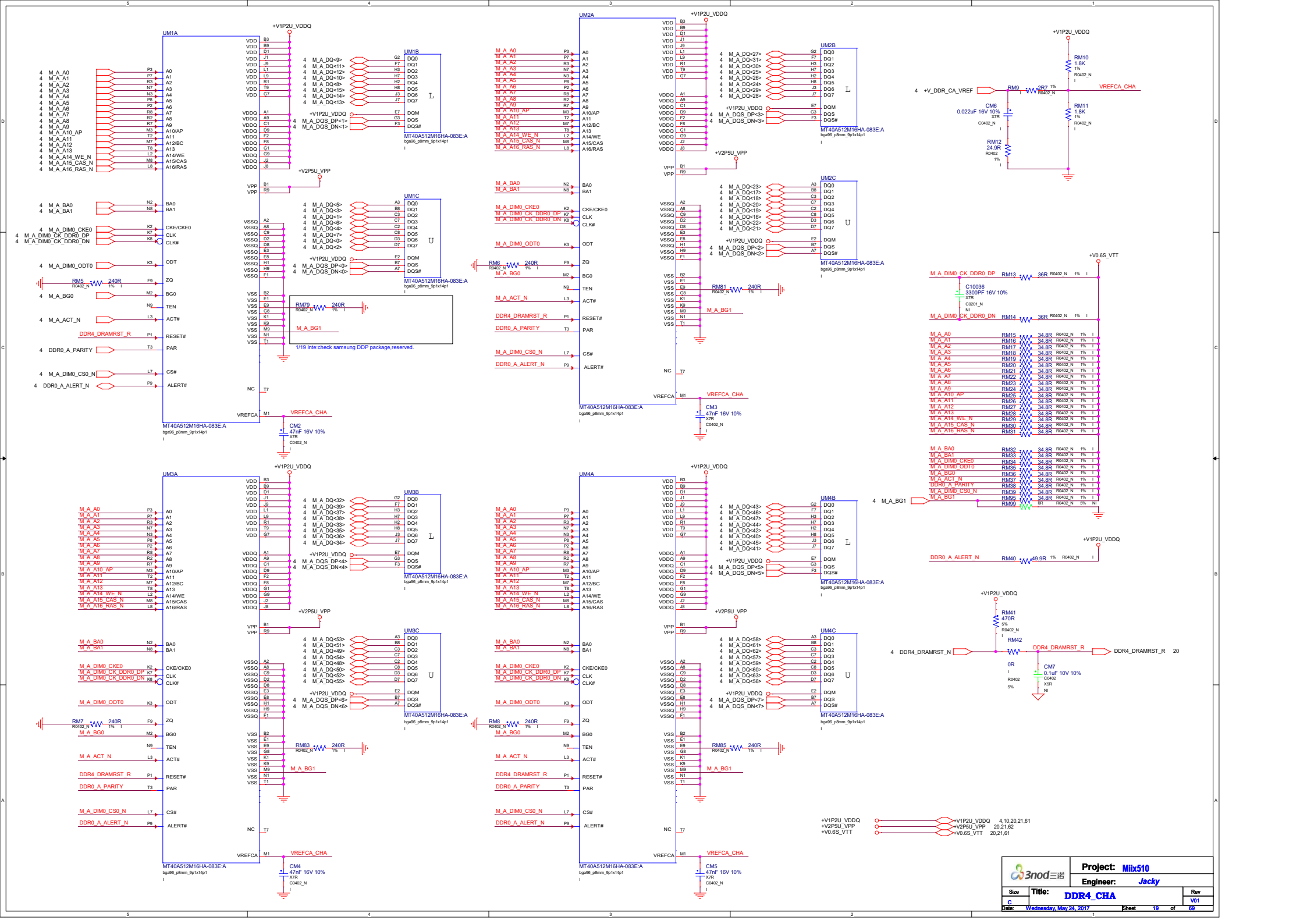
12/30 check PDG

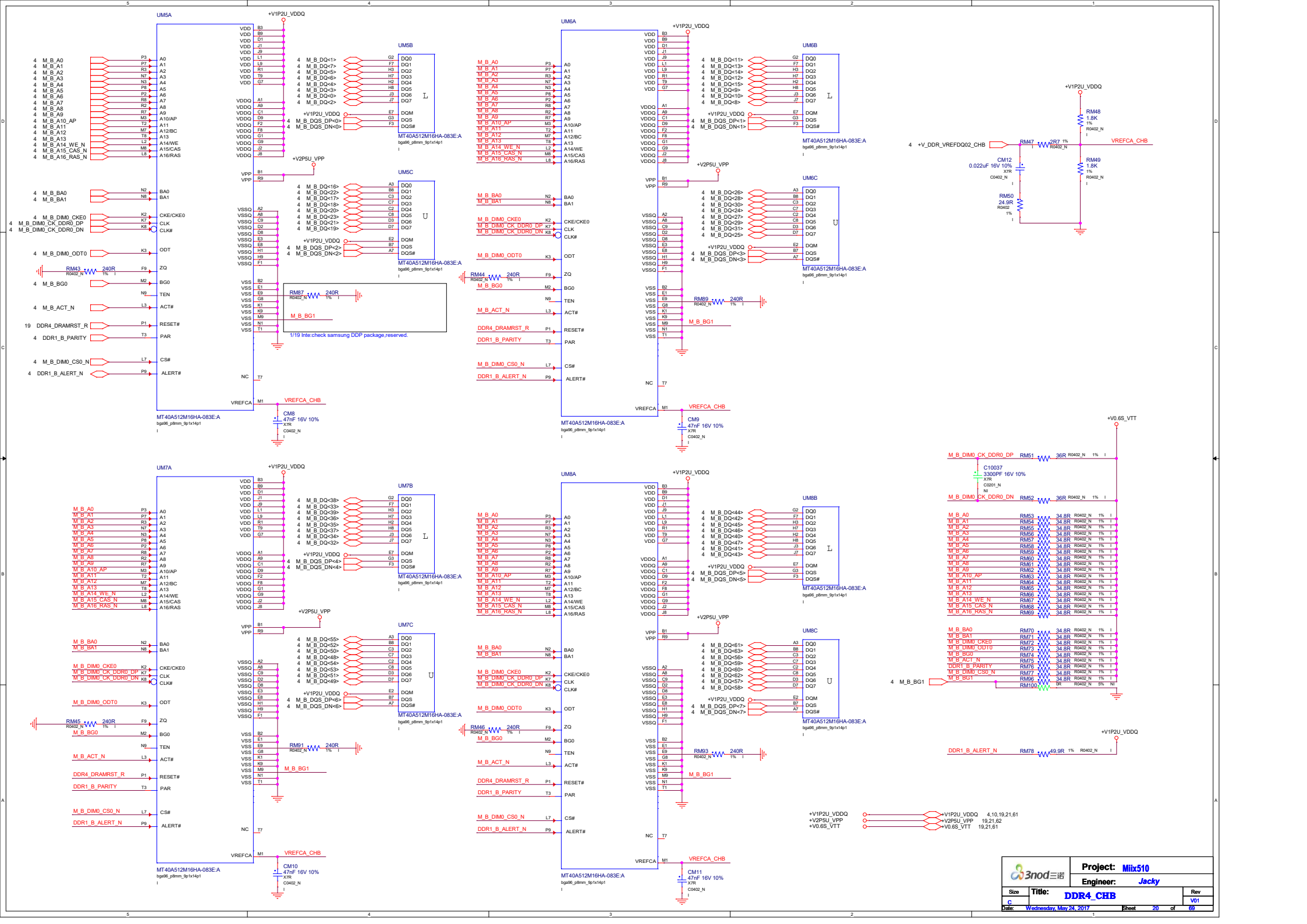
3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: C	Title: SOC (DECOUPLING)	Rev: V01
Date: Thursday, May 25, 2017	Sheet 15 of 69	

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: B	Title: NA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 16 of 69	

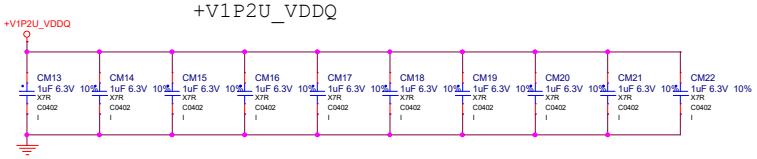
3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: B	Title: NA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 17 of 69	

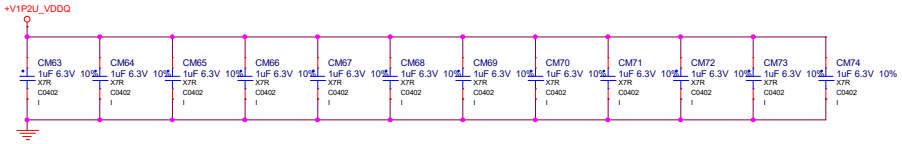
3nod三诺	Project: Miix510	
	Engineer: *Jacky*	
Size: Custom	Title: NA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 18 of 69	

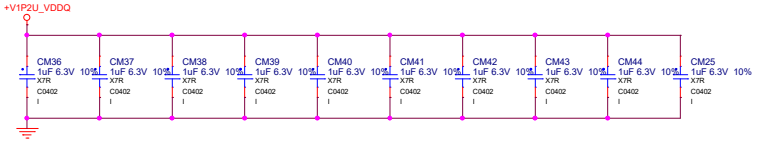

UM1A
UM1B
UM1C
UM2A
UM2B
UM2C
UM3A
UM3B
UM3C
UM4A
UM4B
UM4C
MT40A512M16HA-083E:A
bga96_p8mm_9p1x14p1
+V1P2U_VDDQ
+V2P5U_VPP
+V0.6S_VTT
VREFCA_CHA
1/19 Inte:check samsung DDP package,reserved.
Project: Miix510
Engineer: Jacky
Title: DDR4_CHA
Size: C
Rev: V01
Date: Wednesday, May 24, 2017
Sheet 19 of 69


UM5A
UM5B
UM5C
UM6A
UM6B
UM6C
UM7A
UM7B
UM7C
UM8A
UM8B
UM8C
MT40A512M16HA-083E:A
bga96_p8mm_9p1x14p1
+V1P2U_VDDQ
+V2P5U_VPP
+V0.6S_VTT
+V1P2U_VDDQ 4,10,19,21,61
+V2P5U_VPP 19,21,62
+V0.6S_VTT 19,21,61
VREFCA_CHB
+V_DDR_VREFDQ02_CHB
RM48 1.8K
RM49 1.8K
RM47 2R7
RM50 24.9R
CM12 0.022uF 16V 10%
CM8 47nF 16V 10%
CM9 47nF 16V 10%
CM10 47nF 16V 10%
CM11 47nF 16V 10%
RM43 240R
RM44 240R
RM45 240R
RM46 240R
RM87 240R
RM89 240R
RM91 240R
RM93 240R
M_B_BG1
1/19 Inte:check samsung DDP package,reserved.
C10037 3300PF 16V 10%
RM51 36R
RM52 36R
RM53 34.8R
RM54 34.8R
RM55 34.8R
RM56 34.8R
RM57 34.8R
RM58 34.8R
RM59 34.8R
RM60 34.8R
RM61 34.8R
RM62 34.8R
RM63 34.8R
RM64 34.8R
RM65 34.8R
RM66 34.8R
RM67 34.8R
RM68 34.8R
RM69 34.8R
RM70 34.8R
RM71 34.8R
RM72 34.8R
RM73 34.8R
RM74 34.8R
RM75 34.8R
RM76 34.8R
RM77 34.8R
RM96 34.8R
RM100 0R
RM78 49.9R
DDR1_B_ALERT_N
Project: Miix510
Engineer: Jacky
Title: DDR4_CHB
Size: C
Rev: V01
Date: Wednesday, May 24, 2017
Sheet 20 of 69

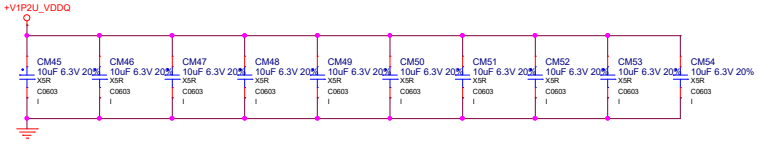
+V1P2U_VDDQ







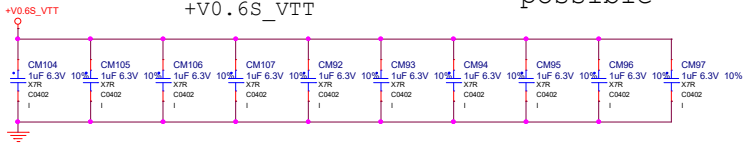
1uF:4 as near each x16 DRAM device as possible

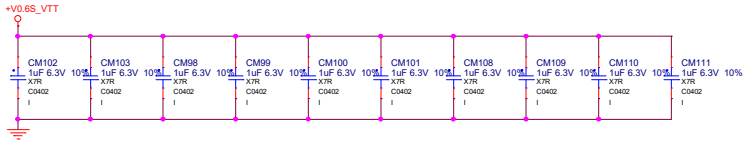


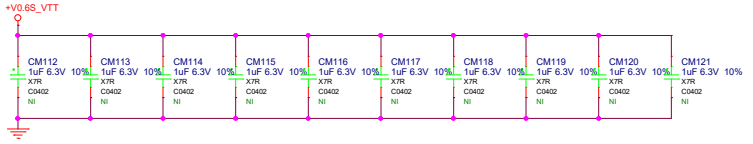
10uF:Distributed around the DRAM devices

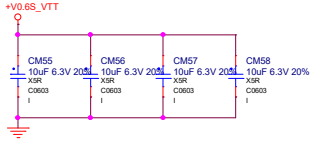
1uF:2 as near each x20 DRAM device as possible

+V0.6S_VTT



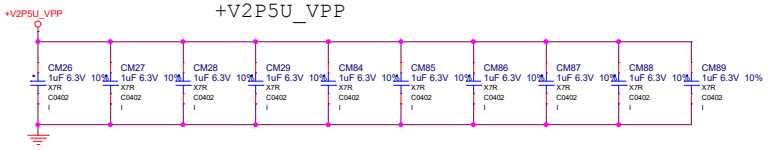


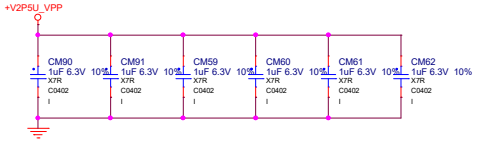




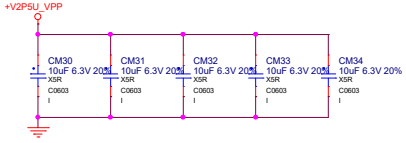
10uF:Distributed around the DRAM devices

+V2P5U_VPP





1uF:2 as near each x16 DRAM device as possible



10uF:Distributed around the DRAM devices

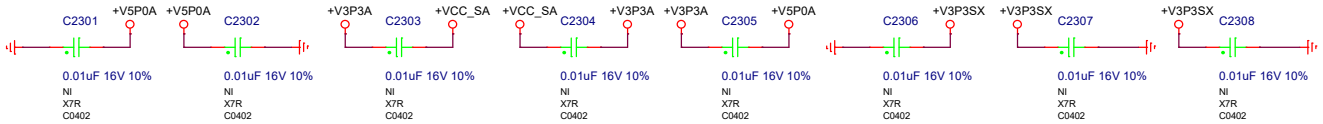
3nod三诺	Project: Mlix510	
	Engineer: Jacky	
Size: C	Title: DDR4 Decoupling	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 21 of 69	

3nod三诺	Project: Miix510	
	Engineer: *Jacky*	
Size: Custom	Title: NA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 22 of 69	

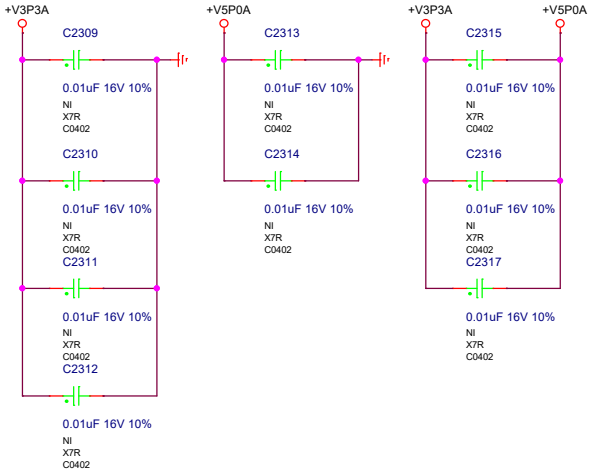
RF Solution

EMC Solution

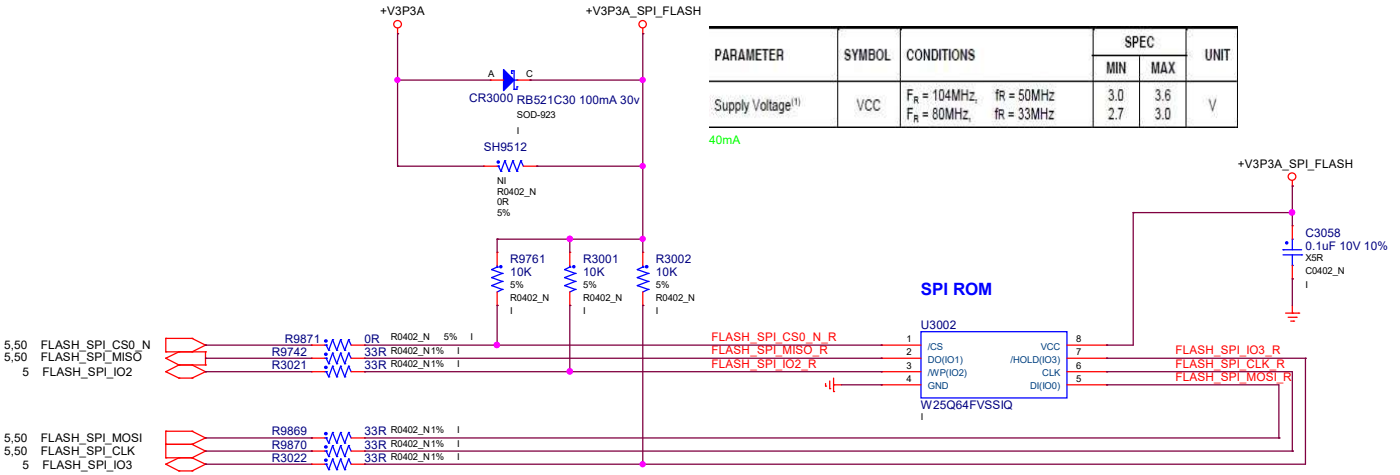
1/26 EMC reserved



5/16 EMC reserved



3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: RF / EMC Solution	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 23 of 69	



PARAMETER	SYMBOL	CONDITIONS	SPEC MIN	SPEC MAX	UNIT
Supply Voltage(1)	VCC	F_R = 104MHz, fR = 50MHz	3.0	3.6	V
		F_R = 80MHz, fR = 33MHz	2.7	3.0	

40mA

Difference with ARMOUR
Series-resistor 0R change to 33R

CIS ok
2/24 SIV:Delet ROM Socket @U3002

Difference with ARMOUR
U3002 package DFN8 change to SOP8

+V3P3A
+V3P3A_SPI_FLASH
+V3P3A 3,4,5,6,7,9,10,11,23,29,31,37,38,42,47,49,50,51,52,53,56,60,62,65,66,67
+V3P3A_SPI_FLASH 50

INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SYSTEM FLASH	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 24 of 69	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: EMMC	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 25 of 69	

M.2 SSD Module

1.4A @ADATA 128GB SSD
2.6A @ADATA 256GB SSD

+V3P3SX → +V3P3SX 5,6,7,9,10,23,30,31,36,37,38,39,40,41,43,44,45,46

+V3P3SX — SH4200 — +V3P3A_SSD

0R I R0805_N 5%

Change SH4200 0805 shunt to resistor

+V3P3A_SSD

C4209	C4204	C4205	C4206	C4207	C4208
22uF 6.3V 20%	22uF 6.3V 20%	0.1uF 10V 10%	0.1uF 10V 10%	0.1uF 10V 10%	0.1uF 10V 10%
X5R	X5R	X5R	X5R	X5R	X5R
C0603_N	C0603_N	C0402_N	C0402_N	C0402_N	C0402_N
I	I	I	I	I	I

CIS ok

JSSD1

1	GND_1	3.3V_2	2
3	GND_3	3.3V_4	4
5	PERn3	Reserved_6	6
7	PERp3	Reserved_8	8
9	GND_9	DAS/DSS# (O)(OD)	10
11	PETn3	3.3V_12	12
13	PETp3	3.3V_14	14
15	GND_15	3.3V_16	16
17	PERn2	3.3V_18	18
19	PERp2	Reserved_20	20
21	GND_21	Reserved_22	22
23	PETn2	Reserved_24	24
25	PETp2	Reserved_26	26
27	GND_27	Reserved_28	28
29	PERn1	Reserved_30	30
31	PERp1	Reserved_32	32
33	GND_33	Reserved_34	34
35	PETn1	Reserved_36	36
37	PETp1	DEVSLP (I)(0/3.3V)	38
39	GND_39	Reserved_40	40
41	PERn0/SATA-B+	Reserved_42	42
43	PERp0/SATA-B-	Reserved_44	44
45	GND_45	Reserved_46	46
47	PETn0/SATA-A-	Reserved_48	48
49	PETp0/SATA-A+	PERST# (I)(0/3.3V)	50
51	GND_51	CLKREQ# (IO)(0/3.3V)	52
53	REFCLKN	PEWake# (IO)(0/3.3V)	54
55	REFCLKP	Reserved_56	56
57	GND_57	Reserved_58	58
	Key M		
67	NC32	SUSCLK(32kHz) (I)(0/3.3V)	68
69	PEDET (OC-PCIe)	3.3V_70	70
71	GND_71	3.3V_72	72
73	GND_73	3.3V_74	74
75	GND_75		
76	GND12		
77	GND13		
78	NC1		
79	NC2		

9 PCIE9_SSD_RX_DN
9 PCIE9_SSD_RX_DP
9 PCIE9_SSD_TX_DN_C
9 PCIE9_SSD_TX_DP_C
9 PCIE10_SSD_RX_DN
9 PCIE10_SSD_RX_DP
9 PCIE10_SSD_TX_DN_C
9 PCIE10_SSD_TX_DP_C
9 PCIE11_SSD_RX_DN
9 PCIE11_SSD_RX_DP
9 PCIE11_SSD_TX_DN_C
9 PCIE11_SSD_TX_DP_C
9 PCIE12_SSD_RX_DP
9 PCIE12_SSD_RX_DN
9 PCIE12_SSD_TX_DN_C
9 PCIE12_SSD_TX_DP_C
7 PCIE_REFCLK_SSD_DN
7 PCIE_REFCLK_SSD_DP

R4200 0R R0402_N 5% I PCIE12_SSD_RX_DP_R
R4201 0R R0402_N 5% I PCIE12_SSD_RX_DN_R

PCIE12 RX follow intel CRB

Difference with armour
SSD interface SATA change to PCIE
If install SATA CARD,R4200,R4201 need install 0.01uF
C0606,C0607 need install 0.01uF

NGFF SSD module interface	PCIE	SATA
Reference	R4200,R4201 install 0ohm C0606,C0607 install 0.22uF	R4200,R4201 install 0.01uF C0606,C0607 install 0.01uF
Detect pin	R1050 install 10Kohm R1087 uninstall 100Kohm	R1050 uninstall 10Kohm R1087 install 100Kohm

Default

3/16 Add SSD(PCIE or SATA) BOM option table

Pin69
PICE module spec is N/C
SATA module spec is GND

+V3P3A_SSD

SATA2_DEVSLP 9

SSD_CLK_REQ_N_R
M.2_SSD_PE_WAKE_N

R4206 0R R0402_N5% I
R4205 0R R0402_N 5% NI

+V3P3A_SSD
R4207 10K 5% R0402_N I

1/4 Add R4206 PU

PLT_RST_N 7,41,43,45,50
SSD_CLK_REQ_N 7
PCIE_WAKE_PCH_N 7

Pin54
PICE module spec is N/C
SATA module spec is N/C

PM_SUSCLK_SSD
TP9980

Pin68
PICE module spec is N/C
SATA module spec is N/C

Co-lay PCIE12 RX, reserved R4202, R4203
please close to R4200, R4201

3/9 Del R4202,R4203,don't Co-lay PCIE12 RX

51747-07502-112

INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.+V3P3.26
Wed Jun 03 11:22:52 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: PCIE SSD MODULE	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 26 of 69	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:53 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: MICRO-SD CARD	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 27 of 69	

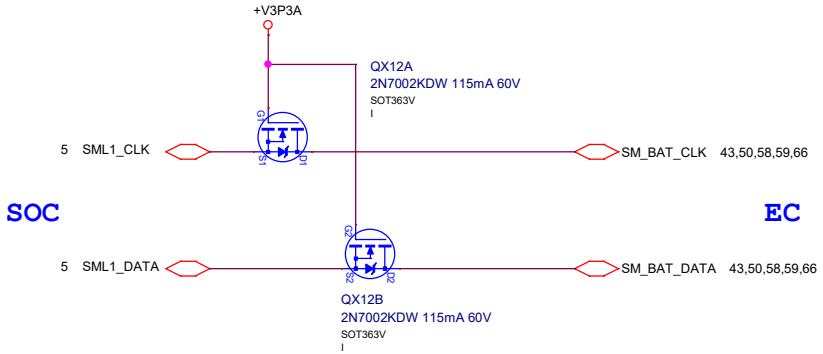
<XR_PAGE_TITLE>

INTERNAL ONLY

BPAGE DRAWING

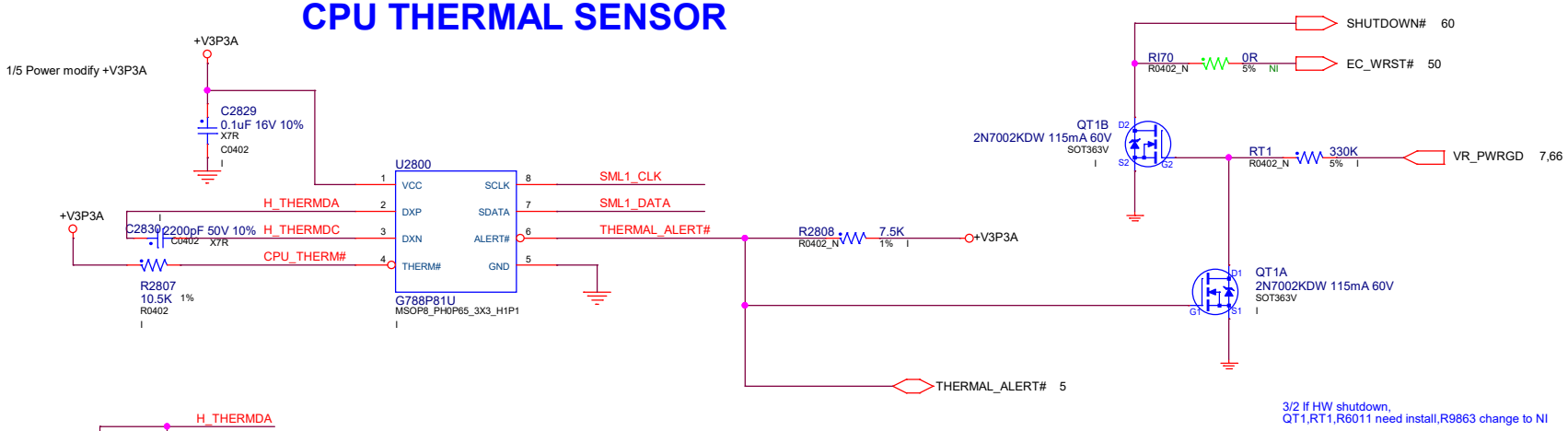
sky_y_mrd.GND
Wed Jun 03 11:22:53 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SD CARD POWER	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 28 of 69	



1/4 Add connect to SOC & EC

CPU THERMAL SENSOR



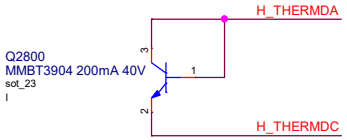


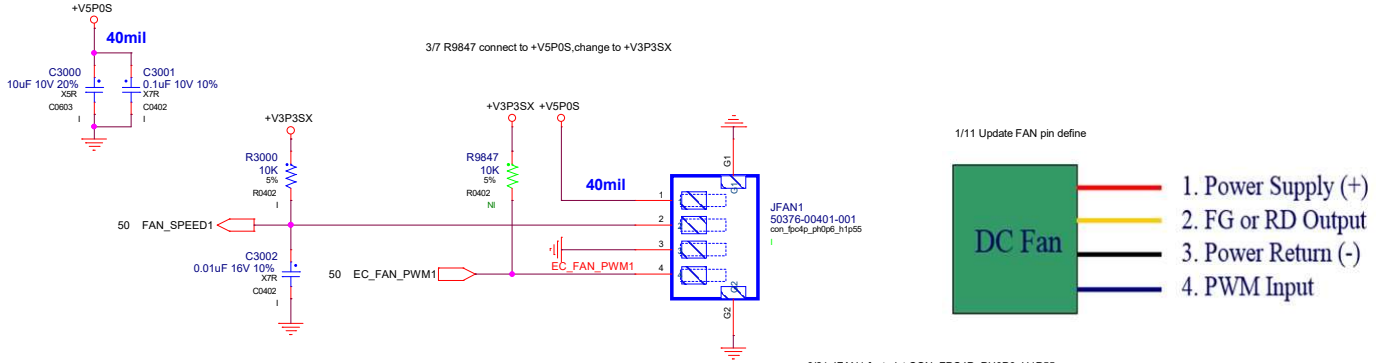
Table 10. Remote temperature $\overline{\text{THERM}}$ limit

The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

+V3P3A +V3P3A 3,4,5,6,7,9,10,11,23,24,31,37,38,42,47,49,50,51,52,53,56,60,62,65,66,67

3nod三诺	Project:	Miix510	
	Engineer:	Jacky	
Size: B	Title:	CPU THERMAL SENSOR	Rev: V01
Date:	Wednesday, May 24, 2017	Sheet 29 of 69	



FAN conn

6/21 JFAN1 footprint CON_FPC4P_PH0P6_H1P55
change to con_wtb_4p_ph0p6_h1p55_50376

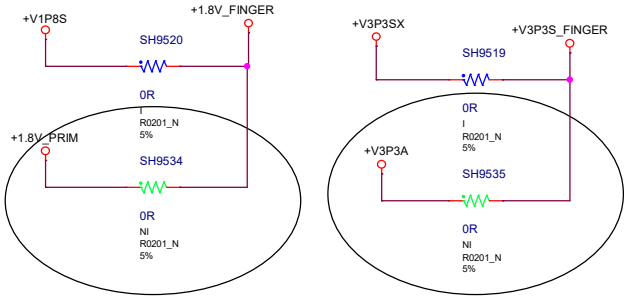
CIS ok

+V5P0S
+V3P3SX

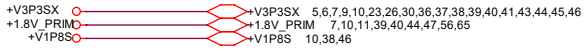
+V5P0S 10,46
+V3P3SX 5,6,7,9,10,23,26,31,36,37,38,39,40,41,43,44,45,46

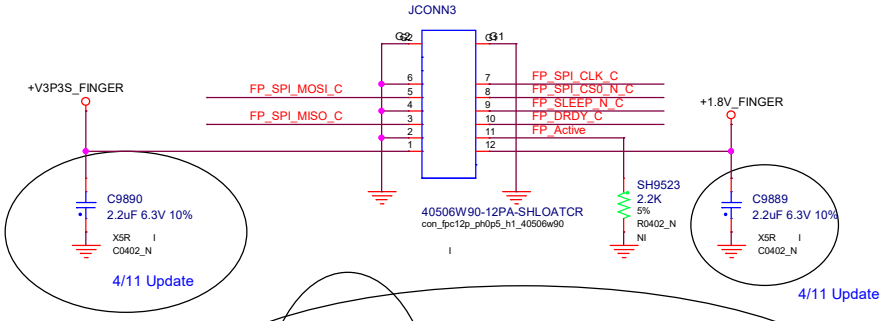
3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: FAN conn	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 30 of 69	

Fingerprint



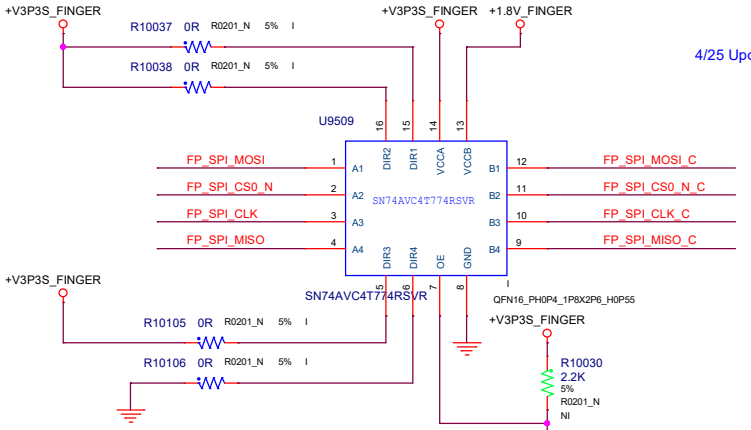
4/11 Support micro stanby function



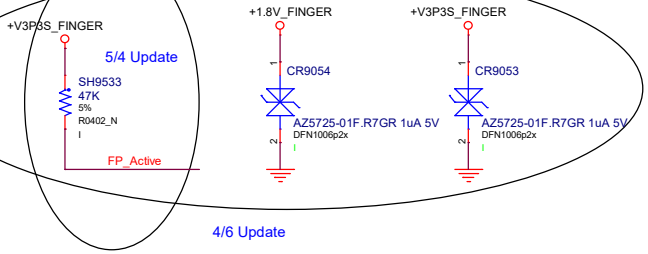


4/11 Update

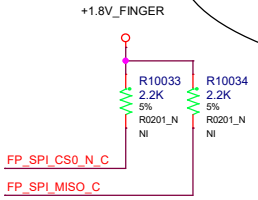
4/11 Update

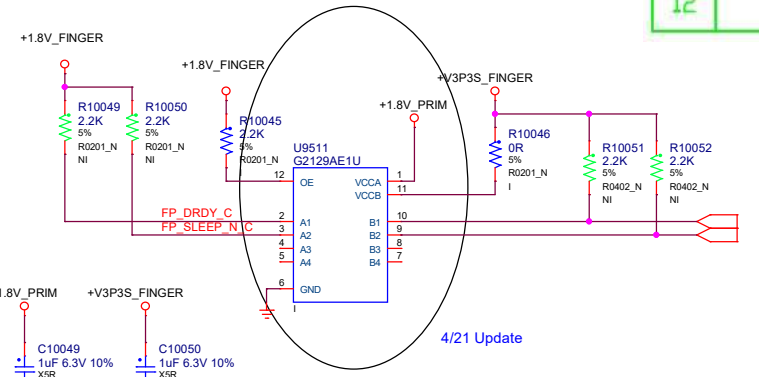


4/25 Update

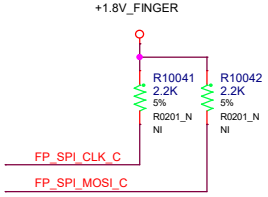


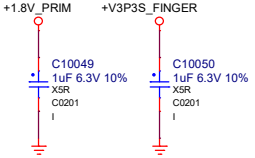
4/6 Update

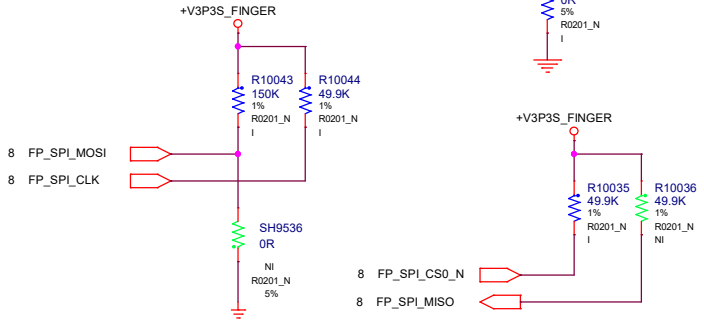




4/21 Update







PIN define	
1	3.3VCC
2	GND
3	MISO
4	GND
5	MOSI
6	GND
7	CLK
8	CS0_N
9	SLEEP_N
10	DRDY
11	FP_ACTIVE
12	1.8VCC

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: FIngerprint	Rev: V01
Date: Thursday, May 25, 2017	Sheet 31 of 69	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.32
Wed Jun 03 11:22:55 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: NA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 32 of 69	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V1P0.33
Wed Jun 03 11:22:55 2015

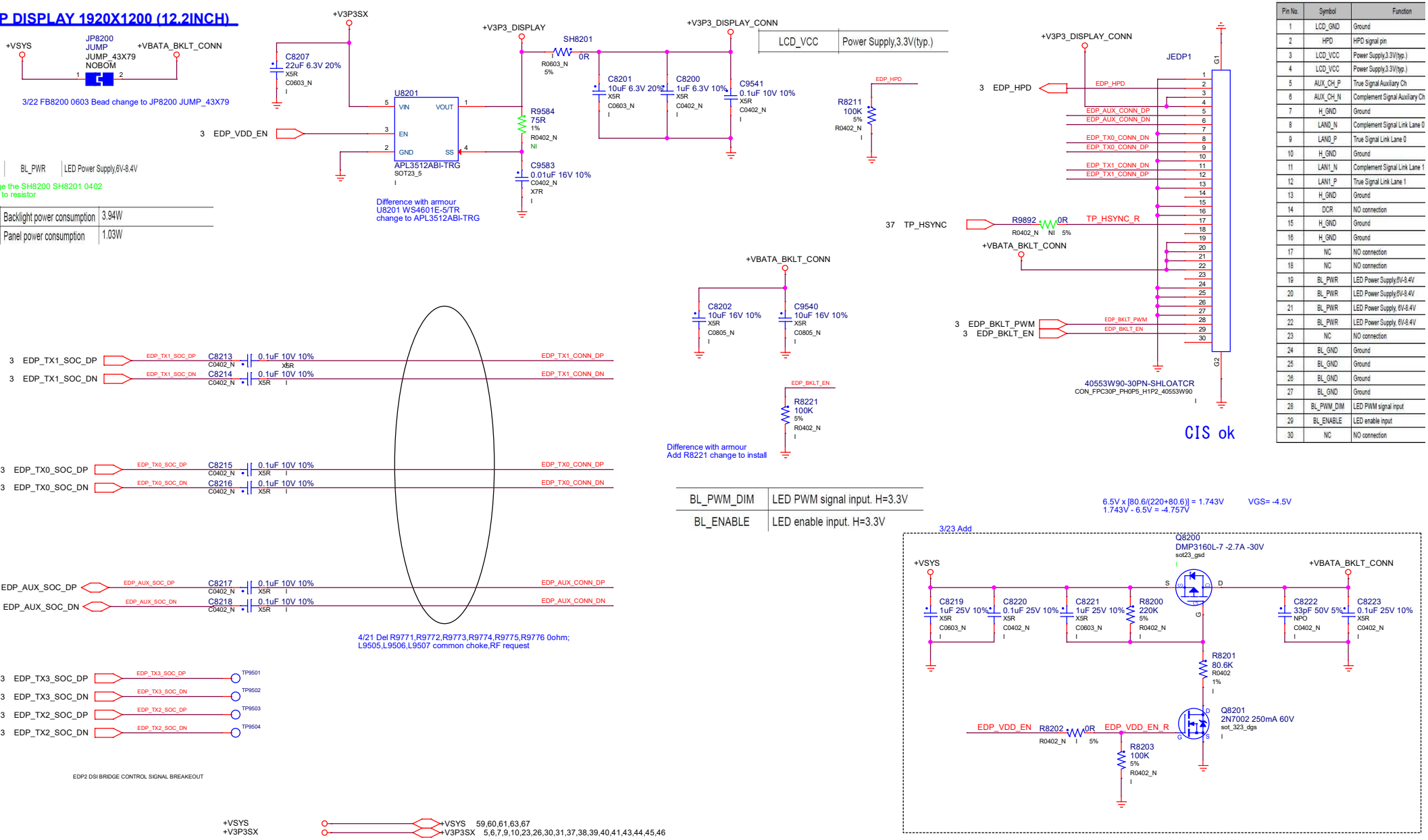
3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: NA	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 33 of 69	

Wed Jun 03 11:22:56 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: HDMI LEVEL SHIFTERS	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 34 of 69	

3nod三诺	Project:	LENOVO_NB116BT
	Engineer:	Jason
Size: Custom	Title:	Sensor & HUB
		Rev: V01
Date: Wednesday, May 24, 2017	Sheet 35 of 69	

EDP DISPLAY 1920X1200 (12.2INCH)



Interface Pin Connection

Pin No.	Symbol	Function
1	LCD_GND	Ground
2	HPD	HPD signal pin
3	LCD_VCC	Power Supply,3.3V(typ.)
4	LCD_VCC	Power Supply,3.3V(typ.)
5	AUX_CH_P	True Signal Auxiliary Ch
6	AUX_CH_N	Complement Signal Auxiliary Ch
7	H_GND	Ground
8	LAN0_N	Complement Signal Link Lane 0
9	LAN0_P	True Signal Link Lane 0
10	H_GND	Ground
11	LAN1_N	Complement Signal Link Lane 1
12	LAN1_P	True Signal Link Lane 1
13	H_GND	Ground
14	DCR	NO connection
15	H_GND	Ground
16	H_GND	Ground
17	NC	NO connection
18	NC	NO connection
19	BL_PWR	LED Power Supply,6V-8.4V
20	BL_PWR	LED Power Supply,6V-8.4V
21	BL_PWR	LED Power Supply, 6V-8.4V
22	BL_PWR	LED Power Supply, 6V-8.4V
23	NC	NO connection
24	BL_GND	Ground
25	BL_GND	Ground
26	BL_GND	Ground
27	BL_GND	Ground
28	BL_PWM_DIM	LED PWM signal input
29	BL_ENABLE	LED enable input
30	NC	NO connection

3nod三诺	Project:	Miix510	
	Engineer:	Jacky	
Size: Custom	Title:	DISPLAY	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 36 of 69		

Touch & Docking

Touch Connector

+V3P3SX — SH8202 0R R0603_N 5% — +V3P3SX_TOUCH

+V3P3SX_TOUCH
- C8205 0.1uF 10V 10% X5R C0402_N
- C8206 4.7uF 6.3V 20% X5R C0402_N

3/18 Add R8212 PU +V3P3SX_TOUCH

+V3P3SX_TOUCH
- R8212 2.2K 5% R0402_N
- R8209 2.2K 5% R0402_N
- R8210 2.2K 5% R0402_N

CIS ok

		JTP1
36	TP_HSYNC	1
3	TOUCH_PANEL_INT_N	2
8	TOUCH_I2C_SDA	3
8	TOUCH_I2C_CLK	4
3	TOUCH_PANEL_RESET_N	5
		6
		7
		8
		9
		10
		G1 G1 G2 G2

40536W90-10PN-SHLOATCR
CON_FPC10P_PH0P5_H1P2_40536W90

+V3P3SX_TOUCH

TP9933	TOUCH_I2C_CLK
TP9934	TOUCH_I2C_SDA
TP9935	TOUCH_PANEL_RESET_N
TP9936	TOUCH_PANEL_INT_N
TP9937	TP_HSYNC
TP9987	
TP9939	

+V3P3SX	+V3P3SX	5,6,7,9,10,23,26,30,31,36,38,39,40,41,43,44,45,46
+V3P3A	+V3P3A	3,4,5,6,7,9,10,11,23,24,29,31,38,42,47,49,50,51,52,53,56,60,62,65,66,67
+V5P0A	+V5P0A	10,11,23,39,40,42,53,60,61,62,63,65

Docking Connector

+V5P0_DOCK

CIS ok

9	USB2_P5_DOCK_DN	R8205 0R R0402_N NI 5%	USB2_P5_DOCK_CONN_DN
9	USB2_P5_DOCK_DP	R8206 0R R0402_N NI 5%	USB2_P5_DOCK_CONN_DP

CO-CH_L4_PH0P8_H1_AB — L8202 67ohm 320mA +-25% NI

GND_DET

	JDOCK1
	1
	2
	3
	4
	5
	6
	7
	8
	G1 G1 G2 G2

40506W90-8PA-SHLOATCR
CON_FPC8P_PH0P5_H1P2_50696

+V5P0_DOCK

TP9941	
TP9943	USB2_P5_DOCK_CONN_DN
TP9944	USB2_P5_DOCK_CONN_DP
TP9945	GND_DET
TP9946	

6/21 JDOCK1 footprint CON_FPC8P_PH0P5_H1P2_50696
change to con_fpc8p_ph0p5_h1_40506w90

+V3P3A
- R8223 470k 1% R0402_N
- R8204 470k 1% R0402_N
- C8203 1uF 16V 10% X5R C0402_N

+V5P0A +V3P3A
- R9879 470k 1% R0402_N

8,50 DOCK_DET

Q8202 2N7002 250mA 60V sot_323_dgs — GND_DET

DOCK_DET — R9830 0R R0402_N NI 5%

U8200 WS4601E-5/TR sot_23_5

+V5P0A_USB_DOCK
- C8204 1uF 16V 10% X5R C0402_N
- C9569 0.1uF 10V 10% X5R C0402_N

+V5P0_DOCK — SH8203 0R R0603_N 5%

1/4 Modify schematic

8	DOCK_DET_SOC	R9880 0R R0402_N	DOCK_DET_SOC_R
6,50	ME_Flash_EN	R9881 0R R0402_N NI	ME_Flash_EN_R

D8200 BAT54A 200mA 30V SOT_23

3/2 ME_Flash_EN connect to R9881

5/23 R9881 uninstall,BIOS request

USB2_P5_DOCK_CONN_DP
USB2_P5_DOCK_CONN_DN
+V5P0_DOCK
GND_DET

CR9043	DFN1006p2x	AZ5725-01F.R7GR 1uA 5V
CR9042	DFN1006p2x	AZ5725-01F.R7GR 1uA 5V
CR9046	DFN1006p2x	AZ5725-01F.R7GR 1uA 5V
CR9047	DFN1006p2x	AZ5725-01F.R7GR 1uA 5V

3/14 EMC:add CR9046,CR9047 reserved
5/12 EMC:CR9046,CR9047 install

INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.+V3P3.37
Wed Jun 03 11:22:57 2015

3nod三诺	Project:	Miix510
	Engineer:	Jacky
Size: Custom	Title:	TOUCH PANEL AND DOCK
	Rev:	V01
Date: Wednesday, May 24, 2017	Sheet 37 of 69	

Sensors

+V1P8S → +V1P8S 10,31,46

+V3P3SX → +V3P3SX 5,6,7,9,10,23,26,30,31,36,37,39,40,41,43,44,45,46

ACCELEROMETER sensor

+V3P3SX — SH8000 0R I R0603_N 5% — +V3P3A_SENSOR

U8003 (BMA222E, bma250e, NI)

8 TP_I2C0_SDA_EDP2DSI — TP_I2C0_SDA_EDP2DSI — SH9521 0R R0402_N 5% NI — I2C_SDA
8 TP_I2C0_SCL_EDP2DSI — TP_I2C0_SCL_EDP2DSI — SH9522 0R R0402_N 5% NI — I2C_CLK

8 ACCEL_INT — ACCEL_INT — TP8001 — INT1_N / INT2_N

CSB — NC — I2C_address

Vddio — Vddio_i2c — Vdd — GND1 — GND2

+V3P3A_SENSOR — C8004 0.1uF 10V 10% X5R C0402_N NI — Vddio

+V3P3A_SENSOR — C8009 0.1uF 10V 10% X5R C0402_N NI — Vdd

ACCEL I2C ADDR: 0X18

+V3P3A_SENSOR — R8004 2.2K 5% R0402_N NI — TP_I2C0_SDA_EDP2DSI

+V3P3A_SENSOR — R8005 2.2K 5% R0402_N NI — TP_I2C0_SCL_EDP2DSI

+V3P3A_SENSOR — R8006 10K 5% R0402_N NI — I2C_address

R8007 0R R0402_N 5% NI — GND1

Difference with armour
Add R8006 reserve 10K PU
Add R8007 0ohm PD

1/18 RF CS2 change to CS0

IMU sensor BMI055(A+G)

+V3P3A_SENSOR — R8019 10K 5% R0402_N I — IMU_I2C_SCL_HUB 8

+V3P3A_SENSOR — R8018 10K 5% R0402_N I — IMU_I2C_SDA_HUB 8

from Intel ISH Bus

U8005 (BMI055, I)

PS — GNDIO — CSB2 — GNDA — VDD — NC — INT2

SCx — SDx — SDO2 — VDDIO — INT3 — INT4 — CSB1 — SDO1 — INT1

+V3P3A_SENSOR — C9979 0.1uF 10V 10% X5R C0402_N I — GNDA

+V3P3A_SENSOR — C9978 0.1uF 10V 10% X5R C0402_N I — VDDIO

+V3P3A_SENSOR — R8024 10K 5% R0402_N I — INT3

R8023 10K 5% R0402_N I — INT4

IMU_INT3 8
IMU_INT4 8

Gyro

+V3P3A_SENSOR — R8021 10K 5% R0402_N I — INT2

R8022 10K 5% R0402_N I — INT1

Accel

8 IMU_INT2
8 IMU_INT1

LID Sensor

+V3P3A — CR9041 RB521C30 100mA 30V SOD-923 I — +V3P3A_LID

C8003 0.1uF 10V 10% X5R C0402_N I

U8001 (BU52012HFV, HVSOF5, I)

NC0 — GND — NC1 — VDD — OUT

R8000 47K 5% R0402_N I — LID_INT_N — LID_INT_N 8,47,50

C8011 100pF 50V 5% NPO C0402_N I

TP_3V3 / U3 (IQS231A)

TP_3V3 — R8011 100K 5% R0402_N NI — R8013 100K 5% R0402_N 231A — R8015 100K 5% R0402_N NI

C7155 1uF 6.3V 10% X7R C0402_N I — C7153 100pF 50V 5% NPO C0402_N I

R8012 100K 5% R0402_N 229 — R8014 100K 5% R0402_N NI — R8016 100K 5% R0402_N 229

U3 (IQS231A, dfn10_ph0p5_3x3_h1_g1)

VDDHI — CX — NC3 — NC1 — IO2/SDA — NC2

VREG — NC4 — IO1/SCL — VSS — EPAD

+VREG — C7156 1uF 6.3V 10% X7R C0402_N I — C7154 100pF 50V 5% NPO C0402_N I

TP_3V3 — R8017 100K 5% R0402_N 229 — MODEM_SAR_3P3

R9037 1M 5% R0402_N 229

TP_3V3 — R8009 4.7K 5% R0402_N 231A

+V1P8S — R8010 100K 5% R0402_N I — MODEM_SAR_1P8 44

Q3800 BSS138 300mA 50V sot23_gsd I

G2129TL1U change MOS

+V3P3SX — SH8001 0R I R0603_N 5% — TP_3V3

R9023 1K R0402_N 5% I

R9024 0R R0402_N 5% I — RFE_50_ANT_MAIN4

C7125 8pF 50V 0.5pF NPO C0402_N NI

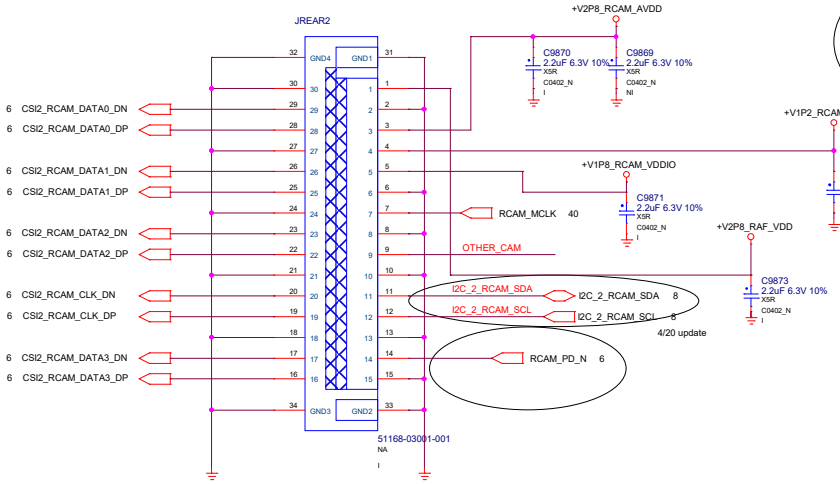
JSAR1 (R0G2-1A7Y1-12004, con_ant4p_2x2_h0p6_20449c6)

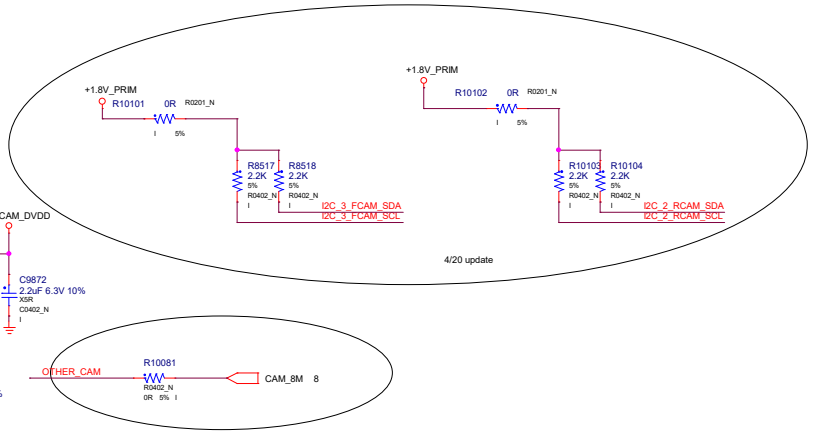
GND_1 — GND_2 — GND_3

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: SENSORS & LID	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 38 of 69	

REAR CAMERA CONNECTOR

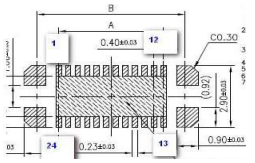
8M OV8858





8M Pin 9 internal is GND

1/18 JREAR1,JFRONT1 change to 24pin



NO	SIGNAL
1	AGND
2	AVDD2.8V
3	DVDD1.2V
4	DOVDD1.8V
5	DGND
6	MCLK
7	NC
8	NC(RESETB)
9	DGND
10	SID_D
11	SID_C
12	DGND
13	XSHUTDOWN
14	DGND
15	MD2_P
16	MD2_N
17	DGND
18	MC_P
19	MC_N
20	DGND
21	MD1_P
22	MD1_N
23	DGND
24	NC

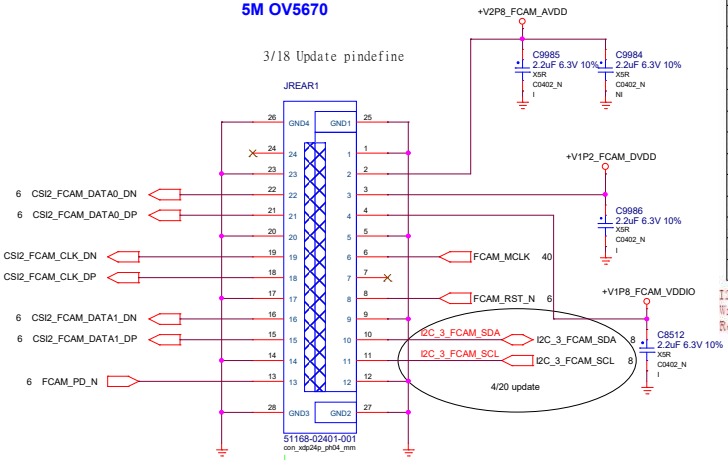
NO	SIGNAL
1	VCM_VDD2.8V
2	VCM_GND
3	AVDD2.8V
4	DVDD1.2V
5	DOVDD1.8V
6	DGND
7	MCLK
8	DGND
9	NC
10	DGND
11	SID_D
12	SID_C
13	DGND
14	XSHUTDOWN
15	DGND
16	MD4_P
17	MD4_N
18	DGND
19	MC_P
20	MC_N
21	DGND
22	MD3_P
23	MD3_N
24	DGND
25	MD2_P
26	MD2_N
27	DGND
28	MD1_P
29	MD1_N
30	DGND

I2C Adress:
Write:0X6C
Read: 0X6D

FRONT CAMERA CONNECTOR

5M OV5670

3/18 Update pindefine

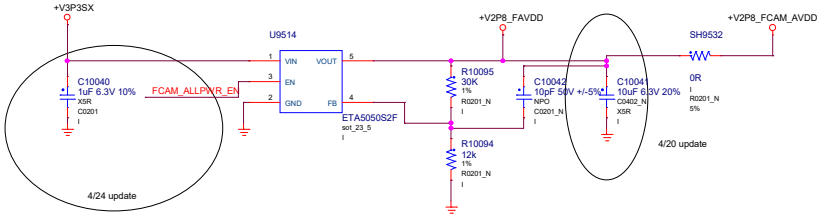


I2C Adress:
Write:0X20
Read: 0X21

CIS ok

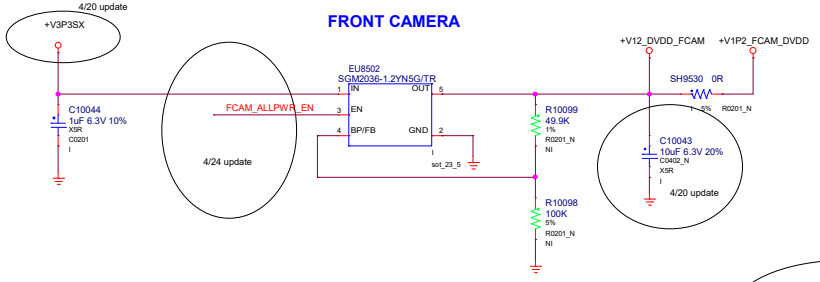
FRONT CAMERA

AVDD_2.8V



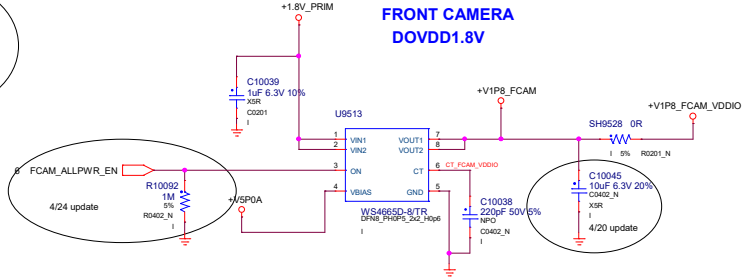
DVDD_1.2V

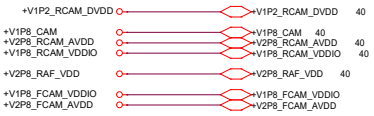
FRONT CAMERA



FRONT CAMERA

DOVDD1.8V



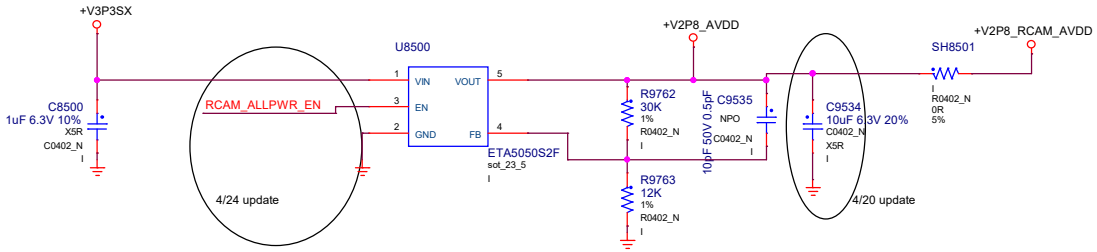


Project:	Mlix510	
Engineer:	Jacky	
Size: C	Title: FRONT AND REAR CAMERA CONN	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 39 of 69	

1/19 Delete DVDD_1.5V

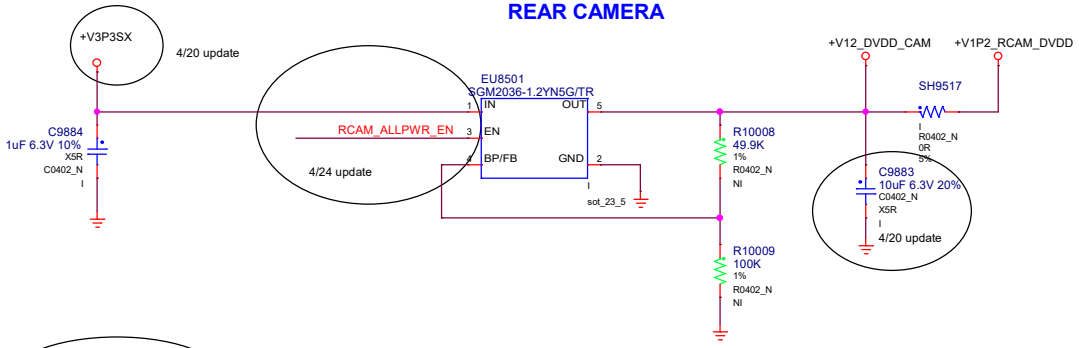
3/18 Add DVDD_1.5V,
Rear camera change to OV5648

AVDD_2.8V REAR CAMERA

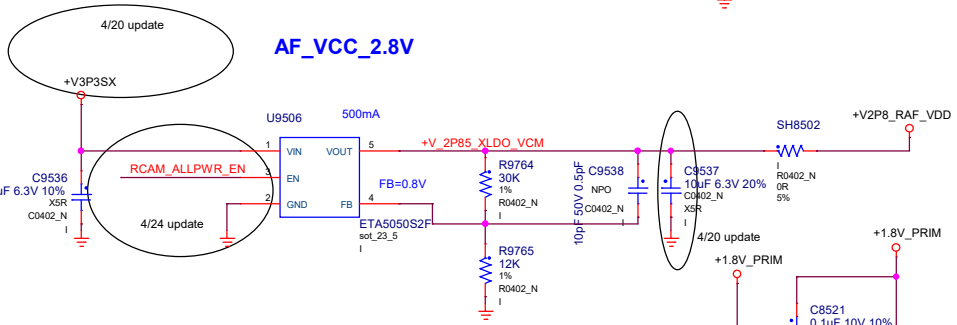


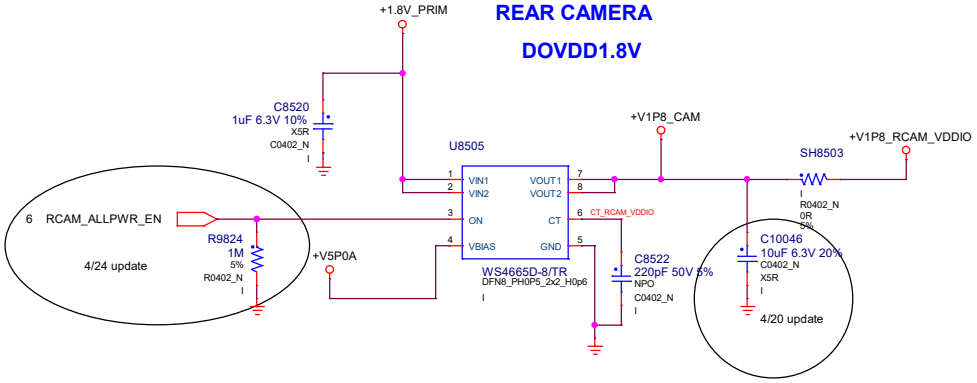
DVDD_1.2V REAR CAMERA

2/18 Add DVDD_1.2V,
Rear camera change to OV8858



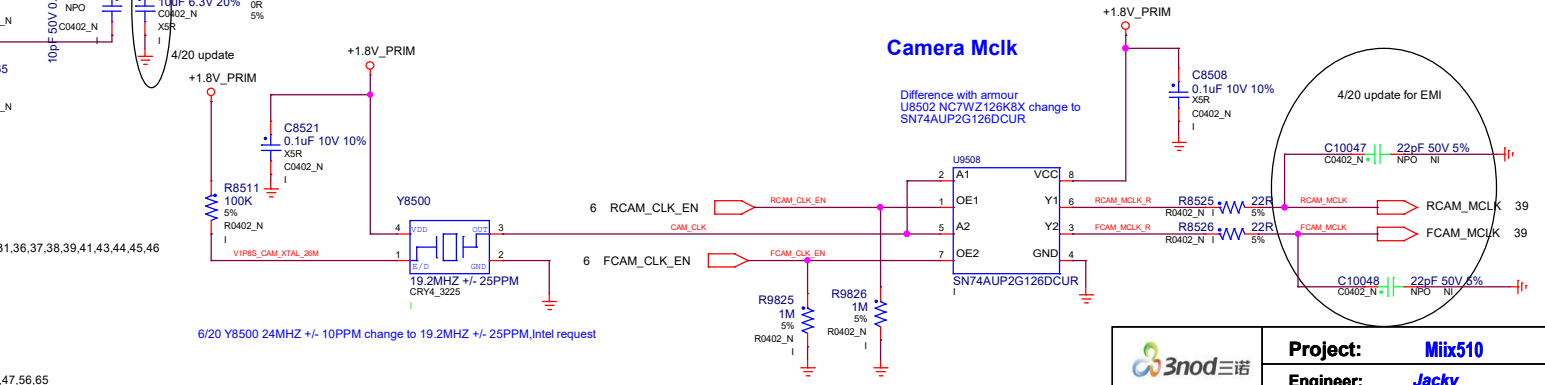
AF_VCC_2.8V





REAR CAMERA DOVDD1.8V

Camera Mclk



6/20 Y8500 24MHZ +/- 10PPM change to 19.2MHZ +/- 25PPM,Intel request

+V1P2_RCAM_DVDD +V1P2_RCAM_DVDD 39

+V3P3SX +V3P3SX 5,6,7,9,10,23,26,30,31,36,37,38,39,41,43,44,45,46
+V1P8_CAM +V1P8_CAM
+V2P8_RCAM_AVDD +V2P8_RCAM_AVDD 39
+V2P8_FCAM_AVDD +V2P8_FCAM_AVDD 39

+V2P8_AF_VDD +V2P8_AF_VDD

+1.8V_PRIM +1.8V_PRIM 7,10,11,31,39,44,47,56,65
+V5P0A +V5P0A 10,11,23,37,39,42,53,60,61,62,63,65
+V1P8_RCAM_VDDIO +V1P8_RCAM_VDDIO 39
+V1P8_FCAM_VDDIO +V1P8_FCAM_VDDIO 39

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: CAMERA DISCRETE CONTROL LOGIC	Rev: V01
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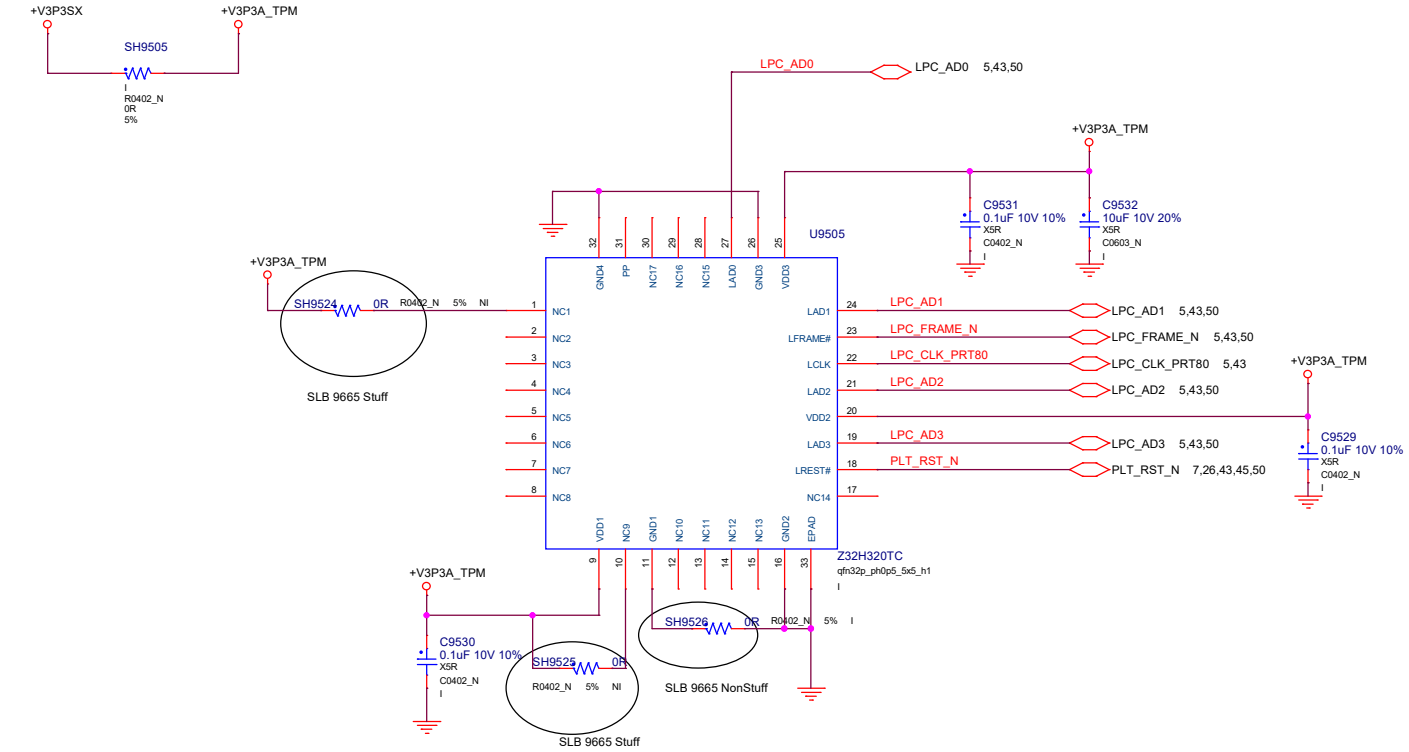
TPM 2.0



INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.41
Wed Jun 03 11:22:59 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: TPM	Rev: V01
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USB3.0

+V5P0A
+V3P3A
+V5P0A 10,11,23,37,39,40,53,60,61,62,63,65
+V3P3A 3,4,5,6,7,9,10,11,23,24,29,31,37,38,47,49,50,51,52,53,56,60,62,65,66,67

+V3P3A
R9005 100K 5% R0402_N I
+V5P0A_USB_WP2
USB2_P1_WP1_OC_N 9

+V5P0A
C : 1.5A/Active High
U9001
VIN VOUT FLG EN GND
RT9711AGB sot_23_5 I
C9004 1uF 6.3V 10% X5R C0402_N NI
7,10,47,50,60 SLP_S4_N
3/14 Change U9001.3 from +V5P0A to SLP_S4_N

+V5P0A_USB_WP2
C9006 470pF 50V 5% COG C0402_N I
C9007 4.7uF 10V 10% X5R C0603_N I
CR9005 AZ5725-01F.R7GR 1uA 5V DFN1006p2x I

CIS ok

JUSB3-1
P1 VBUS
P2 D-
P3 D+
P4 GND
P5 SSRX-
P6 SSRX+
P7 GND_DRAIN
P8 SSTX-
P9 SSTX+
GND G1 GND G2 GND G3 GND G4
W-26-0236-0900B con_usb3_9p_smd_h4p2 I

9 USB2_P1_WP1_DN
9 USB2_P1_WP1_DP
R9007 3.3R R0402_N I 1%
CO-CH_L4_PH0P8_H1_AB 67ohm 320mA +-25%
L9003 NI
R9006 3.3R R0402_N I 1%
USB2_P1_WP1_DN_CONN
USB2_P1_WP1_DP_CONN

9 USB3_P1_RX_DN
9 USB3_P1_RX_DP
R9853 3.3R R0402_N I 1%
CO-CH_L4_PH0P8_H1_AB 67ohm 320mA +-25%
L9508 NI
R9852 3.3R R0402_N I 1%
USB3_P1_RX_DN_CONN
USB3_P1_RX_DP_CONN

9 USB3_P1_TX_DN
9 USB3_P1_TX_DP
C1271 0.1uF 10V 10% X5R C0402_N
C1270 0.1uF 10V 10% X5R C0402_N
USB3_P1_TX_DN_C
USB3_P1_TX_DP_C
R9012 3.3R R0402_N I 1%
CO-CH_L4_PH0P8_H1_AB 67ohm 320mA +-25%
L9002 NI
R9011 3.3R R0402_N I 1%
USB3_P1_TX_DN_CONN
USB3_P1_TX_DP_CONN

USB3_P1_TX_DN_CONN
USB3_P1_TX_DP_CONN
USB3_P1_RX_DP_CONN
USB3_P1_RX_DN_CONN
CR9006
NC NC NC NC
I/O1 I/O2 I/O3 I/O4
GND GND
AZ1045-04F.R7G lcc10_ns_2p5x1p0_p65h I

D+/D- ESD
USB2_P1_WP1_DP_CONN
USB2_P1_WP1_DN_CONN
CR9012 AZ5725-01F.R7GR 1uA 5V DFN1006p2x I
CR9013 AZ5725-01F.R7GR 1uA 5V DFN1006p2x I

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: USB3.0 CONN	Rev: V01
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WIFI & BT Module

+V3P3SX — SH4302 — +V3P3SX_CWS

0R
I
R0603_N
5%

THIS DESIGN SUPPORTS STONE PEAK ONLY

CIS ok

+V3P3SX_CWS

C4320 4.7uF 6.3V 10% X5R C0603_N I
C4321 4.7uF 6.3V 10% X5R C0603_N I
C4322 0.1uF 10V 10% X5R C0402_N I
C4323 0.1uF 10V 10% X5R C0402_N I

C6001 & C6003 FOR PIN 72 &73
C6002 & C6000 FOR PIN 4 & 5

Need Change to 0201 0.1uF

C4318 0.1uF 25V 10% X5R C0201_N
C4319 0.1uF 25V 10% X5R C0201_N

JWLAN1

SLOT A KEY E

1	GND_1	2	3.3V_2
3	USB_D+	4	3.3V_4
5	USB_D-	6	LED1_N
7	GND_7	8	PCM_CLK/I2S_SCK
9	SDIO_CLK	10	PCM_SYNC/I2S_WS
11	SDIO_CMD	12	PCM_IN/I2S_SD_IN
13	SDIO_DATA0	14	PCM_OUT/I2S_SD_OUT
15	SDIO_DATA1	16	LED2_N
17	SDIO_DATA2	18	GND_18
19	SDIO_DATA3	20	UART_WAKE_N
21	SDIO_WAKE_N	22	UART_RX
23	SDIO_RESET_N		

KEY E
PLATFORM_PIN_OUT

33	GND_33	32	UART_TX
35	PETP0	34	UART_CTS
37	PETN0	36	UART_RTS
39	GND_39	38	RESERVED_38
41	PERP0	40	RESERVED_40
43	PERN0	42	RESERVED_42
45	GND_45	44	COEX3
47	REFCLKP0	46	COEX2
49	REFCLKN0	48	COEX1
51	GND_51	50	SSCLK
53	CLKREQ0_N	52	PERST0_N
55	PEWAKE0_N	54	RESERVED_W_DISABLE2_N
57	GND_57	56	W_DISABLE1_N
59	RESERVED_2ND_PETP1	58	I2C_DATA
61	RESERVED_2ND_PETN1	60	I2C_CLK
63	GND_63	62	ALERT
65	RESERVED_2ND_PERP1	64	RESERVED_64
67	RESERVED_2ND_PERN1	66	UIM_SWP/PERST1_N
69	GND_69	68	UIM_PWR_SNK/CLREQ1_N
71	RESERVED/REFCLKN1	70	UIM_PWR_SRC/GPIO1/PEWAKE1_N
73	RESERVED/REFCLKP1	72	3.3V_72
75	GND_75	74	3.3V_74
76	GND76	77	GND77
78	GND78	79	GND79

51749-0750P-205
con_75p_ph05_dip_51749_rvs_e

9 USB2_P4_BT_DP
9 USB2_P4_BT_DN

9 PCIE_WLAN_LN0_TX_SOC_DP
9 PCIE_WLAN_LN0_TX_SOC_DN
PCIE_WLAN_LN0_TX_SOC_DP
PCIE_WLAN_LN0_TX_SOC_DN
PCIE_WLAN_LN0_TX_DP
PCIE_WLAN_LN0_TX_DN

9 PCIE_WLAN_LN0_RX_SOC_DP
9 PCIE_WLAN_LN0_RX_SOC_DN

7 PCIE_REFCLK_WLAN_DP_R
7 PCIE_REFCLK_WLAN_DN_R
PCIE_REFCLK_WLAN_DP
PCIE_REFCLK_WLAN_DN

7 WLAN_CLK_REQ_N
7 PCIE_WAKE_PCH_N
WLAN_CLK_REQ_N
PCIE_WAKE_PCH_N

5,41,50 LPC_FRAME_N
5,41,50 LPC_AD3
LPC_FRAME_N
LPC_AD3

5,41,50 LPC_AD2
5,41,50 LPC_AD1
LPC_AD2
LPC_AD1

5,41 LPC_CLK_PRT80
R4319 0R R0402_N I 5%
5,41,50 LPC_AD0
LPC_AD0

WLAN PCIE AC CAPS

TP9992
TP9993
WIFI/BT_SLOT_TX — TP9976
WIFI/BT_SLOT_RX — TP9977

R4320
0R
R0402_N
5%
I

WLAN_RST_R — SUS_CLK 7
BT_RF_KILL_N — BT_RF_KILL_N 3
WIFI_DISABLE_N — WIFI_DISABLE_N 6
SM_BAT_DATA_DEBUG — R4325 0R R0402_N 5% NI — SM_BAT_DATA 29,50,58,59,66
SM_BAT_CLK_DEBUG — R4326 0R R0402_N 5% NI — SM_BAT_CLK 29,50,58,59,66

4/21 Add SM_BAT_DATA connect to JWLAN1.58,
Add SM_BAT_CLK connect to JWLAN1.60,
Debug card need.

4/21 Add R4325,R4326 0ohm for Debug card

6/27 R4325,R4326 change to NI,
because WLAN card "Intel 2x2AC 8260" I2C is 1.8V,
mother board I2C is 3.3V

+V3P3SX_CWS
R4321
10K
5%
R0402_N
I
WLAN_CLK_REQ_N

Difference with armour
Reserve PLT_RST_N to reset pin and install

WLAN_RST_R — R4323 0R R0402_N 5% — PLT_RST_N 7,26,41,45,50
R4324 0R R0402_N NI 5% — WLAN_RST 8

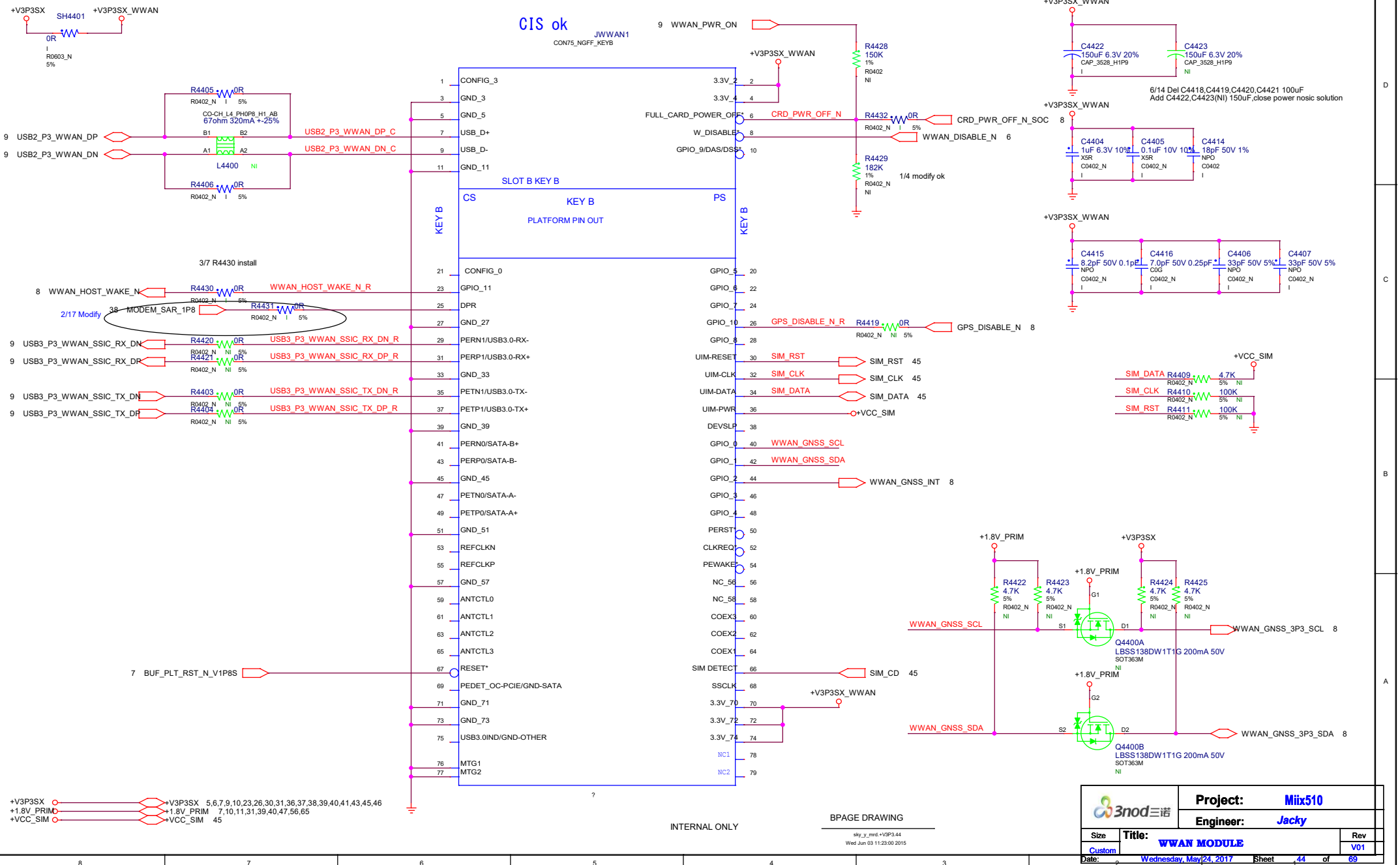
TP6021 — WIFI_DISABLE_N
TP6000 — PCIE_WAKE_PCH_N
TP6020 — BT_RF_KILL_N
TP6007 — SUS_CLK

+V3P3SX — +V3P3SX 5,6,7,9,10,23,26,30,31,36,37,38,39,40,41,44,45,46

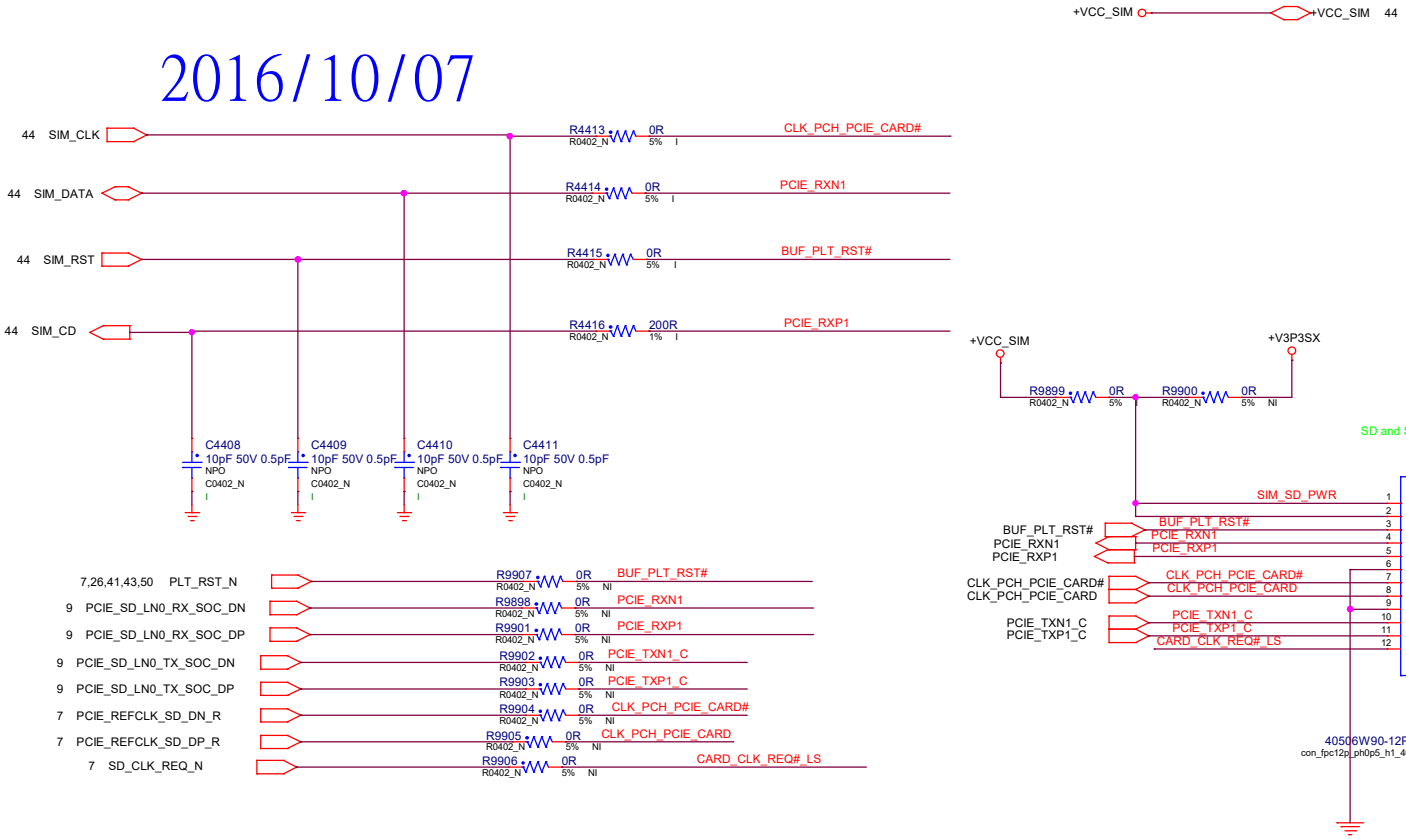
INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.+V3P3.43
Wed Jun 03 11:23:00 2015

3nod三诺	Project:	Miix510	
	Engineer:	Jacky	
Size: Custom	Title:	WLAN WIFI BT MODULE	Rev: V01
Date: Thursday, May 25, 2017	Sheet 43 of 69		


CIS ok
JWWAN1
CON75_NGFF_KEYB
SLOT B KEY B
CS
KEY B
PS
PLATFORM PIN OUT
KEY B
KEY B
+V3P3SX
SH4401
+V3P3SX_WWAN
0R
R0603_N
5%
R4405 0R
R4406 0R
CO-CH_L4_PH0P8_H1_AB
67ohm 320mA +-25%
L4400
NI
9 USB2_P3_WWAN_DP
9 USB2_P3_WWAN_DN
USB2_P3_WWAN_DP_C
USB2_P3_WWAN_DN_C
3/7 R4430 install
8 WWAN_HOST_WAKE_N
R4430 0R
WWAN_HOST_WAKE_N_R
2/17 Modify
38 MODEM_SAR_1P8
R4431 0R
9 USB3_P3_WWAN_SSIC_RX_DN
9 USB3_P3_WWAN_SSIC_RX_DP
R4420 0R
R4421 0R
USB3_P3_WWAN_SSIC_RX_DN_R
USB3_P3_WWAN_SSIC_RX_DP_R
9 USB3_P3_WWAN_SSIC_TX_DN
9 USB3_P3_WWAN_SSIC_TX_DP
R4403 0R
R4404 0R
USB3_P3_WWAN_SSIC_TX_DN_R
USB3_P3_WWAN_SSIC_TX_DP_R
7 BUF_PLT_RST_N_V1P8S
1 CONFIG_3
3 GND_3
5 GND_5
7 USB_D+
9 USB_D-
11 GND_11
21 CONFIG_0
23 GPIO_11
25 DPR
27 GND_27
29 PERN1/USB3.0-RX-
31 PERP1/USB3.0-RX+
33 GND_33
35 PETN1/USB3.0-TX-
37 PETP1/USB3.0-TX+
39 GND_39
41 PERN0/SATA-B+
43 PERP0/SATA-B-
45 GND_45
47 PETN0/SATA-A-
49 PETP0/SATA-A+
51 GND_51
53 REFCLKN
55 REFCLKP
57 GND_57
59 ANTCTL0
61 ANTCTL1
63 ANTCTL2
65 ANTCTL3
67 RESET*
69 PEDET_OC-PCIE/GND-SATA
71 GND_71
73 GND_73
75 USB3.0IND/GND-OTHER
76 MTG1
77 MTG2
3.3V_2
3.3V_4
FULL_CARD_POWER_OFF*
W_DISABLE*
GPIO_9/DAS/DSS*
GPIO_5
GPIO_6
GPIO_7
GPIO_10
GPIO_8
UIM-RESET
UIM-CLK
UIM-DATA
UIM-PWR
DEVSLP
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
PERST*
CLKREQ*
PEWAKE*
NC_56
NC_58
COEX3
COEX2
COEX1
SIM DETECT
SSCLK
3.3V_70
3.3V_72
3.3V_74
NC1
NC2
9 WWAN_PWR_ON
+V3P3SX_WWAN
R4428 150K
R4429 182K
CRD_PWR_OFF_N
R4432 0R
CRD_PWR_OFF_N_SOC 8
WWAN_DISABLE_N 6
1/4 modify ok
GPS_DISABLE_N_R
R4419 0R
GPS_DISABLE_N 8
SIM_RST
SIM_CLK
SIM_DATA
+VCC_SIM
SIM_RST 45
SIM_CLK 45
SIM_DATA 45
WWAN_GNSS_SCL
WWAN_GNSS_SDA
WWAN_GNSS_INT 8
SIM_CD 45
+V3P3SX_WWAN
C4422 150uF 6.3V 20%
C4423 150uF 6.3V 20%
6/14 Del C4418,C4419,C4420,C4421 100uF
Add C4422,C4423(NI) 150uF,close power nosic solution
C4404 1uF 6.3V 10%
C4405 0.1uF 10V 10%
C4414 18pF 50V 1%
C4415 8.2pF 50V 0.1pF
C4416 7.0pF 50V 0.25pF
C4406 33pF 50V 5%
C4407 33pF 50V 5%
+VCC_SIM
SIM_DATA R4409 4.7K
SIM_CLK R4410 100K
SIM_RST R4411 100K
+1.8V_PRIM
+V3P3SX
R4422 4.7K
R4423 4.7K
R4424 4.7K
R4425 4.7K
Q4400A
LBSS138DW1T1G 200mA 50V
SOT363M
Q4400B
LBSS138DW1T1G 200mA 50V
SOT363M
WWAN_GNSS_SCL
WWAN_GNSS_SDA
WWAN_GNSS_3P3_SCL 8
WWAN_GNSS_3P3_SDA 8
+V3P3SX 5,6,7,9,10,23,26,30,31,36,37,38,39,40,41,43,45,46
+1.8V_PRIM 7,10,11,31,39,40,47,56,65
+VCC_SIM 45
INTERNAL ONLY
BPAGE DRAWING
sky_y_mrd.+V3P3.44
Wed Jun 03 11:23:00 2015
Project: Miix510
Engineer: Jacky
Size: Custom
Title: WWAN MODULE
Rev: V01
Date: Wednesday, May 24, 2017
Sheet 44 of 69

2016/10/07

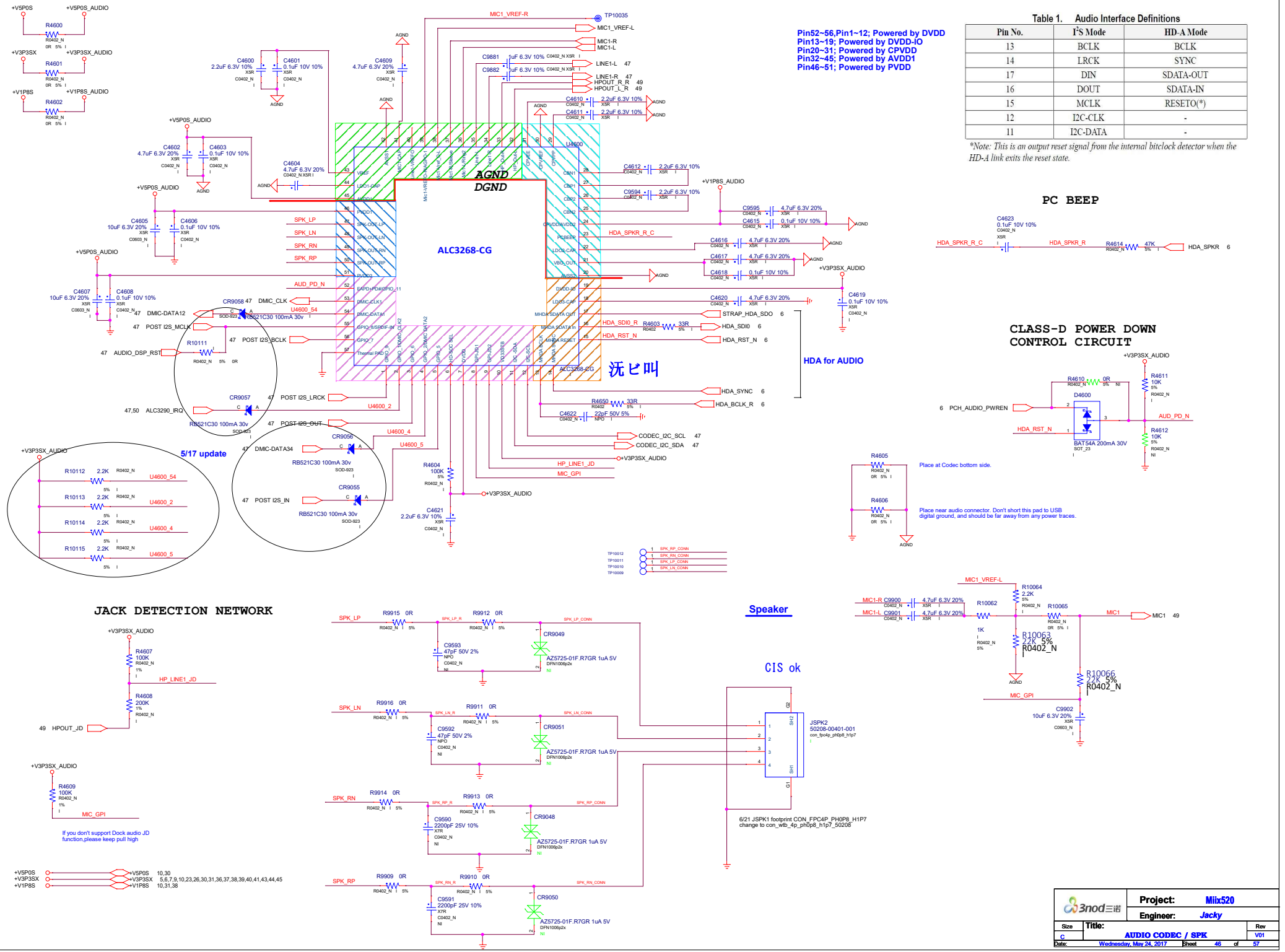


INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:23:01 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: MICRO SIM	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 45 of 69	


ALC3268-CG
AGND
DGND
Pin52~56,Pin1~12; Powered by DVDD
Pin13~19; Powered by DVDD-IO
Pin20~31; Powered by CPVDD
Pin32~45; Powered by AVDD1
Pin46~51; Powered by PVDD
HDA for AUDIO
5/17 update
JACK DETECTION NETWORK
Speaker
CIS ok
PC BEEP
CLASS-D POWER DOWN CONTROL CIRCUIT
Place at Codec bottom side.
Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.
If you don't support Dock audio JD function,please keep pull high
6/21 JSPK1 footprint CON_FPC4P_PH0P8_H1P7 change to con_wtb_4p_ph0p8_h1p7_50208
Table 1. Audio Interface Definitions
Pin No. | I²S Mode | HD-A Mode
13 | BCLK | BCLK
14 | LRCK | SYNC
17 | DIN | SDATA-OUT
16 | DOUT | SDATA-IN
15 | MCLK | RESETO(*)
12 | I2C-CLK | -
11 | I2C-DATA | -
*Note: This is an output reset signal from the internal bitclock detector when the HD-A link exits the reset state.
Project: Mlix520
Engineer: Jacky
Title: AUDIO CODEC / SPK
Size: C
Rev: V01
Date: Wednesday, May 24, 2017
Sheet 46 of 57

AUDIO DSP

ALC3290-CGT

AEC SPK reference signals

NC unused analog power balls
Only PLL related power = AVDD18_1/VAD18 will be used

NC unused analog I/O balls

For AEC SPK reference path , ADC's reference voltage need caps.

NC unused analog ground balls

This SPI is Slave Mode
used to download or flush Flash code

4/26 update

5/24 update

5/17 update

4/28 update

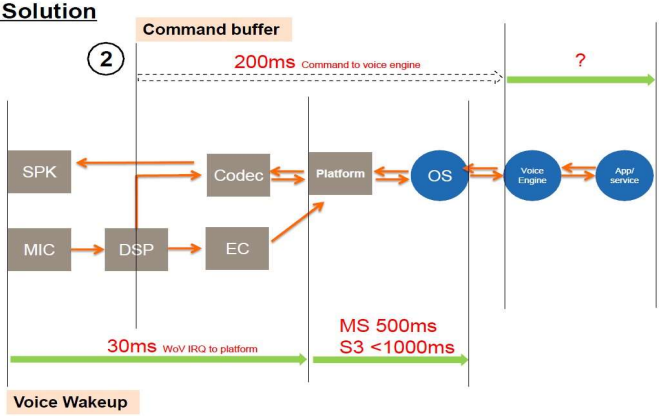
DMIC1

DMIC2

I2S Interface

SPI ROM

Ext. DSP Solution



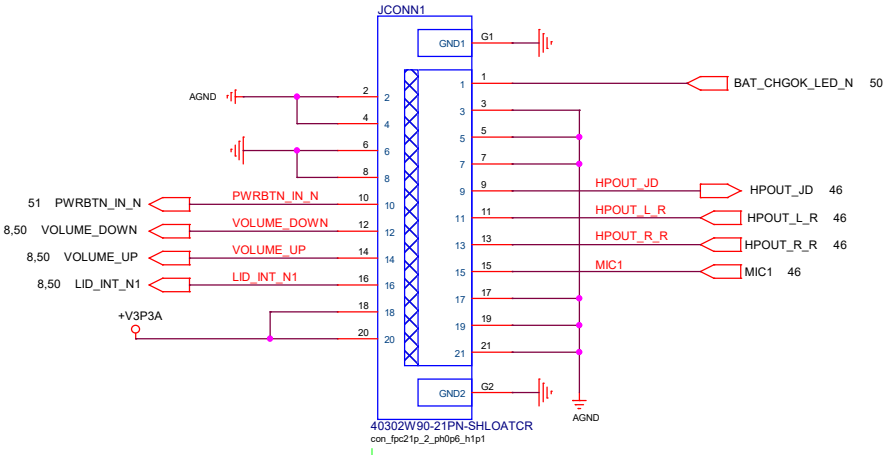
3nod三诺	Project:	Mlix520
	Engineer:	Jacky
Size: C	Title:	AUDIO DSP / DMIC
		Rev: V01
Date: Wednesday, May 24, 2017	Sheet 47 of 57	

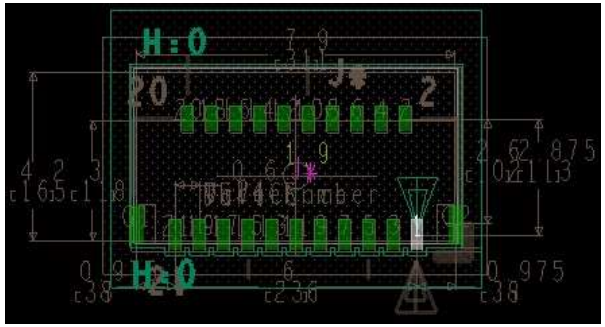
Audio combo jack
Move to IO board

3nod三诺	Project:	Miix510	
	Engineer:	Jacky	
Size: Custom	Title: AUDIO-COMBO JACK		Rev: V01
Date: Wednesday, May 24, 2017	Sheet 48 of 69		

IO Board CONN

CIS ok





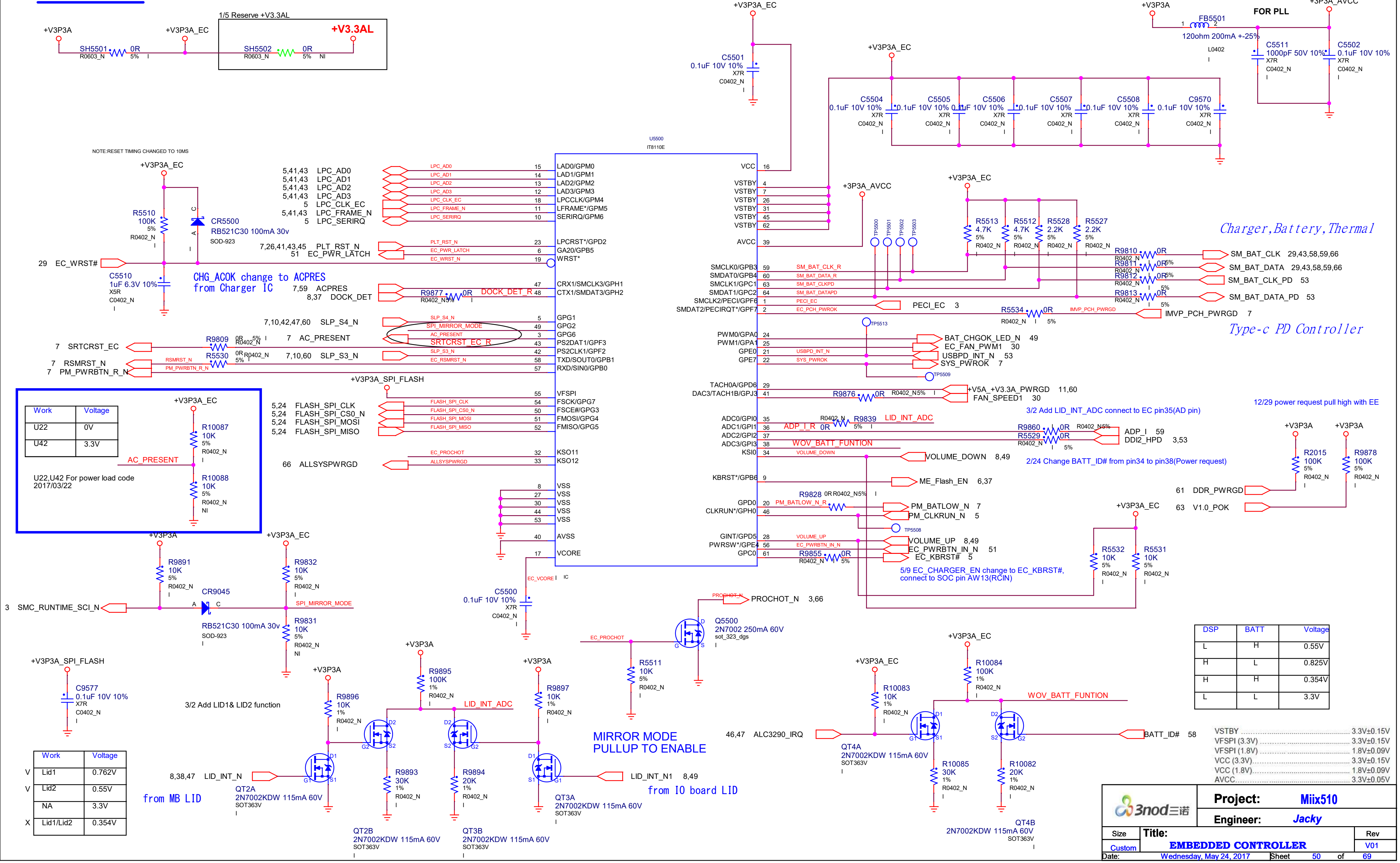
INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+VCHG.49
Wed Jun 03 11:23:03 2015

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: IO board CONN	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 49 of 69	

EC controller



Work	Voltage
U22	0V
U42	3.3V

DSP	BATT	Voltage
L	H	0.55V
H	L	0.825V
H	H	0.354V
L	L	3.3V

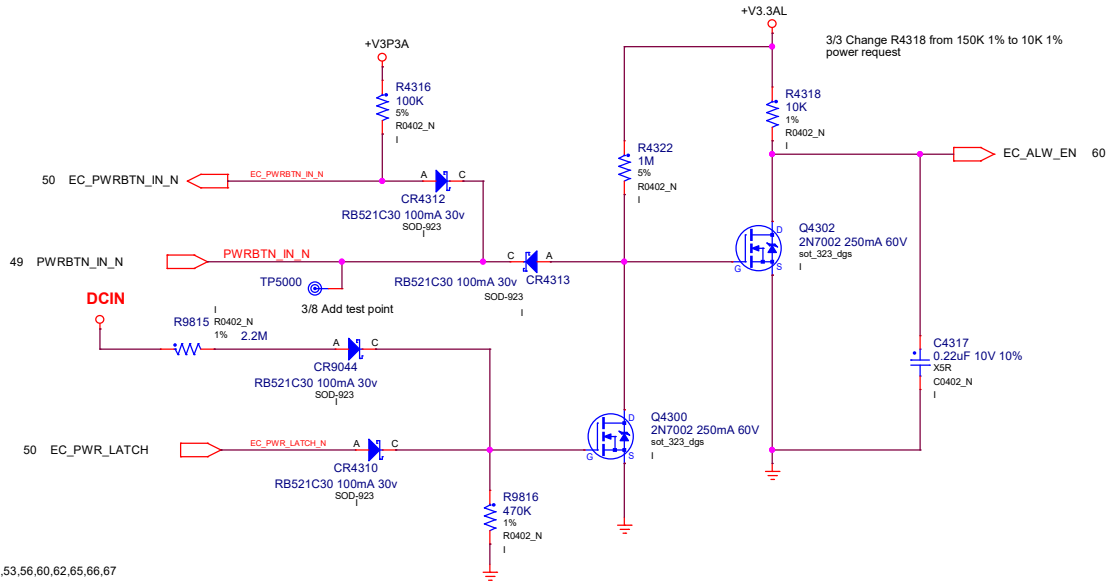
	Work	Voltage
V	Lid1	0.762V
V	Lid2	0.55V
	NA	3.3V
X	Lid1/Lid2	0.354V

VSTBY .... 3.3V±0.15V
VFSPI (3.3V) .... 3.3V±0.15V
VFSPI (1.8V) .... 1.8V±0.09V
VCC (3.3V) .... 3.3V±0.15V
VCC (1.8V) .... 1.8V±0.09V
AVCC .... 3.3V±0.05V

3nod 三诺

Project: Miix510
Engineer: Jacky
Size: Custom
Title: EMBEDDED CONTROLLER
Rev: V01
Date: Wednesday, May 24, 2017
Sheet 50 of 69

Power switch
Move to IO board



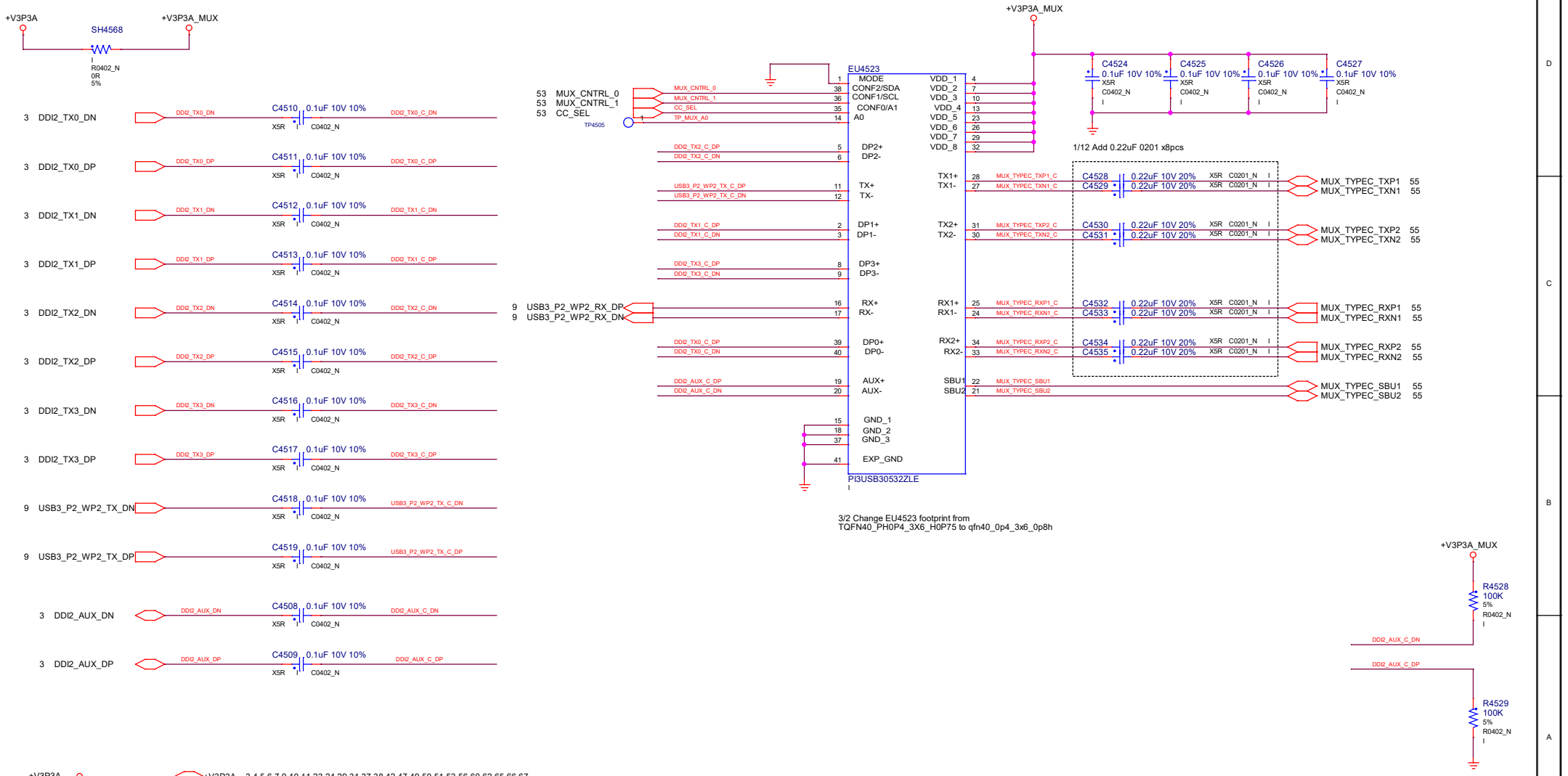
+V3P3A	+V3P3A 3,4,5,6,7,9,10,11,23,24,29,31,37,38,42,47,49,50,52,53,56,60,62,65,66,67
+V3.3AL	+V3.3AL 7,11,50,58,60,66
DCIN	DCIN 58,59

Power LED

	Battery Life <5%			Battery Life <20%			Battery Life <80%			Battery Life <=100%		
	S0	S3	S4/S5	S0	S3	S4/S5	S0	S3	S4/S5	S0	S3	S4/S5
Charge	Amber			Amber			White			White		
	0.25s on			<-			0.1s off			solid on		
	0.25s off			<-			5s on			/		
	0.25s on			<-			/					
	0.25s off			<-								
	0.25s on			<-								
	3s off			<-								
Discharge	Amber	Off	Off	Amber	Off	Off	Off	Off	Off	Off	Off	Off
	0.25s on			solid on								
	0.25s off											

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: BUTTON & LED	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 51 of 69	

TYPE-C Multiplexer



INTERNAL ONLY

BPAGE DRAWING

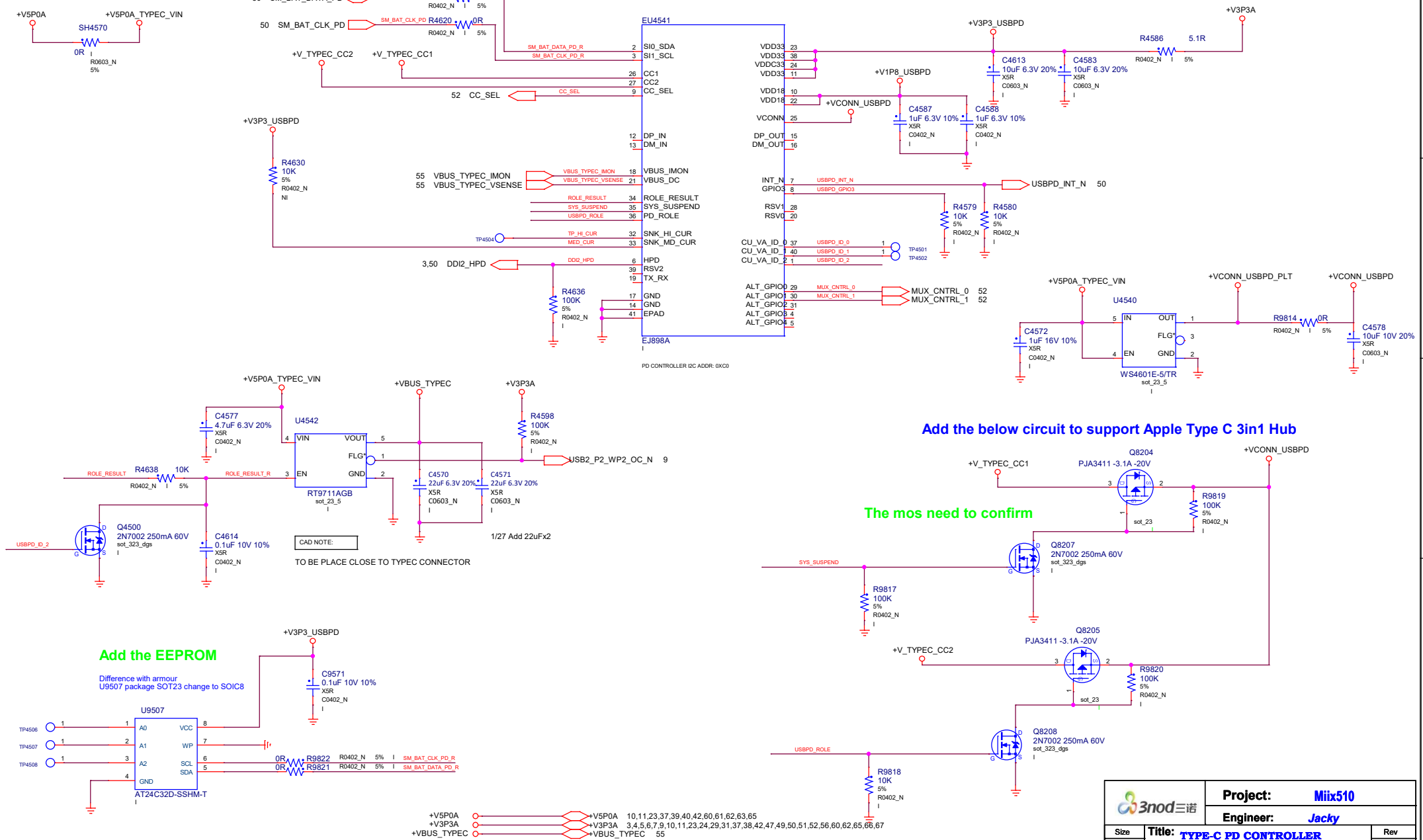
sky_y_mrd.+V3P3.52
Wed Jun 03 11:23:04 2015

Project: Miix510			
Engineer: Jacky			
Size: Custom	Title: TYPE-C MULTIPLEXER		Rev: V01
Date: Wednesday, May 24, 2017	Sheet 52 of 69		

VARIANT:		DOCUMENT_NUMBER	REV	PAGE
<VARIANT>	INTEL CONFIDENTIAL	H78885	1P0	52/57

Type-c PD Controller

PD schematic NEED CONFIRM



3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: TYPE-C PD CONTROLLER	Rev: V01
Date: 2 Wednesday, May 24, 2017	Sheet 531 of 69	

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A

3nod三诺	Project: Miix510	
	Engineer: Jacky	
Size: Custom	Title: TYPE-C BOOST VR	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 54 of 69	

TYPE-C Connector

CIS ok

+VBUS_TYPEC

+VBUS_TYPEC_CONN

R4618 0.010 CH 1% 0805

C4502 1uF 16V 10% X5R C0402_N

CR4561 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

VBUS_TYPEC_SENSE_N

VBUS_TYPEC_SENSE_P

R4533 39K 1% R0402_N

R4530 39K 1% R0402_N

VBUS_TYPEC_IMON

VBUS_TYPEC_VSENSE

R4534 3.01K 1% R0402_N

R4531 3.01K 1% R0402_N

C9576 10nF 50V 10% X7R C0402_N

C9575 10nF 50V 10% X7R C0402_N

VBUS_TYPEC_IMON 53

VBUS_TYPEC_VSENSE 53

+V_TYPEC_CC1

CR4564 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

52 MUX_TYPEC_SBU1

R4507 1M 5% R0402_N

CR4567 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

JTYPEC1 55912-0240Y-101

A1	GND_1	GND_4	B12
A2	SSTXp1	SSRXp1	B11
A3	SSTXn1	SSRXn1	B10
A4	VBUS_1	VBUS_4	B9
A5	CC1	RFU2	B8
A6	Dp1	Dn2	B7
A7	Dn1	Dp2	B6
A8	RFU1	CC2	B5
A9	VBUS_2	VBUS_3	B4
A10	SSRXn2	SSTXn2	B3
A11	SSRXp2	SSTXp2	B2
A12	GND_2	GND_3	B1
G1	GND_5		
G2	GND_6		
G3	GND_7		
G4	GND_8		
G5	GND_9		
G6	GND_10		

MUX_TYPEC_TXP1_CONN

MUX_TYPEC_TXN1_CONN

USB2_P2_WP2_DP_CONN

USB2_P2_WP2_DN_CONN

MUX_TYPEC_SBU1

MUX_TYPEC_RXN2_CONN

MUX_TYPEC_RXP2_CONN

MUX_TYPEC_RXP1_CONN

MUX_TYPEC_RXN1_CONN

MUX_TYPEC_SBU2

MUX_TYPEC_TXN2_CONN

MUX_TYPEC_TXP2_CONN

MUX_TYPEC_SBU2 52

+V_TYPEC_CC2

CR4563 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

R4505 1M 5% R0402_N

CR4566 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

9 USB2_P2_WP2_DP

9 USB2_P2_WP2_DN

R4599 3.3R R0402_N 1%

L4500 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB NI

R4617 3.3R R0402_N 1%

USB2_P2_WP2_DP_CONN

USB2_P2_WP2_DN_CONN

52 MUX_TYPEC_TXP1

52 MUX_TYPEC_TXN1

R9788 3.3R R0402_N 1%

L4559 67ohm 320mA +-25% NI

R9789 3.3R R0402_N 1%

MUX_TYPEC_TXP1_CONN

MUX_TYPEC_TXN1_CONN

52 MUX_TYPEC_RXP1

52 MUX_TYPEC_RXN1

R9790 3.3R R0402_N 1%

L4557 67ohm 320mA +-25% NI

R9791 3.3R R0402_N 1%

MUX_TYPEC_RXP1_CONN

MUX_TYPEC_RXN1_CONN

52 MUX_TYPEC_TXP2

52 MUX_TYPEC_TXN2

R9792 3.3R R0402_N 1%

L4560 67ohm 320mA +-25% NI

R9793 3.3R R0402_N 1%

MUX_TYPEC_TXP2_CONN

MUX_TYPEC_TXN2_CONN

52 MUX_TYPEC_RXP2

52 MUX_TYPEC_RXN2

R9794 3.3R R0402_N 1%

L4558 67ohm 320mA +-25% NI

R9795 3.3R R0402_N 1%

MUX_TYPEC_RXP2_CONN

MUX_TYPEC_RXN2_CONN

CR9014 AZ1045-04F.R7G lcc10_ns_2p5x1p0_p65h

CR9015 AZ1045-04F.R7G lcc10_ns_2p5x1p0_p65h

USB2_P2_WP2_DP_CONN

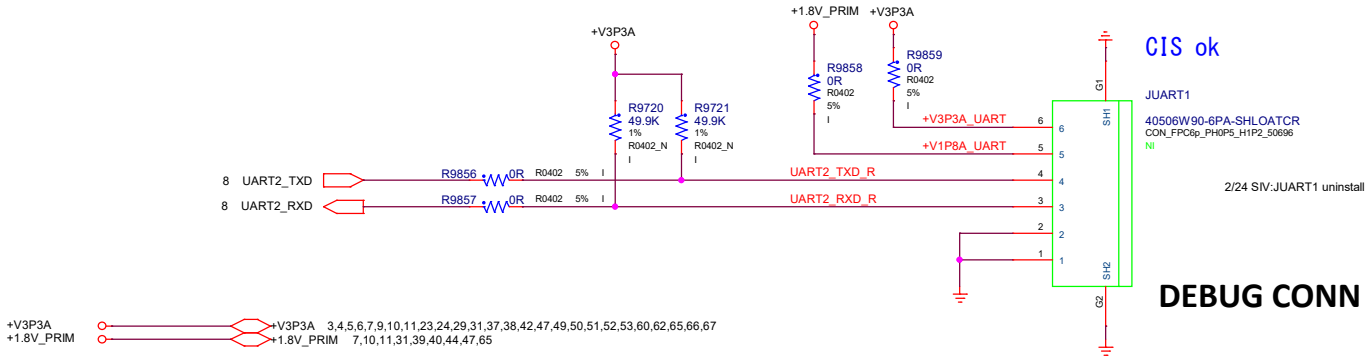
USB2_P2_WP2_DN_CONN

CR4556 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

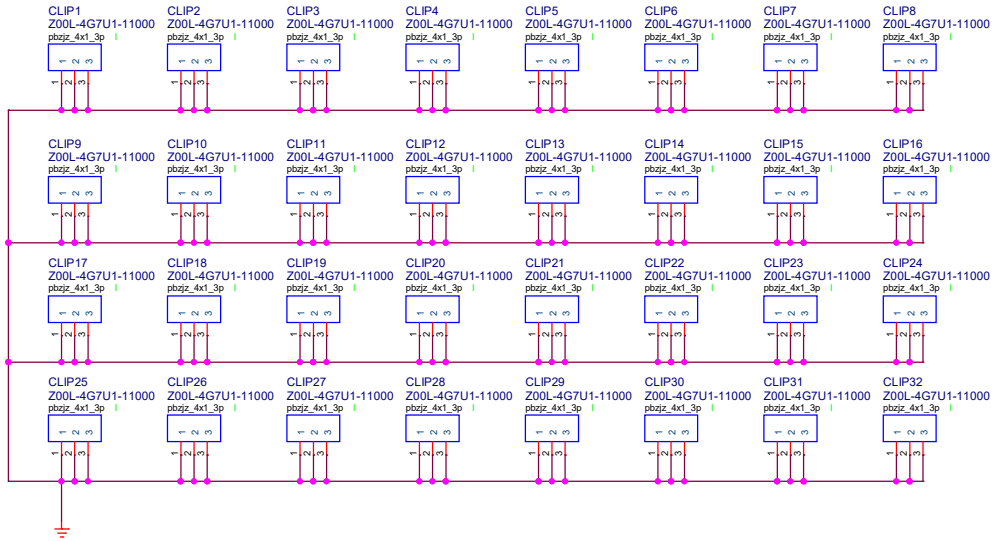
CR4568 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

+VBUS_TYPEC +VBUS_TYPEC 53

3nod三诺	Project:	Miix510
	Engineer:	Jacky
Size: Custom	Title:	TYPE-C CONNECTOR
	Rev	V01
Date:	Wednesday, May 24, 2017	Sheet 55 of 69



Shielding



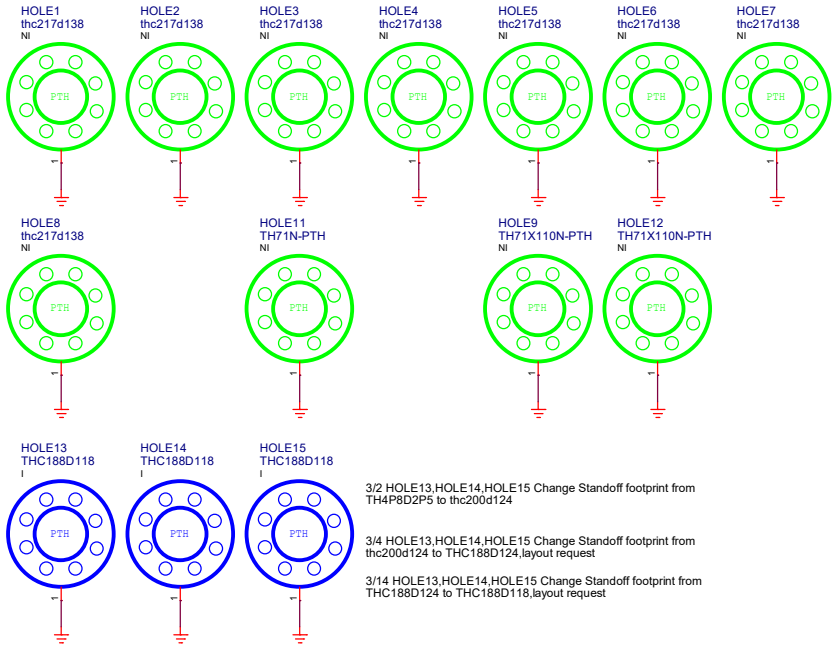
1/13 copy 11.6" NB Shielding

3/9 Del Z000-4G7U1-11000(CLIP1~CLIP24),
add Z00L-4G7U1-11000(CLIP1~CLIP32)

5/5 footprint pbzjz_4x1_3p change to SHEILDING_CASE_3P_0P8X4,SMT request

INTERNAL ONLY

Holes



3/2 HOLE13,HOLE14,HOLE15 Change Standoff footprint from TH4P8D2P5 to thc200d124

3/4 HOLE13,HOLE14,HOLE15 Change Standoff footprint from thc200d124 to THC188D124,layout request

3/14 HOLE13,HOLE14,HOLE15 Change Standoff footprint from THC188D124 to THC188D118,layout request

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:23:06 2015

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	Engineer: Jacky	
Size: Custom	Title: UART CONN & HOLE & CLIP	Rev: V01
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SDV=>SIV

2/2 Page04 Add Rsv RM97,RM98 for 16Gb memory(BG1)
2/2 Page04 Add (4Gb 8Gb) & (16Gb) BOM option table
2/2 Page19,20 Memory pin M9 connect to CPU BG1

2/24 Page10 UC6,UC7 pin9 connect GND,need change to +1.0V_PRIM (HW issue)
2/24 Page07 Add R1042,VR_PWRGD connect to IMVP_PCH_PWRGD,SOC and EC (HW issue)
2/24 Page56 Delete JUART1,Debug conn
2/24 Page24 Delete @U3002,SPI ROM conn
2/24 Page50 Change BATT_ID# from pin34 to pin38[ADC pin] (Power request)
2/24 Page50 Change LID_INT_N from pin38 to pin34

3/2 Page05 R9863 change to NI,THERMAL HW shutdown
3/2 Page08 Change memory ID PU from +1.8V_PRIM to +3V_PRIM
3/2 Page37 ME_Flash_EN connect to R9881
3/2 Page50 Add LID1 & LID2 function,add QT2,QT3,R9893,R9894,R9895,R9896,R9897
3/2 Page56 HOLE13,HOLE14,HOLE15 Change Standoff footprint from TH4P8D2P5 to thc200d124
3/2 Page52 Change EU4523 footprint from TQFN40_PHOP4_3X6_HOP75 to qfn40_Op4_3x6_Op8h

3/3 Page51 Change R4318 from 150K 1% to 10K 1%,power request
3/3 Page50 Change EC_CHARGER_EN to pin61(pin61 can outpin)
3/4 Page56 hange Standoff footprint from thc200d124 to THC188D124(layout request)
3/7 Page19,20 Add RM99,RM100 0ohm to GND,for 4/8 Gb memory
3/7 Page38 +1.8V_PRIM change to +V3P3SX,and add R8020,close +V3P3SX leakage
3/7 Page30 R9847 connect to +V5POS,change to +V3P3SX
3/7 Page07 Del R1088,Add R9865 , HW_ID SIV
3/7 Page44 R4430 install
3/8 Page06 Del RCAM_PD_N offpage,add TP1061
3/8 Page39 JREAR1 pin8 change to NC,pin11 change to RCAM_RST_N,delete RCAM_PD_N
3/8 Page08 Change WWAN_SAR_DET from BA7 to AD11(Group F is 1.8V)
3/8 Page08 Change R1094 from 100K to 0ohm,Del R1095 120K,can use HUAWEI module
3/8 Page51 Add TP5000,close to PWRBTN_IN_N
3/9 Page26 Del R4202,R4203,don't Co-lay PCIE12 RX
3/9 Page11 Del RC429,don't connect to BATT_RTC
3/9 Page56 Del Z000-4G7U1-11000(CLIP1~CLIP24),add Z00L-4G7U1-11000(CLIP1~CLIP32)
3/10 Page07 Change Y1000 from seiko to HOSONIC
3/10 Page07 C1251,C1252 from 18pF to 12pF,HOSONIC request
3/10 Page07 C1249,C1250 from 22pF to 8.2pF,HOSONIC request
3/11 All ESD part,ESDL0402-05 Born change to AZ5725-01F.R7GR Amazing;
ESD5344D Willse change to AZ1045-04F.R7G Amazing
3/14 Page56 HOLE13,HOLE14,HOLE15 Change Standoff footprint from
THC188D124 to THC188D118,layout request
3/14 Page42 Change U9001.3 from +V5POA to SLP_S4_N
3/14 Page15 Add CC390,CC391 reserved,Power request
3/15 Page37 Add CR9046,CR9047 reserved,EMC request
3/15 Page07 R9889,R9890 move to page43,RF request
3/16 Page26 Add SSD(PCIE or SATA) BOM option table
3/18 Page06 Add TP1061
3/18 Page39 Update REAR CAMERA pindefine(Use ov5648 Rear camera module)
3/18 Page40 Add DVDD_1.5V solution(ov5648 Rear camera module need)
3/18 Page37 Add R8212 PU +V3P3SX_TOUCH,for TOUCH_PANEL_INT_N
3/21 Page07 Change C1251,C1252 from 12pF to 15pF,hosonic & seiko share
3/22 Page36 FB8200 0603 Bead change to JP8200 JUMP_43X79,for EDP VBAT
3/23 Page36 Add Q8200,Q8201,R8200,R8201,R8202,R8203,C8219,C8220,C8221,C8222,C8223, for Panel power
3/24 Page50 Add R9898 0ohm reserved,connect to EDP_VDD_EN_R

SIV=>SIT

4/21 Page36 Del R9771,R9772,R9773,R9774,R9775,R9776 0ohm;L9505,L9506,L9507 common choke,RF request
4/21 Page43 Add SM_BAT_DATA connect to JWLAN1.58,Add SM_BAT_CLK connect to JWLAN1.60,Debug card need.
4/21 Page43 Add R4325,R4326 0ohm for Debug card
4/21 Page07 Del R9865,R1089,add R1088,R9866,for HW_ID SIT
4/28 Page38 U8002 G2129BAE1U change to G3401A91G,4bit=>2bit
5/4 Page09 WIFI PCIE port 8 change to port 4,because PCH HSIO 8 can use PCIe interface (for Base-U)
5/9 Page50 EC_CHARGER_EN change to EC_KBRST#,connect to SOC pin AW13(RCIN)
5/9 Page05 EC_KBRST# Add PU R1066 10Kohm +V3P3SX
5/10 Page50 Del R9898,Del net EDP_VDD_EN_R offpage
5/10 Page06 Del TP1055,TP1056,TP1057,TP1058,TP1059,TP1060,TP1016,TP1017,MIPI defferential don't test point
5/12 Page37 EMC:CR9046,CR9047 install
5/16 Page23 EMC reserved C2309,C2310,C2311,C2312,C2313,C2314,C2315,C2316,C2317
5/23 Page37 R9881 uninstall,BIOS request
5/23 Page06 R9848 install,BIOS request

SIT=>SIT2

Page38 R8014 install,SAR_PROX_INT need PU
Page38 Del JSAR1,JSAR2 416990534200,del R8008 0ohm,del TP8002; add JSAR1 conn 416990528900,RF request
Page44 Del C4418,C4419,C4420,C4421 100u,add C4422,C4423(NI) 150uF,close power nosic solution

SIT2=>SVT

5/30 Page07 HW_ID3 add SAR sensor to decide on,driver request
5/30 Page07 Del R1088,add R9865,for SVT phase
6/6 Page51 Del LED1 for SVT phase
6/20 Page40 Y8500 24MHZ +/- 10PPM change to 19.2MHZ +/- 25PPM,Intel request
6/21 Page38 Reserve R8021,R8022 0ohm, ISH I2C to SAR sensor
6/24 Page38 SAR_PROX_RST add R8023 PU,RF request
6/24 Page08 SAR_PROX_RST,reserved R1096 connect to GPP_A12,add R1095 connect to GPP_A22,BIOS request
6/27 Page43 R4325,R4326 change to NI,because WLAN card "Intel 2x2AC 8260" I2C is 1.8V,mother board I2C is 3.3V

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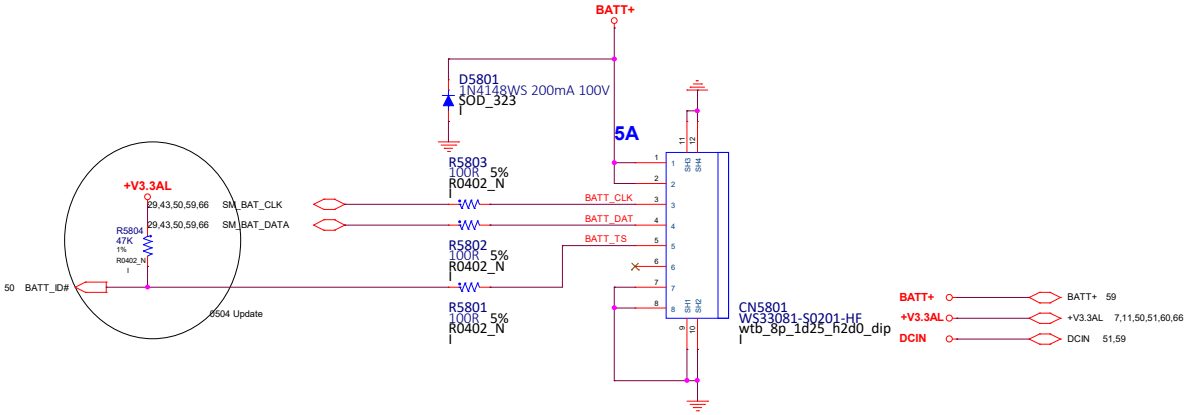
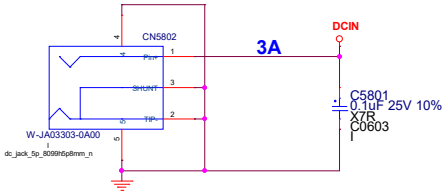
58: DC-IN & BATTERY CONNECTOR





3nod三诺	Project: Miix510	
	Engineer: Frank	
Size: C	Title: DCIN/BATT CONN	Rev: V01
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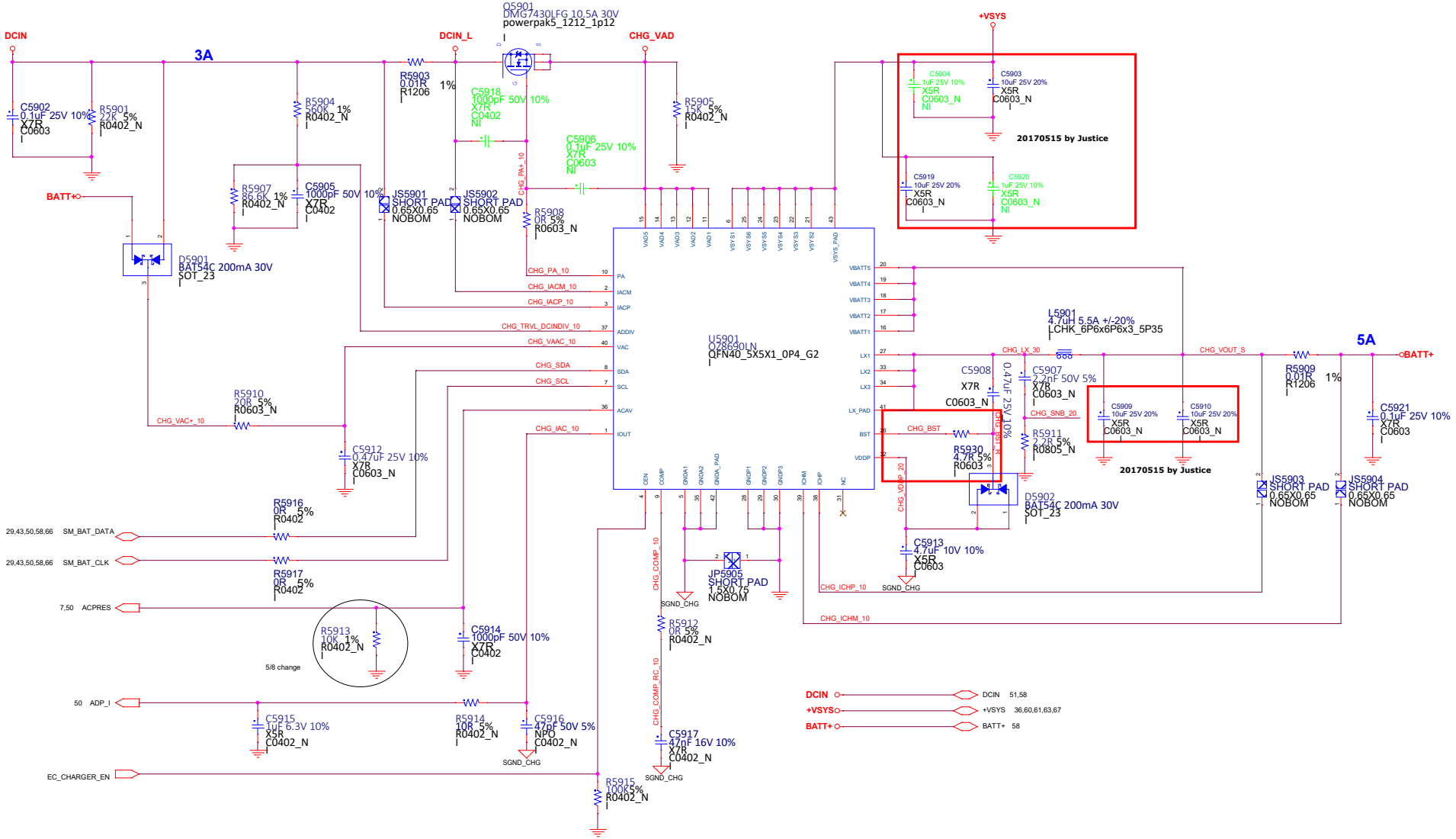
59: BATTERY CHARGER



3nod三诺	Project: Miix510		
	Engineer: Frank		
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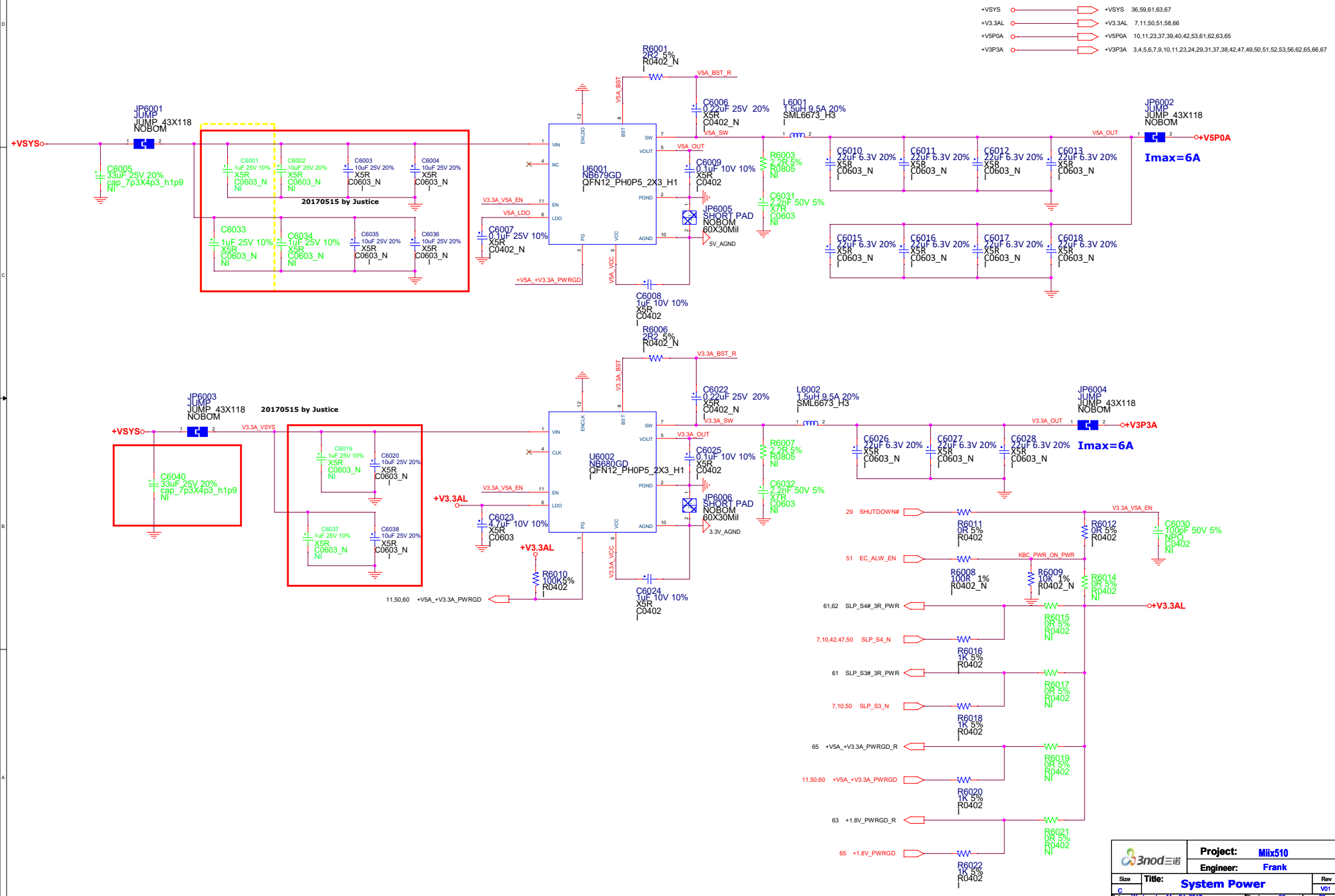
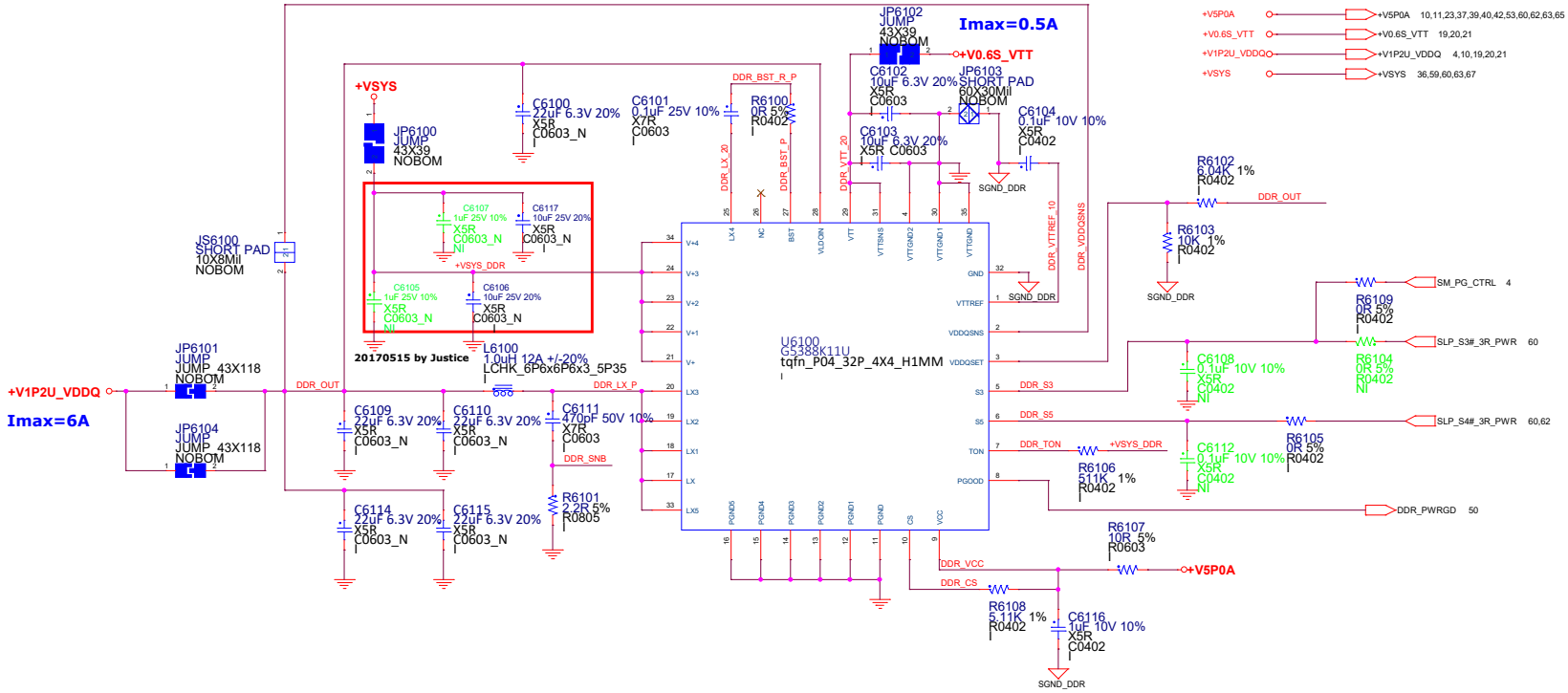
60: +V5P0A / +V3P3A POWER SUPPLY



61: DDR POWER SUPPLY



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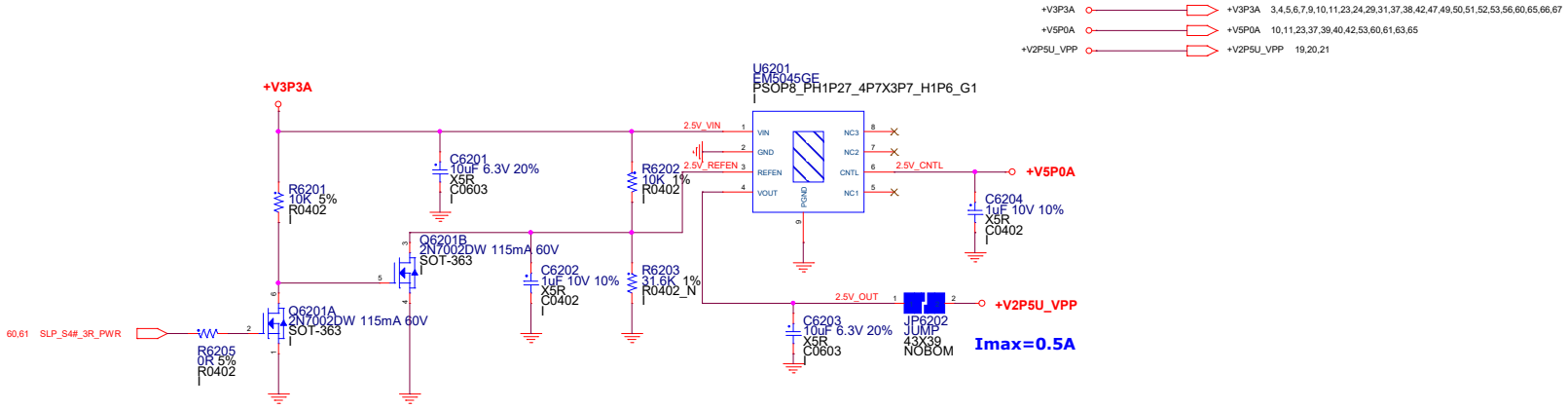
62: +V2P5U_VPP POWER SUPPLY



3nod三诺	Project: Miix510	
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Size: C	Title: +V2P5U_VPP	Rev: V01
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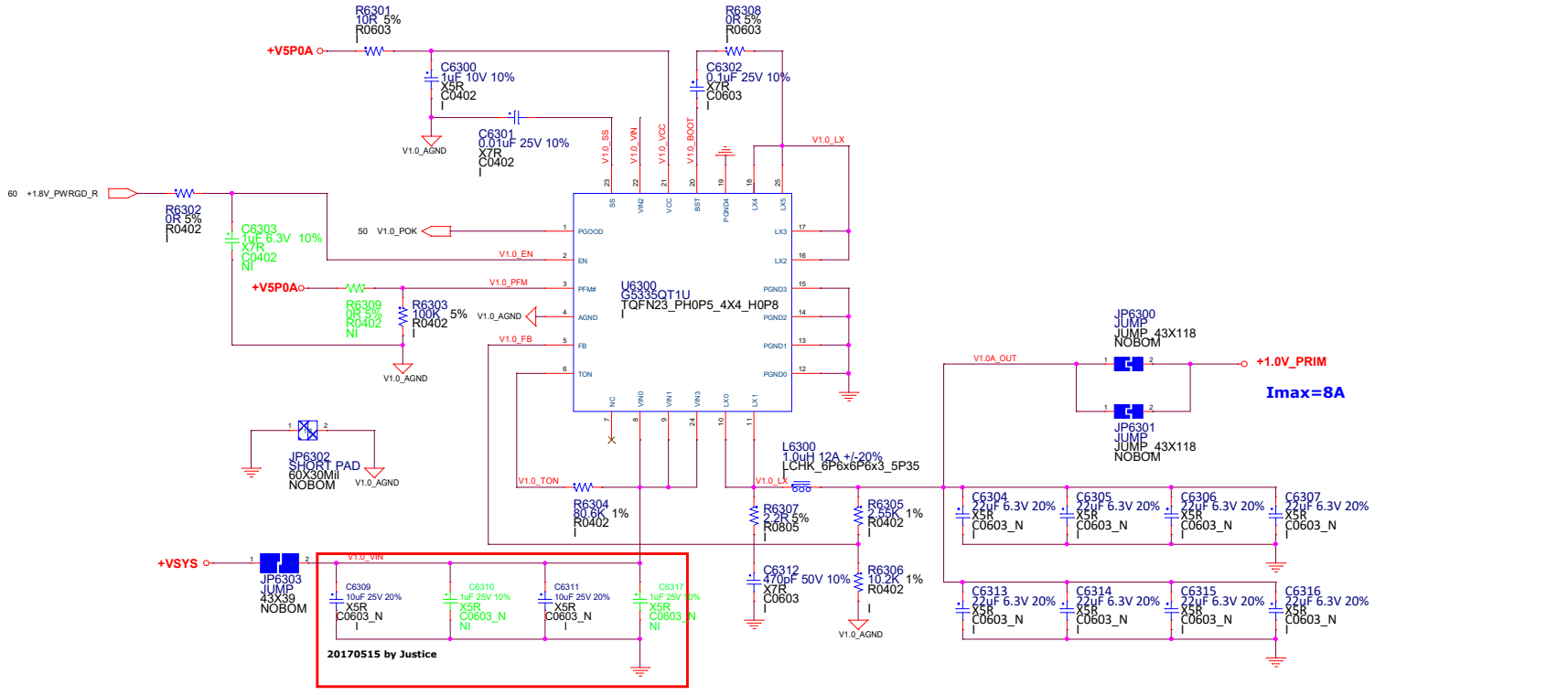
63: +1.0V_PRIM POWER SUPPLY



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	Engineer:	Frank	
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3nod三诺	Project:	Miix510	
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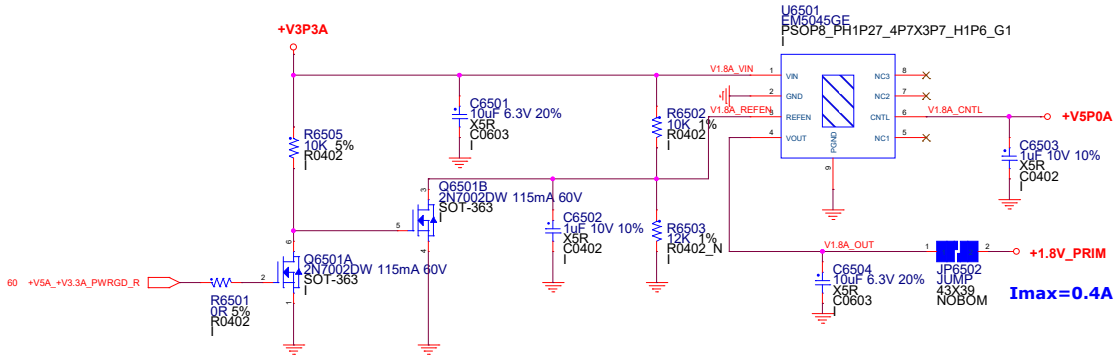
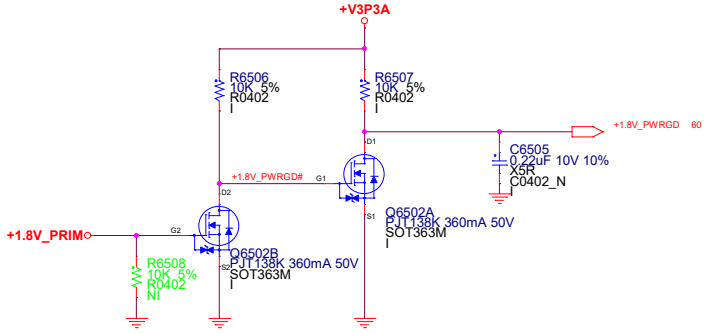
65: +1.8V_PRIM POWER SUPPLY





3nod三诺	Project: Miix510		
	Engineer: Frank		
Size C	Title: +1.8V_PRIM		Rev V01
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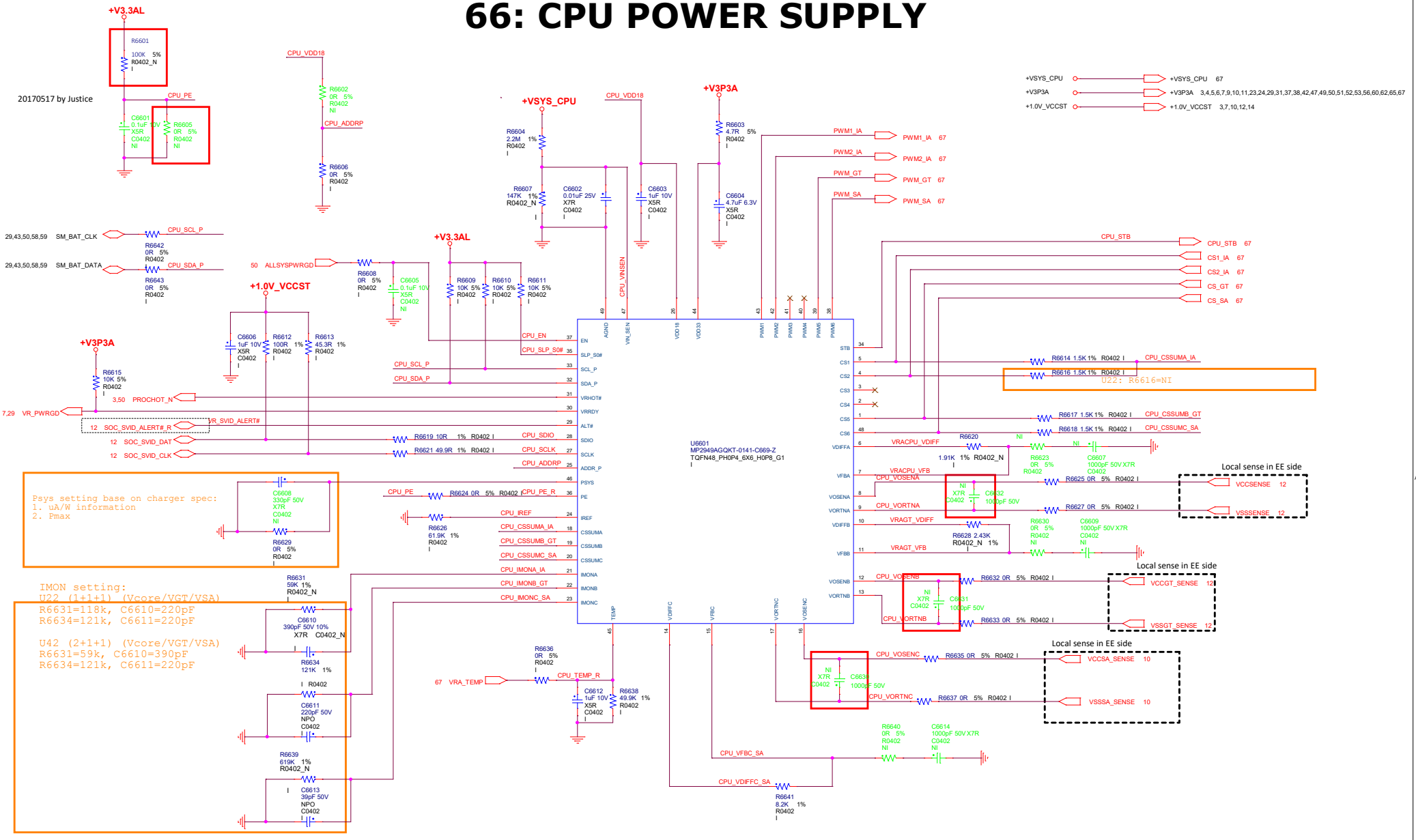
66: CPU POWER SUPPLY



3nod三诺	Project:	Miix510	
	Engineer:	Frank	
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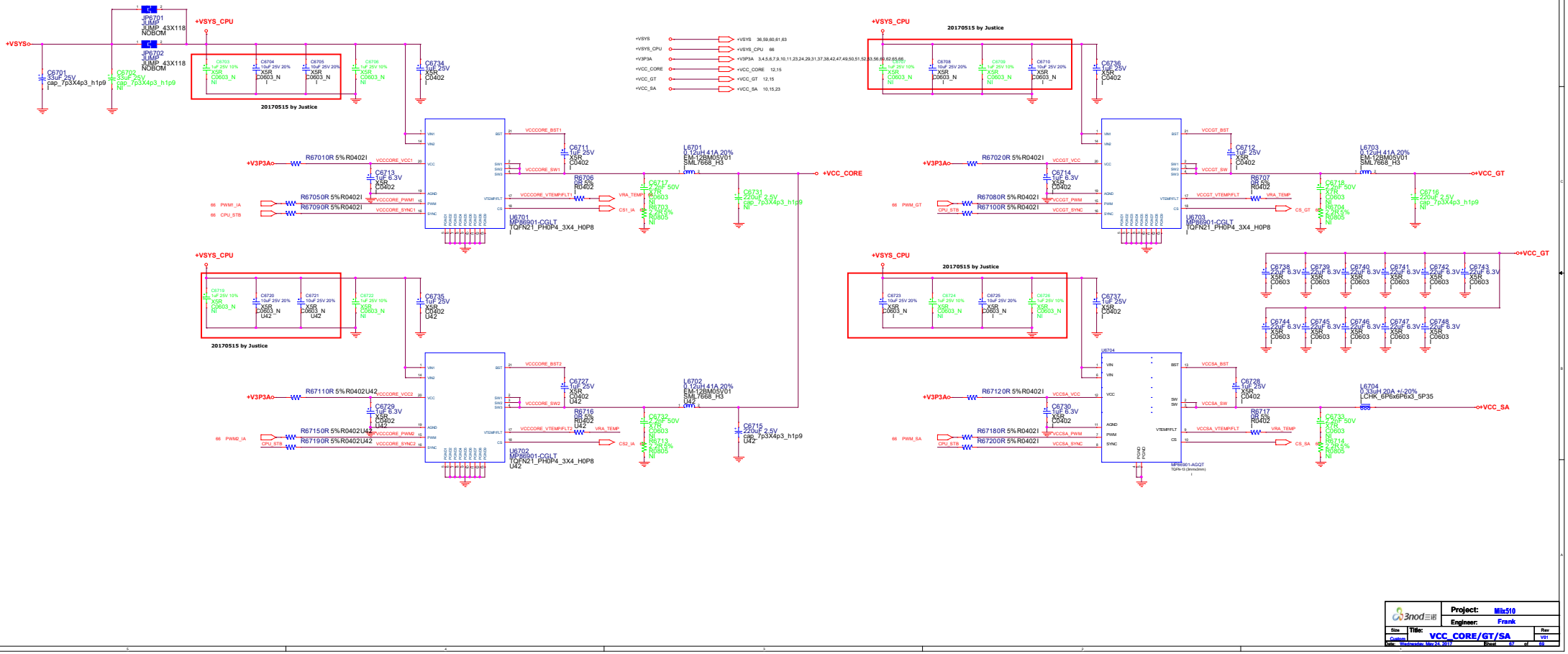
67: VCC_CORE/GT/SA POWER SUPPLY



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	Engineer:	Frank
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3nod三诺	Project: Mix510	
	Engineer: Frank	
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POWER CHANGE LIST
SDV to SIV

3/3 Page60. Change R6008 from 1k to 100R and R6009 from 150k to 10k to fine tune enable level.
3/17 Page66. Fine tune CPU transient,LL. Change R6603 to 1.87Kohm. Change R6619 to 604ohm. Change C6615 to 3300pF. Change R6628 to 150Kohm. Change C6622 to 68nF. Change R6651 to 39.2Kohm. Change R6655 to 100Kohm. Change R6644 to 1.1Kohm. Change R6646 to 1.5Kohm. Change R6635 to 30Kohm. Change R6618 to 69.8Kohm. Change C6609 to 3300pF

3nod三诺	Project: Miix510	
	Engineer: Frank	
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