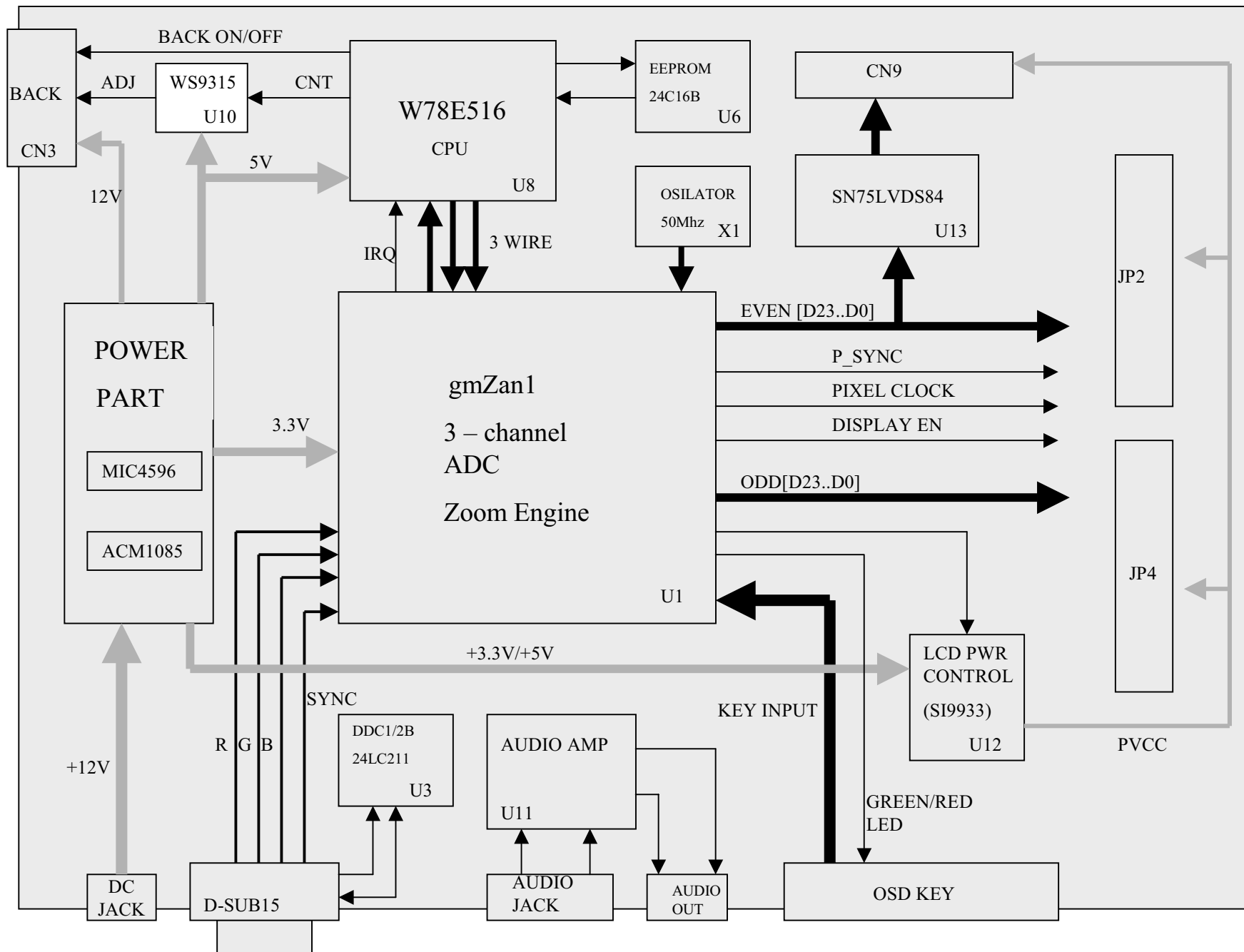
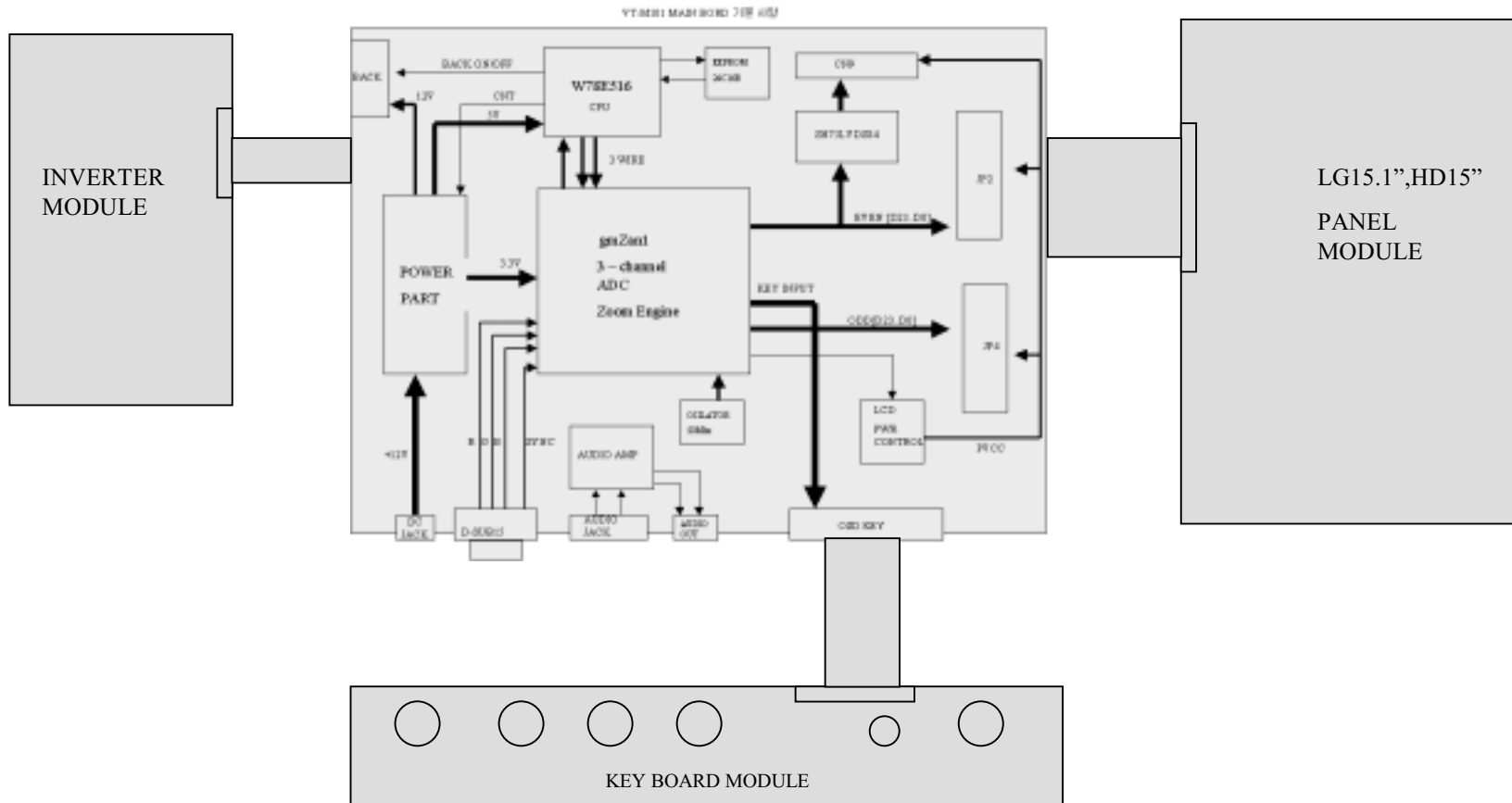


The block diagram illustrates the internal components and interconnections of the W78E516-based video camera system. The central component is the **W78E516 CPU (U8)**, which is connected to an **EEPROM 24C16B (U6)** and an **OSILATOR 50Mhz (X1)**. The CPU is also connected to a **WS9315 U10** (containing **MIC4596** and **ACM1085**) and a **gmZan1 3-channel ADC Zoom Engine (U1)**. The **POWER PART** block provides **+12V** and **+3.3V/+5V** power to the system. The **DC JACK** is connected to the **POWER PART**. The **D-SUB15** connector is connected to the **gmZan1** and the **DDC1/2B 24LC211 (U3)**. The **AUDIO JACK** is connected to the **AUDIO AMP (U11)**, which is also connected to the **AUDIO OUT**. The **OSD KEY** is connected to the **KEY INPUT** of the **gmZan1** and the **GREEN/RED LED**. The **LCD PWR CONTROL (SI9933) (U12)** is connected to the **KEY INPUT** and the **OSD KEY**. The **SN75LVDS84 (U13)** is connected to the **gmZan1** and the **CN9** connector. The **BACK ON/OFF** button is connected to the **BACK** pin of the **CN3** connector. The **BACK** pin of the **CN3** is also connected to the **ADJ** pin of the **WS9315**. The **CNT** pin of the **WS9315** is connected to the **W78E516 CPU**. The **IRQ** pin of the **W78E516 CPU** is connected to the **gmZan1**. The **3 WIRE** interface connects the **W78E516 CPU** and the **gmZan1**. The **gmZan1** outputs **EVEN [D23..D0]**, **P_SYNC**, **PIXEL CLOCK**, **DISPLAY EN**, and **ODD[D23..D0]** signals to the **JP2** and **JP4** connectors. The **JP2** and **JP4** connectors are also connected to the **BACK** pin of the **CN3**. The **PVCC** pin of the **LCD PWR CONTROL** is connected to the **POWER PART**.





SC-1510,1511M BLOCK DIAGRAM