Radiant
First to a wireless planet

Radiant Broadband Wireless Access Network

Test Specification / Test Plan for Transmit Receive Modules, Band 2

Author/Editor: Charlie Caddick / Nigel Watson
Document Number : 881080_02.PTS
Status: 1.0
Date 19 April 2002

Approvals			
Name	**Title**	**Department**	**Signature**
N Watson	Principal Engineer	Radio Systems	
E Bayar	Senior Development Manager	Radio Systems	
W Tondryk	Principal Systems Engineer	Radio Systems	
R Husain	Quality Manager	QA	

Radiant Networks PLC
The Mansion
Chesterford park
Little Chesterford
Essex
CB10 1XL

Tel: (01799) 533600
Fax: (01799) 533601

CHANGE HISTORY

Version	Author	Date	Comments
Drawing No. 881020			
Draft-1	C Caddick	07/12/00	Initial draft
Draft-2	C Caddick	08/02/01	Updated to reflect manufacturers comments
Draft-3	N Watson	24/2/01	Update to include ESS
1	N Watson	1/7/01	Update to include I^2C and detail changes to detector measurements. First Issue for production. Split specs for Band 1 and Band 2.
Reissued as drawing No. 881080			
1			Update for TR3 and includes LNA cal

CONTENTS

1 INTRODUCTION 6

1.1 SYSTEM DESCRIPTION 6
1.2 TRANSMIT RECEIVE MODULE 6
1.3 TEST PHILOSOPHY 7
1.4 DESIGN VERIFICATION TEST (DVT) AIM 8
1.5 PRODUCTION TEST AIM 8
1.6 TESTING AIMS 8

2 TRANSMIT RECEIVE MODULES TEST LEVELS 18

2.1 LIMITED FUNCTIONAL TEST (LFT) 20
2.2 FULL FUNCTIONAL TESTS (FFT) 23
2.3 EXTENDED FUNCTIONAL TEST (EFT) 25
2.4 DESIGN VERIFICATION TEST (DVT) 25
2.5 ASSEMBLY / TEST FLOW 19
2.6 SUMMARY OF TEST STAGES 18
2.7 RECORDING OF TEST DATA ..... **ERROR! BOOKMARK NOT DEFINED.**

3 REQUIREMENTS SPECIFICATIONS 9

3.1 ELECTRICAL SPECIFICATION [3] 9
3.2 MECHANICAL SPECIFICATION [3] 9
3.3 ENVIRONMENTAL SPECIFICATION [2] 10
3.4 ELECTRICAL STRESS SCREENING 19
3.5 CONTROL SIGNALS 10
3.6 TRM CONNECTION CONTROL TABLE 13
3.7 CONNECTORS 14
3.8 POWER SUPPLIES 14
3.9 RF TEST SOURCES REQUIRED 14

4 TEST METHODS 15

4.1 VISUAL 15
4.2 MECHANICAL 15
4.3 ELECTRICAL 15
4.3.1 Calibration Procedure 15

Figures

Figure 1-1. T/R module functionality block diagram.....7
Figure 3-1. T/R module ICD (preliminary).....9
Figure 3-2 Connector Pin Numbering Scheme 14

Tables

Table 2-1 Tests and measurements 18
Table 2-2 Measurement Method and Number of Measurement Points for LFT tests.....20
Table 2-3 LFT Tests.....23
Table 2-4 FFT Tests.....25
Table 2-5 EFT Tests.....25
Table 2-6 DVT Tests 26
Table 2-7 Tests and measurements 26
Table 3-1 Electrical Stress Screening Regime 20
Table 3-2 Logic Definition 10
Table 3-3 Control Definition.....10
Table 3-4 Temperature Monitor Bus Connections.....11
Table 3-5 Temperature Monitor Specifications 12
Table 3-6 Temperature-to-Digital Transfer Function 12
Table 3-7 Connector Control Table 13
Table 4-2 I^2C Programming worked example..... **Error! Bookmark not defined.**

References

[1] ETS 300 019-1-4: ETSI "EE; Environmental conditions and environmental test for telecommunications equipment; Part 1-4: Classification of environmental conditions stationary use at non-weather protected locations.

[2] RBWAN: Environmental Requirements Specification, 02-206vxx*

[3] RBWAN: Ka-Band T/R Module Specification (2:1 type) 06-402vxx*

[4] RBWAN: Test Specification for Switch and Decoupling PCB 07-122vxx*

[5] RBWAN: Test Specification for Control and Regulator PCB 07-123vxx*

[6] RBWAN: Assembly and Production Instructions for the T/R module 08-100vxx*

xx* = Latest Issue

Abbreviations/Terms Used

ATE	Automatic Test Equipment Testing
BER	Bit Error Rate
DVT	Design Verification Tests
E-FFT	Extended Full Functional Tests
FFT	Full Functional Tests
ICD	Interface Control Drawing
Ka Band	Refers to bands 24.25 to 29.5GHz
LFT	Limited Functional Tests
MIP	Mesh Insertion Point (connects)
ODU	Out Door Unit
RBWAN	Radiant Broadband Wireless Access Network
TBD	To Be Decided/Determined
TBC	To Be Confirmed
TRM	Transmit Receive Module
ICT	In Circuit Test
ESS	Electrical Stress Screening

1 Introduction

This document defines the test specification and test plan for use on TRMs within the Band –1 and Band –2 products used within the Radiant Broadband Wireless Access Network (RBWAN).

1.1 System Description

The RBWAN is essentially multipoint-to-multipoint radio links configured in a mesh structure. Each user node handles both its own traffic and also relays traffic between the surrounding nodes, so there are no base stations. As nodes are added to or removed from the mesh, the network needs to dynamically reconfigure. For high node density and maximum frequency reuse narrow beam antennas are required, therefore to achieve reconfiguration it is necessary to steer the antenna in the azimuth plane. Four steerable mm-wave antennas will be mounted within radomes' enclosure. These antennas will be free to rotate in the azimuth plane over the entire 360°.

1.2 Transmit Receive Module

The active TRM is the most costly of assemblies within the millimetric section, and also consists of two sub assemblies, a conventional regulation and control board, and the RF/DC hybrid board. The conventional board is assembled tested and presented to the TRM assembly as BOM part. The RF/DC hybrid has the DC side assembled and tested as a part of the TRM assembly procedure.

ICT and functional testing of the conventional board and DC side of RF/DC hybrid board will guarantee DC operation of the TRM DC electronics, so any initial DC level failure at TRM test level is associated with RF electronics.

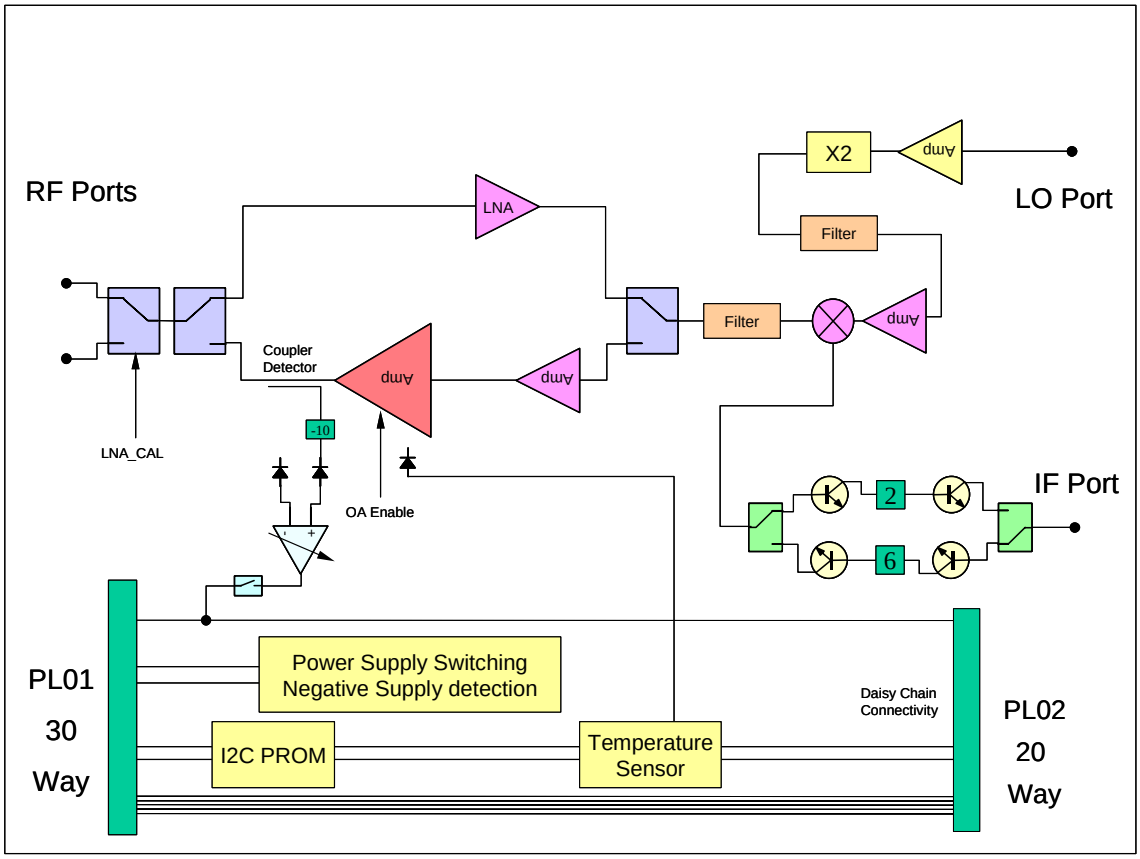

Figure 1-1. T/R module functionality block diagram

1.3 Test Philosophy

The scope of this document is to specify RBWAN ODU antenna and radome test requirements for use in different stages of the product cycle. For this reason the document covers different levels of test and refers to DVT and ATE processes. The tests are defined at three different levels listed below:

i. Limited Functional Tests (LFT)

ii. Full Functional Tests (FFT)

iii. Extended FFT (EFFT)

The extent of each test can be readily observed by referring to relevant test matrices. The objective in LFT is to exercise basic tests (and inspection where applicable) to achieve the required level of confidence in quality and performance of the product in a cost effective manner. FFT is the more extensive test performed in product development phases and exercised on a small part of a production batch, typically 5 to 10% on batches of 1K to 10K pieces. The percentage sharply falls to coupon samples in volume production. E-FFT includes added

environmental test that forms the key test in product and process proving. The tests will be conducted in product development and process proving stages.

Production tests are integral part of the manufacturing process. In addition to Design Verification Tests (DVTs) established ATE techniques shall be deployed to ensure correct manufacturing and minimize reject levels on value added hardware. Routine production tests will be carried out at LFT levels. However FFT and E-FFT test levels will be carried out on smaller samples, on batch basis for process validations and checks.

Where appropriate manufacturer may have the option to negotiate further reduction in test levels. This will depend on process robustness and benefits of such trade offs!

1.4 Design Verification Test (DVT) Aim

The aim of DVT tests are to prove that functionality provided by a DUT matches to its specification. The results are recorded in a compliance table and compared against the requirements laid in the corresponding specifications.

1.5 Production Test Aim

The aim of production test is to prove that the specified hardware component has been manufactured correctly. This is confirmed by a limited set of tests and measurements integrated into the production flow. These tests are planned and configured to enable uninterrupted production run unless a fault or non-compliance to specifications is detected.

1.6 Testing Aims

The aim is to ensure that the DUT is designed and manufactured to meet all requirements stated in the corresponding requirements specifications [1] and [2]. The test sequence and procedure shall be such that it will provide fault and none compliance detection at the earliest possible point.

2 Requirements Specifications

In the following text if a conflict arises between the requirements specifications listed in the References section and the specifications listed below the Reference documents shall take precedence.

2.1 Electrical Specification [3]

The electrical specification is detailed in 06_402 (latest issue) Ka-Band T/R Module Specification (2:1 Type) section 2.2 and the test matrix with refer to this document

2.2 Mechanical Specification [3]

The mechanical specification is detailed in 06_402 (latest issue) Ka-Band T/R Module Specification (2:1 Type) section 2.3 and the test matrix with refer to this document.

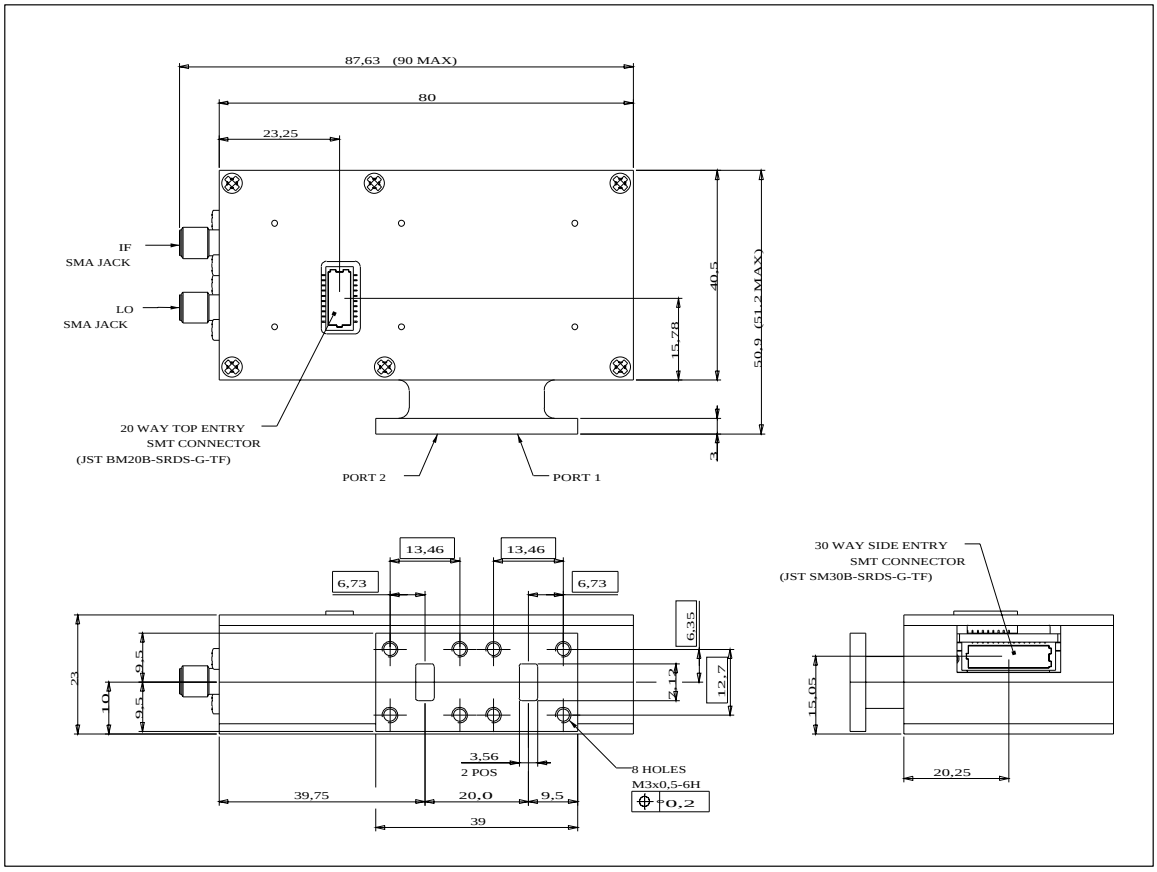

Figure 2-1. T/R module ICD

2.3 Environmental Specification [2]

The environmental specification is detailed in 02_206 (latest issue) Environmental Requirements Specification (2:1 Type) section 2.4 and the test matrix with refer to this document

2.4 Control Signals

2.4.1.1 Logic Inputs

All control functions shall be driven by differential inputs, each control shall have a plus input (P) and a minus input (M). The TRM will default to state 1 if no control signal is supplied.

Parameter	Specification
Input Voltage	-0.3V to +5.5V (P or M)
Input Resistance	7kΩ min (P or M)
Input Current	+/-700μA max (P or M)
TRM Default State, no input	Control State 1
Maximum Differential Input	+/-5.8V (P-M)
State 0	< -0.2V (P-M)
State 1	> +0.2V (P-M)

Table 2-1 Logic Definition

Function	Description	State	Action
MM_TRSel	T/R select	0	Receive
		1	Transmit
MM_APSel	Antenna Port Selection	0	RF Port 1
		1	RF Port 2
MM_RxEn	Rx Amplifier enable	0	Rx Amplifier on
		1	Rx Amplifier off
MM_PAEn	Tx PA enable	0	Tx PA on
		1	Tx PA off

Table 2-2 Control Definition

T/R Select sets the state of the RF and IF T/R switches. Antenna select sets the RF waveguide port to be used. Rx and PA enables control bias modulation/switching to be performed in timed sequence to best meet the module settling time requirements. The ODU controller can provide time sequencing of controls in accordance to requirements specified by the MM T/R Module design authority. Provided all the specifications and functionality can be met it is not mandatory to use all the controls within the MM T/R Module, this is just a statement of intended control signal provision. It would be beneficial at system level to minimise interconnects to the MM T/R Module.

2.4.1.2 Detector output Gain adjustment

An RF detector is coupled to the transmit power amplifier output. The detector output voltage is amplified and provided at the DC1 connector. Voltage measurements are performed by measuring the difference between V_{OUT} with RF_{ON} and V_{OUT} with RF_{OFF}. In this way detector offsets are removed. The detector output should always be positive voltage. Provision is made for trimming the detector voltage by a digital potentiometer, which is controlled by a single digital input, DC1 pin 30 (see Dallas semiconductor data sheet DS1669-010 for control of the potentiometer).

The potentiometer position can be adjusted by input of logic 0 pulses to the TRM DC1, pin 30, pulses should not be sent more rapidly than 1ms intervals. Alternatively the input, pin 30 can be held low and the DS1669 will increment every 100ms. When the DS1669 gets to the max or minimum range it reverses direction. The DS1669 has 64 possible states.

The detector output is only active when the transmit amplifier is enabled. When the output amplifer is not enabled the detector output is high impedance. When two TRMs are joined together in the daisy chain function the Detector outputs are connected together but only one TRM is active at any one time and the active transmit TRM takes control of the single detector output.

2.4.1.3 Temperature Sensor and Protection Circuit

The internal temperature of the TRM shall be measured and relayed to external circuits via an I²C interface bus. The TRM should be shut down if exposed to conditions outside a programmable safe operating temperature range and an interrupt signal to alert this condition should also be provided. The data and command format shall be equivalent to that used in the National Semiconductor LM83.

The Temperature setpoint for the shut down flag (T_CRIT or INT on the LM83) is programmable via the I^2C (for further details see the National Semiconductor datasheet LM83). The T_CRIT and INT functions of the LM83 are wired together to the TRM SIN (Pin 15, 30 way connector) and this is also wired to the daisy chain connector so that the SIN line will report if any TRM or and LM83 functions go above the programmed critical temperature. If no critical temperature is programmed the LM83 critical temperature point will default to 127°C on power up.

Name	Function
MM_SCL	I²C Clock input
MM_SDA	I²C Data I/O (Serial)
MM_SIN	Thermal Alert Interrupt

Table 2-3 Temperature Monitor Bus Connections

Parameter	Specification
Measurement Range	10°C above and below TRM operating temp. TBC
Measurement Resolution	1°C
Measurement Accuracy	+/-4°C

Digital Range	7 bit + MSB polarity (8 bit total)
MSB Polarity	'1' < 0°C
Data '1'	+2.1V to +3.6V
Data '0'	0V to +0.8V
Clock Input Frequency	10kHz to 100kHz
Interrupt State	'0'
I²C Address (7bit)	TBD, 1 bit factory settable
Command and Register Format	LM83 Equivalent

Table 2-4 Temperature Monitor Specifications

Measured Temperature	Digital Codeword
+125°C	01111101
0°C	00000000
-1°C	11111111
-55°C	11001001

Codeword increases linearly from –55 to -1°C and 0 to +125°C

Table 2-5 Temperature-to-Digital Transfer Function

2.5 TRM Connection Control Table

No	Function	Description	Primary Connector	Secondary Connector
1	RF1	mm-wave interface to antenna #1	WG22 #1	-
2	RF2	mm-wave interface to antenna #2	WG22 #2	-
3	IF1	First IF	SMA #1	-
4	LO1	Half LO frequency (LO/2)	SMA #2	-
5	MM_TRSel_M	LNA Cal (minus)	DC1, Pin #01	DC2, Pin #01
6	MM_TRSel_P	LNA Cal (plus)	DC1, Pin #02	DC2, Pin #02
7	MM_APSel_M	Antenna Port Select (minus)	DC1, Pin #03	DC2, Pin #03
8	MM_APSel_P	Antenna Port Select (plus)	DC1, Pin #04	DC2, Pin #04
9	MM_PAAEn_M	TRMA Power Amp Enable (minus)	DC1, Pin #05.	-
10	MM_PAAEn_P	TRMA Power Amp Enable (plus)	DC1, Pin #06.	-
11	MM_PABEn_M	TRMB Power Amp Enable (minus)	DC1, Pin #07	DC2, Pin #07
12	MM_PABEn_P	TRMB Power Amp Enable (plus)	DC1, Pin #08	DC2, Pin #08
13	MM_RxAEn_M	TRMA Receive Amp Enable (minus)	DC1, Pin #09	-
14	MM_RxAEn_P	TRMA Receive Amp Enable (plus)	DC1, Pin #10	-
15	MM_RxBEn_M	TRMB Receive Amp Enable (minus)	DC1, Pin #11	DC2, Pin #11
16	MM_RxBEn_P	TRMB Receive Amp Enable (plus)	DC1, Pin #12	DC2, Pin #12
17	MM_SCL	Serial Clock	DC1, Pin #13	DC2, Pin #13
18	DC Ground	DC Ground	DC1, Pin #14	DC2, Pin #14
19	MM_SIN	Serial Interrupt	DC1, Pin #15	DC2, Pin #15
20	MM_SDA	Serial Data	DC1, Pin #16	DC2, Pin #16
21	DC Ground	DC Ground	DC1, Pin #17	DC2, Pin #18
22	MM_TxMA_S	TRM Transmit Monitor (signal)	DC1, Pin #18	DC2, Pin #20
23	DC Ground	DC Ground	DC1, Pin #19	DC2, Pin #19
24		No Connect	DC1, Pin #20	
25	VP1	Positive power supply #1	DC1, Pins #21 & 22	DC2, Pins #05 & 06
26	GND	DC Ground	DC1, Pin #23	DC2, Pin #9
27	VN1	Negative power supply	DC1, Pin #24	DC2, Pin #10
28		No Connect	DC1, Pin #25	
29	MM_SWC	Serial Write Control	DC1, Pin #26	-
30		No Connect	DC1, Pin #27	
31	MM_SET	Serial Address Set Ground	DC1, Pin #28	-
32	MM_SAD	Serial Address Set	DC1, Pin #29	-
33	Detector Gain	Digital Input D	DC1, Pin #30	

Table 2-6 Connector Control Table

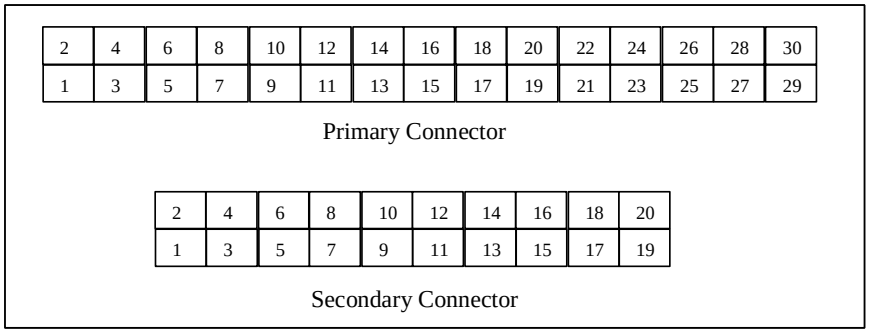

Figure 2-2 Connector Pin Numbering Scheme

2.6 Connectors

RF Connections

RF1 and RF2 connections are made by Waveguide 22 connection

IF1 and LO1 connectors are standard SMA.

DC Connections

The dc connector types used on the TRM are manufactured by JST:

20 Way JST BM20B-SRDS-G-TF

30 Way JST SM30B-SRDS-G-TF

To connect to these connectors the following test connectors may be used:

20 Way Shell SHDR-20V-S-B

30 Way Shell SHDR-30V-S-B

Crimp Contact SSH-003GA-P0.2

2.7 Power Supplies

The following power supplies should be available for test of the TRM:

6.5V ± 0.1V, 1.5 A

-8.0V ± 0.1V, 0.25 A

2.8 RF Test Sources Required

The following RF test sources are required:

RF1 24,000 to 30,000 MHz, 1 MHz steps, -81dBm to 0dBm, 1dB steps

RF2 24,000 to 30,000 MHz, -81dBm to 0dBm, 1dB steps

RF3 10,000 to 13,000 MHz, 0dBm to +4dBm, 1dB steps

Noise source 1 24,000 to 30,000 MHz

3 Test Methods

The Production contractor shall produce a test plan detailing the test methods and equipment used. The production contractor shall work out and state magnitude of the measurement errors of equipment used. The test plan shall be submitted to Radiant PLC for approval prior to shipment of any production hardware.

3.1 Visual

Visual inspection is required at final RF assembly to ensure that the MMIC die have been correctly bonded and have been undamaged by the assembly process. It is also necessary as it is impractical to perform any pre-checks to the MMIC parts. A visual check that the test lids have been correctly fitted.

3.2 Mechanical

Mechanical checks of alignment of SMA and DC interfaces and wave guide ports.

3.3 Electrical

Standard test techniques may be used to demonstrate unit compliance to requirement specification.

3.3.1 Calibration Procedure

The Calibration data can be calculated for the results taken in the LFT tests and is programmed into the PROM in the TRM via the I^2C bus at the end of the test. The data loaded is a mixture of data about the hardware build standard and electrical test results. The data required is defined in table 2.2 and is loaded in the following format.

The PROM has an address bit (Pin 29, SAD) which should be set to 0 and a write control pin (Pin 26, SWC) which should also be set to 0 for writing data.

TRM EEPROM data

0x78	tag for ODU TRM configuration
0x80	record of unknown length
0x40	tag for P/N
0x06	record length 6 bytes
0x 38 38 31 30 32 30	“881020”
0x41	tag for issue
0x02	length
0x 20 44	“ D” (space D)
0x42	tag for Mod State
0x02	length
0x 20 20	“ “ (two spaces for unknown)
0x43	tag for S/N
0x06	length
0x 30 30 30 30 30 xx	“00000x” – variable

0x44	tag for date code
0x06	length
0x 30 35 30 36 30 31	"050601" – 5 Jun 2001
0x45	tag for site code
0x01	length
0x41	"A"
0x4A	tag for TRM Cal data block
0xC0	141 bytes: 11 x 32-bit integers: version, P1dB, NF, Freq, CalP 4 x 8-bit integers (NumP, Lomult, spare1, spare2) 48 x 8-bit integers P1 detector, 48 for P2
0x 07 00 00 00	version 7 (LSByte first) – version of TRM Cal data structure
0x nn nn nn nn	P1dB at Min Freq: 10 x dBm as signed integer-32 LSByte first
0x nn nn nn nn	P1dB at Mid Freq: 10 x dBm as signed integer-32 LSByte first
0x nn nn nn nn	P1dB at Max Freq: 10 x dBm as signed integer-32 LSByte first
0x nn nn nn nn	NF at Min Freq: 10 x dB as unsigned integer-32 LSByte first
0x nn nn nn nn	NF at Mid Freq: 10 x dB as unsigned integer-32 LSByte first
0x nn nn nn nn	NF at Max Freq: 10 x dB as unsigned integer-32 LSByte first
0x nn nn nn nn	Min Frequency in 100kHz units as unsigned integer-32 LSByte first
0x nn nn nn nn	Max Frequency in 100kHz units as unsigned integer-32 LSByte first
0x nn nn nn nn	Step Frequency in 100kHz units as unsigned integer-32 LSByte first
0x nn nn nn nn	Cal Output Power 100 x dBm units as unsigned integer-32 LSByte first
0x 02	Number of antenna ports: unsigned integer-8
0x 02	LO Multiplier Number: unsigned integer-8
0x 02	Spare 1: unsigned integer-8
0x 02	Spare 2: unsigned integer-8
0x nn	voltage x 255/3.3 – voltage for <Cal Output Power> output at <Min Freq> as above, step <StepFreq> to <MaxFreq> (spare values to make 48 points of int-8) and similar block for Port 2
0x 01 00 00 00	version 1 (LSByte first) – version of Antenna data structure
0x nn nn nn nn	Antenna overlap angle in units of 0.25 degrees
0x 01 00 00 00	1st antenna type (1 = rotating, 2 = fixed)
0x 01 00 00 00	2nd antenna type (1 = rotating)
0x 01 00 00 00	3rd antenna type (1 = rotating)
0x 01 00 00 00	4th antenna type (1 = rotating)
0x 00 00 00 00	5th antenna type (0 = none)
0x 00 00 00 00	6th antenna type (0 = none)
0x 00 00 00 00	7th antenna type (0 = none)
0x 00 00 00 00	8th antenna type (0 = none)
0x00	null tag
0x00	null length (end of data marker)

233 bytes total (at this revision)

example p1dB = 26.5dBm => 265 stored => 00000000 00000000 00000001 00001001
=> 00 00 01 09

store as 09 01 00 00

```
struct st_mo_cal_trm_v7 // receiving data structure for TRM board (at rev 7)
{
    unsigned int version;   /* Should be '7' */
    int p1_dbm_min;    /* In 0.1 dbm values */
    int p1_dbm_mid;
```

```
    int p1_dbm_max;
    unsigned int nf_db_min;                 // In 0.1 db values
    unsigned int nf_db_mid;
    unsigned int nf_db_max;
    unsigned int freq_min;          // units = 0.1MHz
    unsigned int freq_max;          // units = 0.1MHz
    unsigned int freq_step;         // units = 0.1MHz
    unsigned int cal_power_dbm;             // units = 0.01 dBm
    unsigned char num_antenna_ports;        // 1 or 2
    unsigned char lo_multiplier;            // 2
    unsigned char spare1;           // set to 0 if not needed
    unsigned char spare2;           // set to 0 if not needed
    unsigned char v_qpsk_p1[48];            // voltage x 255/3.3 into 8-bit integer
    unsigned char v_qpsk_p2[48];             // voltage x 255/3.3 into 8-bit integer
 };

struct st_mo_cal_antenna_v1
{
        unsigned int version;                           // 1
        unsigned int overlap_angle;                     // 0.25 degree units
        unsigned int ant_type[8];               // type of antenna: 0=none, 1=rotating, 2=fixed
} ;
```

4 Transmit Receive Modules Test Levels

The tests and measurements shall be conducted at 3 different levels:

LFT: The objective is to exercise basic tests and measurements to ensure smooth production and high yield. This shall be done in a cost effective manner.

FFT: FFT is the more extensive test performed in product development phases and exercised on a small part of a production batch, typically 5 to 10% on batches of 1K to 10K pieces. The percentage sharply falls to coupon samples in volume production.

EFT: EFT includes environmental test. These tests will be conducted in product development and process proving stages.

The following table defines criteria of tests required with respect to batch volume.

Batch Size	LFT	FFT	EFT
1-99	100%	10%	1%
100-999	100%	5%	1%
1000-9999	100%	1%	0.1%
>10000	100%	0.1%	0.01%

Table 4-1 Tests and measurements

4.1 Summary of Test Stages

This section defines the different tests required for different designations. The designations are determined by batch sizes given in table 2.1. The objective of LFT is to exercise basic tests (and inspection where applicable) to achieve the required level of confidence in quality and performance of the product in a cost effective manner. FFT is the more extensive test performed in product development phases and exercised on a small part of a production batch. The percentage sharply falls to coupon samples in volume production. E-FFT includes added environmental test that forms the key test in product and process proving. The tests will be conducted in product development and process proving stages.

The following matrix shows a summary of the tests required for each test level.

Test/Inspection	LFT	FFT	EFT	DVT
Electrical Stress Screening ESS	☑			
Visual Inspection	☑			
Gain/flatness/switch isolation/tracking/Frequency Tx	☑			
Gain/NF/flatness/tracking/Frequency Rx	☑			
P1db Tx	☑			

Test/Inspection	LFT	FFT	EFT	DVT
Detector Levels at +20dBm output	☑			
Temperature Sensor Function	☑			
Power Supply Currents	☑			
Daisy Chain Connectivity	☑			
Calibration Table loaded into E^2 PROM	☑			
TRM Temperature Performance (all LFT tests at -35, 0, +20, +40, +75 ^oC) (oven ambient temperature)		☑		

4.2 Assembly / Test Flow

The following procedure shall be used for assembly test flow

1. DC Test RF/DC Hybrid Assembly PCB
2. Assemble Microwave Circuit
3. Visual Inspection
4. Assemble Lid
5. Functional Test (LFT)
6. Electrical Stress Screen Procedure (ESS)
7. Functional Test (LFT)
8. Sample Tests, FFT and EFT

4.3 Electrical Stress Screening

The following regime shall be used on the TRM prior to LFT final test.

06_402 Para No.	Parameter	Min	Max	Units
ESS Tests				
Temperature Cycling	5.5 cycles oven temperature -35^{o}C to +75^{o}C, first half cycle hot, 10mins dwell at extremes, 5 ± 1^{o}C oven ramp rate, log data every 2 minutes.			
2.2.3.6	Date and time of test			
2.2.3.6	Power Supply On			
2.2.3.6	Oven Temperature			
2.2.3.6	Temperature Sensor Function Chip, internal sensor, difference from ambient	-20	20	C
2.2.3.6	Temperature Sensor Function, RF board sensor, difference from ambient	-20	20	C
2.2.3.4	Current, 6.5 V Rail, Tx Amps On, select Port 1, select Tx	820	1000	mA

2.2.3.4	Current, -8.0 V Rail Tx Amps On,select Port 1, select Tx	10	20	mA
2.2.3.4	Current, 6.5 V Rail, all amps off, select Port 1, select Tx	200	270	mA
2.2.3.4	Current, -8.0 V Rail, all amps off,select Port 1, select Tx	5	15	mA
2.2.3.4	Current, 6.5 V Rail, all amps off, select Port 1, select Rx	230	320	mA
2.2.3.4	Current, -8.0 V Rail, all amps off,select Port 1, select Rx	5	15	mA
	Current, 6.5 V Rail, all amps off, select Port 2, select Rx	230	320	
	Current, -8.0 V Rail, all amps off,select Port 2, select Rx	5	15	
2.2.3.6	Power Supply Off			

Table 4-2 Electrical Stress Screening Regime

No failures are permitted during ESS testing. If a failure occurs the unit may be reworked but should repeat the ESS procedure.

Where measurements are performed data shall be recorded for analysis at a later date. The format for the data files produced shall be as section 2.7.

4.4 Limited Functional Test (LFT)

All limited functional tests and measurements shall be carried out at room temperature of 22°±3°C unless otherwise stated. Limited functional tests will include tests and measurements defined in table 2.1.

06_402 Specification para. No.	Parameter	Measurement Method and Number of measurements
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, 20dBm o/p	Measured 50MHz steps, IF = 4070.5 MHz, record measurement array
2.2.1.4	Tx, 50MHz Channel Flatness Window	Calculated from conversion gain results array
2.2.1.4	Tx Switch Isolation	Measure leakage power at Port 1 while transmitting to Port 2, terminate Port 2
2.2.1.5	Tx, P-1dB o/p, Port 1	record measurement array 0.25GHz intervals, P_{OUT}, V_{OUT} at Pin = -30 to -10 dBm 1dB intervals
2.2.1.9	Tx, Detector, Vout at Tx P_{OUT} = +20dBm, select Port 1	$V_{OUT} = V_{(TX=+20dBm)} - V_{(TX=RF\_OFF)}$
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, Port 1	measured 50MHz steps, IF = 4070.5 MHz, record measurement array
2.2.3.3	Daisy Chain Connectivity	Check connection resistance and for short circuits to ground
2.2.3.7	Calibration Table loaded into E^2 PROM	load in cal table, read back and check numbers against the write numbers

Table 4-3 Measurement Method and Number of Measurement Points for LFT tests

Table 2.3 defines the LFT tests to be performed:

06_402 Specification para. No.	Parameter	Min	Max	Units
	Electrical Stress Screening ESS	Pass		P/F
	Visual Inspection	Pass		P/F
Tx Functions				
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, 20dBm o/p, Port 1	44		dB
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, 20dBm o/p, Port 1		53	dB
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, 20dBm o/p, Port 2	44		dB
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, 20dBm o/p, Port 2		53	dB
2.2.1.4	Tx, Conversion Gain Frequency Variation 27.5 to 29.5GHz, Port 1		6.5	dB
2.2.1.4	Tx, Conversion Gain Frequency Variation 27.5 to 29.5GHz, Port 2		6.5	dB
2.2.1.4	Tx Conversion Gain, Port tracking (Port 1 gain - Port 2 gain)		3	dB
2.2.1.4	Tx, 50MHz Channel Flatness Window, Port 1		0.5	dB
2.2.1.4	Tx, 50MHz Channel Flatness Window, Port 2		0.5	dB
2.2.1.4	Tx Switch Isolation Port 1	27		dB
2.2.1.4	Tx Switch Isolation Port 2	27		dB
2.2.1.5	Tx, P-1dB o/p, Port 1	24		dBm
2.2.1.5	Tx, P-1dB o/p, Port 1		28	dBm
2.2.1.5	Tx, P-1dB o/p, Port 2	24		dBm
2.2.1.5	Tx, P-1dB o/p, Port 2		28	dBm
2.2.1.9	Tx, Detector, Vout at Tx Pout = +20dBm, select Port 1	0.586	2.336	V
2.2.1.9	Tx, Detector, Vout at Tx Pout = +20dBm, select Port 2	0586	2.336	V
2.2.1.9	Tx, Detector, Vout Pin = OFF, select Port 1	0	0.3	V
2.2.1.9	Tx, Detector, Vout Pin = OFF, select Port 2	0	0.3	V
Rx Functions				
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, Port 1	24		dB
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, Port 1		30	dB
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, Port 2	24		dB
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, IF = 4070.5 MHz, Port 2		30	dB
2.2.2.4	Rx, Conversion Gain, Frequency Variation 27.5 to 29.5GHz, Port 1		4	dB
2.2.2.4	Rx, Conversion Gain, Frequency Variation 27.5 to 29.5GHz, Port 2		4	dB
	Rx Conversion Gain, Port tracking (Port 1 gain - Port 2 gain)		3	dB
2.2.2.4	Rx, 50MHz Channel Flatness Window, Port 1		0.5	dB
2.2.2.4	Rx, 50MHz Channel Flatness Window, Port 2		0.5	dB

06_402 Specification para. No.	Parameter	Min	Max	Units
2.2.2.5	Rx Noise Figure, Port 1		6	dB
2.2.2.5	Rx Noise Figure, Port 2		6	dB
Control and DC Functions				
2.2.3.3	Daisy Chain Connectivity	Pass		
2.2.3.4	Current, 6.5 V Rail, Tx Amps On, select Port 1, select Tx		950	mA
2.2.3.4	Current, -8.0 V Rail Tx Amps On,select Port 1, select Tx		20	mA
2.2.1.10	Current, 6.5 V Rail, all amps off, select Port 1, select Tx		270	mA
2.2.1.10	Current, -8.0 V Rail, all amps off,select Port 1, select Tx		15	mA
2.2.2.10	Current, 6.5 V Rail, all amps off, select Port 1, select Rx		270	mA
2.2.2.10	Current, -8.0 V Rail, all amps off,select Port 1, select Rx		15	mA
2.2.2.10	Current, 6.5 V Rail, all amps off, select Port 2, select Rx		270	mA
2.2.2.10	Current, -8.0 V Rail, all amps off,select Port 2, select Rx		15	mA
2.2.2.10	Current, 6.5 V Rail, Rx Amp On, select Port 1, select Rx		300	mA
2.2.2.10	Current, -8.0 V Rail, Rx Amp On, select Port 1, select Rx		15	mA
2.2.3.6	Temperature Sensor Function Chip, internal sensor, difference from ambient	-20	20	C
2.2.3.6	Temperature Sensor Function, RF board sensor, difference from ambient	20	20	C
2.2.3.7	Calibration Table loaded into E^2 PROM	Pass		
2.2.3.7	881020, Part Number			bit
2.2.3.7	xxxxxx, Issue Number			bit
2.2.3.7	xxxxxx, Modification State			bit
2.2.3.7	xxxxxx, Serial Number			bit
2.2.3.7	ddmmyy, Date Code			bit
2.2.3.7	xxxxxx, Site Code			bit
2.2.3.7	10 x Tx P1dB at 27.5GHz	240	280	bit
2.2.3.7	10 x Tx P1dB at 28.5GHz	240	280	bit
2.2.3.7	10 x Tx P1dB at 29.5GHz	240	280	bit
2.2.3.7	10 x Rx NF at 27.5GHz	0	60	bit
2.2.3.7	10 x Rx NF at 28.5GHz	0	60	bit
2.2.3.7	10 x Rx NF at 29.5GHz	0	60	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=27.50 GHz, Port 1	64	255	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=27.55 GHz, Port 1	64	255	bit
2.2.3.7		64	255	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=29.45 GHz, Port 1	64	255	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=29.45 GHz, Port 1	64	255	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=27.50 GHz, Port 2	64	255	bit

06_402 Specification para. No.	Parameter	Min	Max	Units
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=27.55 GHz, Port 2	64	255	bit
2.2.3.7		64	255	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=29.45 GHz, Port 2	64	255	bit
2.2.3.7	(256 x Vout)/3.3 at Pout=+20dBm at F=29.45 GHz, Port 2	64	255	bit

Table 4-4 LFT Tests

4.5 Full Functional Tests (FFT)

06_402 Specification para. No.	Parameter	Min	Max	Units
Temperature Tests	TRM Temperature Performance at -20, 0, +20, +40, +60 ^{o}C			
Tx Functions				
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, 20dBm o/p, Port 1	40		dB
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, 20dBm o/p, Port 1		57	dB
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, 20dBm o/p, Port 2	40		dB
2.2.1.4	Tx Conversion Gain, 27.5 to 29.5GHz, 20dBm o/p, Port 2		57	dB
2.2.1.4	Tx Conversion Gain, Port tracking (Port 1 gain - Port 2 gain)		3	dB
2.2.1.4	Tx, Frequency Variation 27.5 to 29.5GHz, Port 1		6.5	dB
2.2.1.4	Tx, Frequency Variation 27.5 to 29.5GHz, Port 2		6.5	dB
2.2.1.4	Tx, 50MHz Channel Flatness Window, Port 1		0.5	dB
2.2.1.4	Tx, 50MHz Channel Flatness Window, Port 2		0.5	dB
2.2.1.4	Tx Switch Isolation Port 1	27		dB
2.2.1.4	Tx Switch Isolation Port 2	27		dB
2.2.1.5	Tx, P-1dB o/p, Port 1	22		dBm
2.2.1.5	Tx, P-1dB o/p, Port 1		28	dBm
2.2.1.5	Tx, P-1dB o/p, Port 2	22		dBm
2.2.1.5	Tx, P-1dB o/p, Port 2		28	dBm
2.2.1.6	Tx o/p power, Min 24dB C/I, Port 1	15		dBm
2.2.1.6	Tx o/p power, Min 24dB C/I, Port 2	15		dBm
2.2.1.6	Tx o/p power, Min 32dB C/I, Port 1	11		dBm
2.2.1.6	Tx o/p power, Min 32dB C/I, Port 2	11		dBm
2.2.1.6	Tx o/p power, Min 40dB C/I, Port 1	7		dBm
2.2.1.6	Tx o/p power, Min 40dB C/I, Port 2	7		dBm
2.2.1.9	Tx, Detector, Vout at Tx Pout = +20dBm, select Port 1	0.586	2.336	V
2.2.1.9	Tx, Detector, Vout at Tx Pout = +20dBm, select Port 2	0.586	2.336	V
2.2.1.9	Tx, Detector, Vout Pin = OFF, select Port 1	0	0.3	V
2.2.1.9	Tx, Detector, Vout Pin = OFF, select Port 2	0	0.3	V

06_402 Specification para. No.	Parameter	Min	Max	Units
Rx Functions				
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, Port 1	22.5		dB
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, Port 1		31.5	dB
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, Port 2	22.5		dB
2.2.2.4	Rx, Conversion Gain, 27.5 to 29.5GHz, Port 2		31.5	dB
2.2.2.4	Rx Conversion Gain, Port tracking (Port 1 gain - Port 2 gain)		3	dB
2.2.2.4	Rx, Conversion Gain, Frequency Variation 27.5 to 29.5GHz, Port 1		4	dB
2.2.2.4	Rx, Conversion Gain, Frequency Variation 27.5 to 29.5GHz, Port 2		4	dB
2.2.2.4	Rx, 50MHz Channel Flatness Window, Port 1		0.5	dB
2.2.2.4	Rx, 50MHz Channel Flatness Window, Port 2		0.5	dB
2.2.2.5	Rx Noise Figure, Port 1		7	dB
2.2.2.5	Rx Noise Figure, Port 2		7	dB
Control and DC Functions				
2.2.3.3	Daisy Chain Connectivity	Pass		
2.2.3.4	Current, 6.5 V Rail, Tx Amps On, select Port 1, select Tx		950	mA
2.2.3.4	Current, -8.0 V Rail Tx Amps On,select Port 1, select Tx		20	mA
2.2.1.10	Current, 6.5 V Rail, all amps off, select Port 1, select Tx		270	mA
2.2.1.10	Current, -8.0 V Rail, all amps off,select Port 1, select Tx		15	mA
2.2.2.10	Current, 6.5 V Rail, all amps off, select Port 1, select Rx		270	mA
2.2.2.10	Current, -8.0 V Rail, all amps off,select Port 1, select Rx		15	mA
2.2.2.10	Current, 6.5 V Rail, all amps off, select Port 2, select Rx		270	mA
2.2.2.10	Current, -8.0 V Rail, all amps off,select Port 2, select Rx		15	mA
2.2.2.10	Current, 6.5 V Rail, Rx Amp On, select Port 1, select Rx		300	mA
2.2.2.10	Current, -8.0 V Rail, Rx Amp On, select Port 1, select Rx		15	mA
2.2.3.6	Temperature Sensor Function Chip, internal sensor, difference from ambient	-20	20	C
2.2.3.6	Temperature Sensor Function, RF board sensor, difference from ambient	-20	20	C
Temperature Results analysis				
2.2.1.4	Tx Conversion Gain, Temperature Variation at any frequency over -20 to +60°C 20°C as reference, 13dBm o/p	-3.5		dB
2.2.1.4	Tx Conversion Gain, Temperature Variation at any frequency over -20 to +60°C 20°C as reference, 13dBm o/p		3.5	dB
2.2.2.4	Rx Conversion Gain, Temperature Variation at any frequency over -20 to +60°C 20°C as reference	-2.5		dB

06_402 Specification para. No.	Parameter	Min	Max	Units
2.2.2.4	Rx Conversion Gain, Temperature Variation at any frequency over -20 to +60°C 20°C as reference		2.5	dB
Additional 25C testing				
2.2.1.4	Tx Conversion Gain, IF Flatness window IF = 4045.5 to 4095.5 MHz, 20dBm o/p, Port 1		0.5	dB
2.2.1.4	Tx Conversion Gain, IF Flatness window IF = 4045.5 to 4095.5 MHz, 20dBm o/p, Port 2		0.5	dB
2.2.1.4	Rx Conversion Gain, IF Flatness window IF = 4045.5 to 4095.5 MHz, 20dBm o/p, Port 1		0.5	dB
2.2.1.4	Rx Conversion Gain, IF Flatness window IF = 4045.5 to 4095.5 MHz, 20dBm o/p, Port 2		0.5	dB
2.2.1.11	Return Loss, Port 1 Tx	10		dB
2.2.1.11	Return Loss, Port 2 Tx	10		dB
2.2.1.11	Return Loss, IF Port Tx	10		dB
2.2.1.11	Return Loss, LO Port	10		dB
2.2.2.11	Return Loss, Port 1 Rx	10		dB
2.2.2.11	Return Loss, Port 2 Rx	10		dB
2.2.2.11	Return Loss, IF Port Rx	10		dB

Table 4-5 FFT Tests

4.6 Extended Functional Test (EFT)

06_402 Specification para. No.	Parameter	Min	Max	Units
2.2.1.4	Tx, Gain droop 2ms time frame, 13dBm o/p		0.2	dB
2.2.1.9	Tx Detector Monitor Settling time	2		µS
2.2.2.6	Rx P-1dB referred to input power	-20		dBm
2.2.2.7	Rx 2 tone Linearity	Pass		dB
2.2.3.1	Switching Speed		5	us
2.2.3.6	TRM Over Temperature Shutdown	Pass		
2.3.1	Dimensions to ICD	Pass		P/F
2.3.3	Mass		80	g

Table 4-6 EFT Tests

4.7 Design Verification Test (DVT)

06_402 Specification para. No.	Parameter	Min	Max	Units
2.2.1.7	Unwanted Emissions (in Tx)	Pass		
2.2.1.8	Interfering IF Input Signals	Pass		
2.2.1.9	Maximum VOUT (MM_TxMB_S), Fault Condition	4		V
2.2.2.2	RF Damage Levels	Pass		dBm
2.2.2.8	Unwanted Emissions (in Rx)	Pass		
2.2.2.9	Interfering RF Input Signals	Pass		
2.2.3.4	Power Supply Damage Levels and Rail Switch on	Pass		

06_402 Specification para. No.	Parameter	Min	Max	Units
	order			
2.4	Environmental Tests	Pass		
2.4.2	Cold Start Up performance	Pass		

Table 4-7 DVT Tests

C/I performance at -20, 0,+20, +40,+60 °C		☑		
IF Conversion Gain Flatness, Tx		☑		
IF Conversion Gain Flatness, Rx		☑		
Port Matches		☑		
Tx, Gain droop 2ms time frame, 13dBm o/p			☑	
Tx Detector Monitor Settling time			☑	
Rx P-1dB referred to input power			☑	
Rx 2 tone Linearity			☑	
Switching Speed			☑	
TRM Over Temperature Shutdown			☑	
Dimensions to ICD			☑	
Mass			☑	
Unwanted Emissions (in Tx)				☑
Interfering IF Input Signals				☑
Maximum VOUT (MM_TxMB_S), Fault Condition				☑
RF Damage Levels				☑
Unwanted Emissions (in Rx)				☑
Interfering RF Input Signals				☑
Power Supply Damage Levels and Rail Switch on order				☑
Environmental Tests				☑
Cold Start Up performance				☑

Table 4-8 Tests and measurements