MESHWORKS™

Radiant Broadband Wireless Access Network

Production Test Specification for IF Processor Board (Bands 1 & 2, 28MHz Channel)

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Draft 0.1	AKA	21/06/01	Draft for comment. LFT only.
Draft 0.2	AKA	17/07/01	Corrections and Logic definition
1.0	AKA/PJR	17/07/01	Including review comments. /new section2.2 added, Section 2.4.3 not complete.
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3.0	AKA/PJR	24/01/02	Updated for TR2d design
4.0	AKA/PJR	24/05/02	Updated for TR3/CR1 design release

Change History

Page No.	Change Detail in This Issue
19	Section 2,4,2 Additional control inputs
31	Band Specific Firmware re-introduced
32-40	Updated Acceptance Criteria in all Tx and Rx Tests (Sections 3.2.3 and 3.2.4)
33-35	Section 3.2.3.2, test extended.
35	Section 3.2.3.4, Band 1 specific test re-introduced
35	Section 3.2.3.5, New test added.
37-39	Section 3.2.4.2, test extended.
39	Section 3.2.4.3, Band 1 specific test re-introduced.
39	Section 3.2.4.5, New test added.
42	Section 3.2.5.1.1 Updated Calibration data structure.
46-48	3.2.5 Calibration memory map changed.

Contents

Figures

Tables

Glossary

ADC	Analogue to Digital Converter
C/I	Carrier to Inter-modulation ratio
DC	Direct Current
EFT	Extended Functional Test
EMC/EMI	Electro-Magnetic Compatibility/ Electro-Magnetic Interference
EEPROM	Electrically Erasable Programmable Read Only Memory
FFT	Full Functional Test
FPGA	Field Programmable Gate Array
ICT	In-Circuit Test
IF	Intermediate Frequency
IFP	Intermediate Frequency Processor
LFT	Limited Functional Test
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
PSU	Power Supply Unit
Rx	Receiver (or receive)
STTE	Special to Type Test Equipment
TBA	To be advised
TBC	To be confirmed
TBD	To Be Determined
TRM	Transmit/Receive Module
TT&C	Telemetry, Tele-command and Control
Tx	Transmitter (or transmit)
MRB	Manufacturing Review Board

References

Refer to latest issues

[1] 05_203, “Radiant Node Phase-1 IF Module Engineering Specification, ETSI Variant for Bands I and II”. (V06 or later)

[2] ETS300 019-1-4: ETSI “EE; Environmental conditions and environmental test for telecommunications equipment; Part 1-4: Classification of environmental conditions stationary use at non-weather protected locations.

[3] RBWAN: Environmental Requirements Specification, 02-206Vxx*

[4] RBWAN: IFP Specification 06-255Vxx*

[5] RBWAN: IFP Production Test Plan PRD_IFSY_IFP_1_PLAN_0.3_17

[6] RBWAN: Specification for Production Data Collection TBD

[7] ITU ‘Series X: Data networks and open systems communications IT – ASN.1 encoding rules, ITU-T X.690.

[8] Philips Semiconductors ‘The I^2C-Bus Specification’, Version 2.1, Jan 2000

[9] RBWAN Board I2C Configuration Format 04_780Vxx*

[10] National Semiconductor, LM83 Triple-diode input and local digital temperature sensor with two wire interface, DS101058.

1 Introduction

This document specifies the production test and calibration of the IF Processor board for bands 1 & 2 with 28MHz channels. This specification is applicable to Trials and Phase 1 equipment for both Band 1 and Band 2 frequencies. All tests are to be carried out in Band 2 configuration. The IF Processor is the analogue link between the millimetric radio (TRM) and Modem in both transmit and receive modes. It provides bi-directional frequency conversion and the analogue element of the AGC in addition to distribution of command and control to the TRM and Synthesiser. A simplified block diagram is shown in Figure 1.1. The acceptance criteria used in this document applies to TR3/CR1 unless otherwise stated.

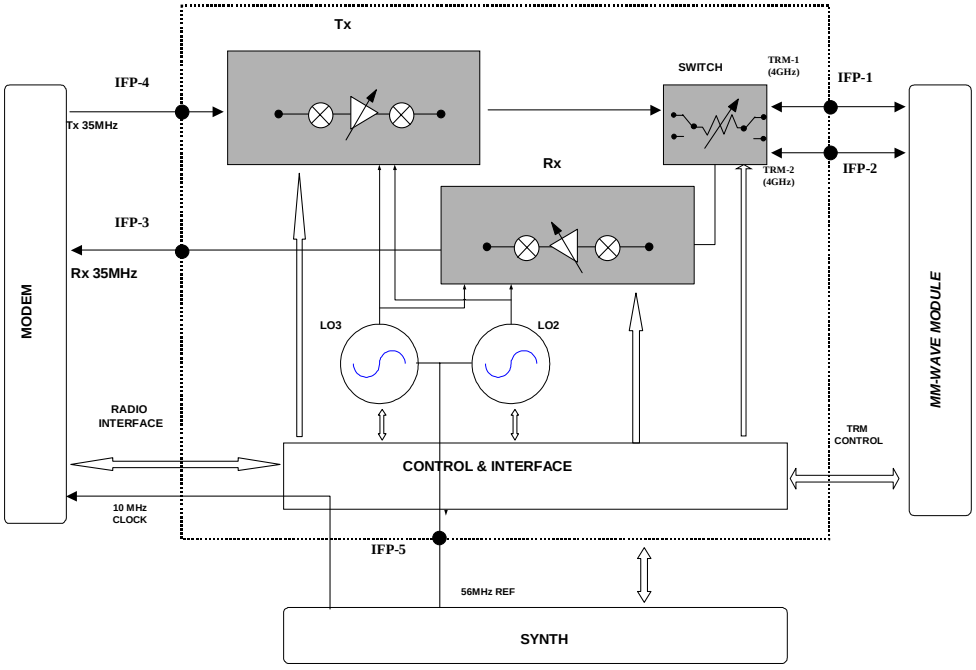


Figure 1-1 ***Block Diagram of IF Processor***

1.1 Objective

The aim is to ensure that tests are clearly specified so that a unified test methodology is applied at all production sites and the production test plan [5] is implemented.

2 Interface, Configuration and Control

2.1 IFP Interface Specification

This section outlines the test and control interfaces.

2.1.1 IFP Connectors

Circuit Ref.	Function	Type
J1	mmW B (4Ghz)	50 Ohm SMA jack
J2	mmW A (4GHz)	50 Ohm SMA jack
J3	Tx I/P from MODEM	50 Ohm MCX Jack
J4	Rx O/P to MODEM	50 Ohm MCX Jack
J5	56 MHz Reference Input	50 Ohm micro-miniature Jack
J6	MODEM Control	Header Pin DIL 50 way 0.05”
J7	DC Power Input	Header Skt DIL 6 way 3mm
J8	Synthesiser Control	Socket Strip DIL 40 way 0.1”
J9	10 MHz Clock To MODEM	50 Ohm MCX Jack
J10	Mm Wave Unit Control	Header Skt DIL 20 way 2.54mm
J11	DC Power to Synth	Socket Pin SIL 5 way 0.2”

Table 2-1 ***IFP Connectors***

2.1.2 J6: Modem Control

This connector passes control signals from the MODEM to the IFP and telemetry in the reverse direction. This is used to configure and control the IFP during tests.

Figure 2-1 ***Component Side View of J6***

Pin	Test Point	Function	Format	Pin	Test Point	Function	Format
1	TP214	IFCFG_XLXPGM_N	LVTTL	26		Ground	DC
2		Ground	DC	27	TP227	IFCTRL_ CLK_SEL	LVTTL
3	TP215	IFCFG_XLXDIN	LVTTL	28		Ground	DC
4		Ground	DC	29	TP228	IFCFG_ CTRL	LVTTL
5	TP216	IFCFG_XLXINIT	LVTTL	30		Ground	DC
6		Ground	DC	31		MODEM_SPARE0	LVTTL
7	TP217	IFCFG_XLXDONE	LVTTL	32		Ground	DC
8		Ground	DC	33		MODEM_SPARE1	LVTTL
9	TP218	IFCFG_RESET	LVTTL	34		Ground	DC
10		Ground	DC	35		MODEM_SPARE2	LVTTL
11	TP219	IFCFG_XLXCLK	LVTTL	36		Ground	DC
12		Ground	DC	37	TP229	NC	LVTTL (not used)
13	TP220	IFCTRL_CLK	LVTTL	38		Ground	DC
14		Ground	DC	39	TP230	NC	(not used)
15	TP221	IFCTRL_ TXFS_N	LVTTL	40		Ground	DC
16		Ground	DC	41	TP231	NC	(not used)
17	TP222	IFCTRL_ TXD	LVTTL	42		Ground	DC
18		Ground	DC	43	TP232	NC	(not used)
19	TP223	IFCTRL_ RXFS_N	LVTTL	44		Ground	DC
20		Ground	DC	45	TP233	SDA	I^2C Serial Bus
21	TP224	IFCTRL_ RXD	LVTTL	46		Ground	DC
22		Ground	DC	47	TP234	SIN	I^2C Interrupt
23	TP225	IFCTRL_ SOTS_N	LVTTL	48		Ground	DC
24		Ground	DC	49	TP235	SCL	I^2C Clock
25	TP226	IFCFG_ RD_XLXINIT_N	LVTTL	50		Ground	DC

Table 2-2 ***MODEM Control Connector J4***

2.1.3 J7: DC Power Input

This is the main DC power input connector for the IFP, power also enters here for onwards transmission to the Synth via J11.

Pin	Function	Format	Test Point	Comment
1	Ground	DC		
2	+13.5V	DC	TP238	Note 1
3	Ground	DC		
4	+6.5V	DC	TP237	
5	Ground	DC		
6	-8.0V	DC	TP236	

Table 2-3 ***Power Input Connector J7***

Note 1: This input is not required to test the IFP it is a direct feed for the Synth via J11.

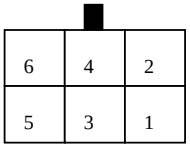


Figure 2-2 ***Component Side View of J7***

2.1.4 J8: Synthesiser Control

This connector passes control signals from the IFP to the Synth and telemetry in the reverse direction.

Pin	Test Point	Function	Format	Pin	Test Point	Function	Format
1	TP239	CHstrobe	LVTTL	21	TP244	Channel3	LVTTL
2		Ground	DC	22	TP256	Channel2	LVTTL
3		Ground	DC	23	TP245	Channel1	LVTTL
4	TP252	RefDacClk	LVTTL	24	TP257	Channel0	LVTTL
5	TP240	RefDacEn	LVTTL	25	TP249	LDSynthRef	LVTTL
6	TP251	IFCFG_XLXDOUT	LVTTL	26		Ground	DC
7	TP241	CALenable	LVTTL	27		Ground	DC
8	TP250	RefDacData	LVTTL	28	TP261	IFCFG_XLXPGM_N	LVTTL
9		Ground	DC	29	TP248	IFCFG_XLXCLK	LVTTL
10		Ground	DC	30	TP260	IFCFG_XLXINIT_N	LVTTL
11		Ground	DC	31	TP247	IFCFG_XLXDONE	LVTTL
12	TP190	Not Connected	DC	32	TP259	IFCFG_ RESET	LVTTL
13	TP189	Not Connected	DC	33		Spare0	LVTTL
14	TP253	10MHz Clock I/P	LVTTL	34		Spare1	LVTTL
15		Ground	DC	35		Spare2	LVTTL
16		Ground	DC	36		Spare3	LVTTL
17	TP242	Channel7	LVTTL	37		CalReq	LVTTL
18	TP254	Channel6	LVTTL	38	TP258	SCL	I^2C Clock
19	TP243	Channel5	LVTTL	39	TP246	SDA	I^2C Serial Bus
20	TP255	Channel4	LVTTL	40	TP191	Not Connected	LVTTL

Table 2-4 ***Synth Control Connector J8***

Figure 2-3 ***Top View of J8***

2.1.5 J10: MM-Wave Module Control

This connector passes control signals from the IFP to the MM-Wave Module (TRM) and telemetry in the reverse direction.

Pin	Test Point	Function	Format
1	TP262	MM_TRSel_N	Differential LVTTL
2	TP274	MM_TRSel_P	Differential LVTTL
3	TP263	MM_APSel_N	Differential LVTTL
4	TP273	MM_APSel_P	Differential LVTTL
5	TP264	MM_PA1En_N	Differential LVTTL
6	TP272	MM_PA1En_P	Differential LVTTL
7	TP265	MM_PA2En_N	Differential LVTTL
8	TP271	MM_PA2En_P	Differential LVTTL
9	TP269	MM_Rx1En_N	Differential LVTTL
10	TP270	MM_Rx1En_P	Differential LVTTL
11	TP268	MM_Rx2En_N	Differential LVTTL
12	TP275	MM_Rx2En_P	Differential LVTTL
13	TP267	SCL	I^2C Clock
14		Ground	DC
15	TP266	SIN	I^2C Interrupt
16	TP276	SDA	I^2C Serial Bus
17		Ground	DC
18	TP277	MM_TxM1_S	Analogue
19		Ground	DC
20	TP278	MM_TxM2_S	Analogue

Table 2-5 ***Millimeter Wave Unit Interface Connector J10***

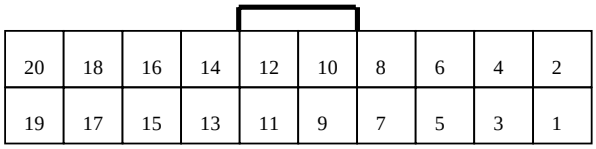


Figure 2-4 ***View of J10 as Seen When PCB is End On***

2.1.6 J11: DC Power to Synth

This connector is an un-buffered daisy chain from J7, it is intended as an output but can be used as an alternative DC power input during test if access is more convenient.

Pin	Function	Format	Test Point	Comment
1	-8.0V	DC	TP281	
2	+6.5V	DC	TP280	
3	Ground	DC		
4	Ground	DC		
5	+13.5V	DC	TP279	

Table 2-6 ***Power Output Connector J11***

Figure 2-5 ***Component Side View of J11***

2.1.7 IFP Electrical Interface

Operation cannot be guaranteed (tests may not be valid) unless the following electrical interfaces are used.

2.1.8 LVTTL I/O

Parameter	Specification
VIH	+2.0V to +3.6V
VIL	0V to +0.8V
VOH	+2.4V to +3.6V
VOL	0V to +0.4V
Output drive capability	12mA

Table 2-7 ***LVTTL I/O Specification***

2.1.9 Differential LVTTL Outputs

Differential outputs are used in pairs, one line is ‘P’ and the other ‘M’. Logic state ‘1’ or High occurs when P>M and ‘0’ or Low occurs when P<M.

Parameter	Specification
V_{OH}	+1.85V to +3.6V
V_{OL}	0V to +1.05V
Output drive capability	30mA

Table 2-8 ***Differential LVTTL Output Specification***

2.1.10 MM_TxMA/B_S Analogue Inputs

These are the inputs to J10 pins 18 and 20.

Parameter	Specification
I/P Voltage Range	0 to +3.3V
Input Impedance	2 kOhm

Table 2-9 ***MM_TxMA/B_S Analogue Input Specification***

2.1.11 I^2C

Parameter	Specification
VIH	+2.1V to +3.6V
VIL	0V to +0.8V
IOH	100µA max
VOL	0V to +0.4V @ 3mA
Clock Frequency	10 to 100kHz
Input Capacitance	20pF max

Table 2-10 ***I^2C I/O Specification***

2.2 Configuring the IFP using External Controller and FPGA Clock

This section describes the recommended procedure for configuring the FPGA. This set-up will use an external EEPROM, the internal clock of the FPGA and an external controller as shown below. It assumes that the controlling device is a PC.

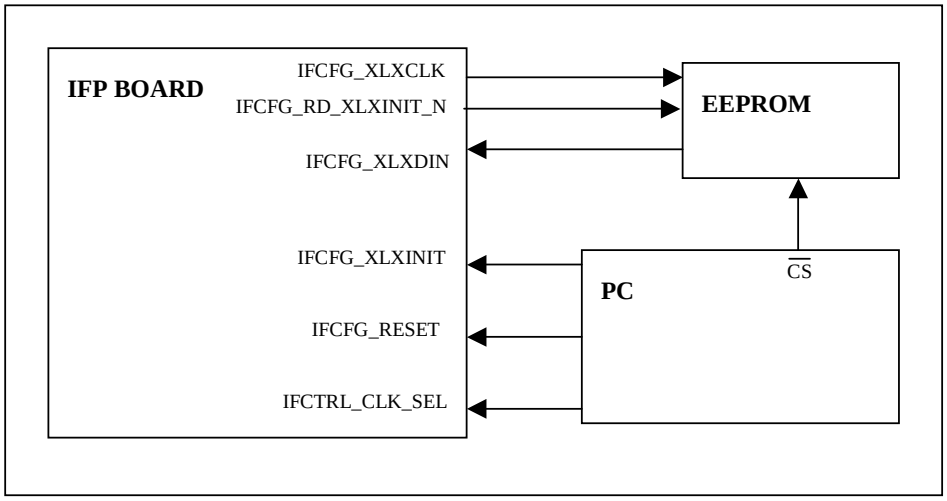


Figure 2-6 ***Configuring IFP using External EEPROM and Controller***

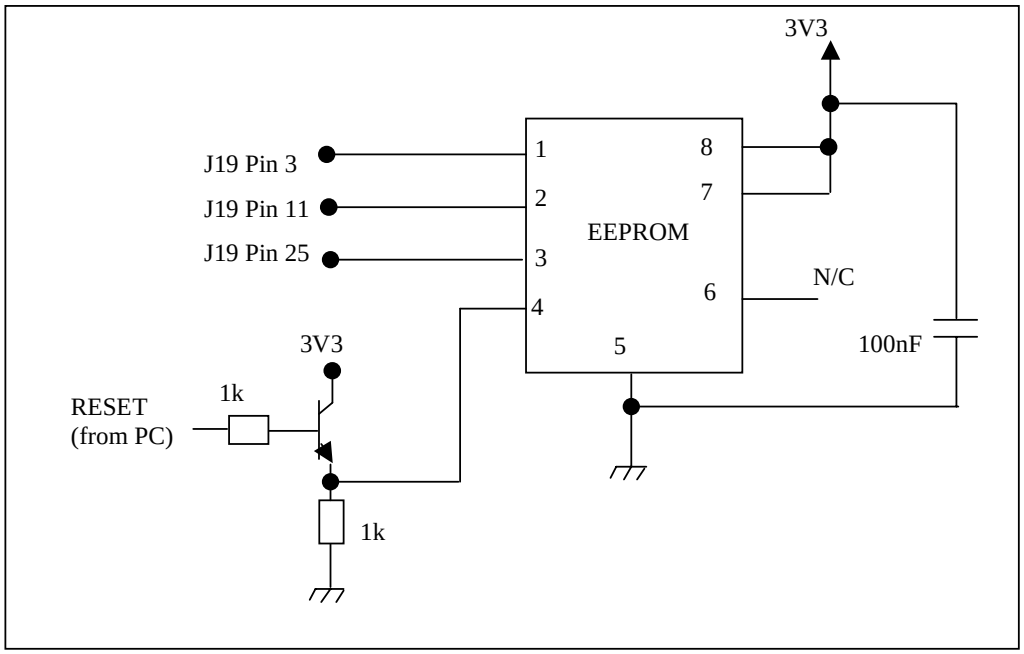


Figure 2-7 ***Recommended Connections to External EEPROM***

In order for the FPGA to configure, the IFCFG_XLXINIT, IFCFG_RESET, IFCTRL_CLK_SEL and /CS lines from the PC should be held low. The power to the IFP board should then be applied, LED1 should illuminate confirming that the FPGA has configured (alternatively, wait for IFCFG_RD_XLXINIT_N to go high), the /CS line should then be set high. Once the IFP has been configured, the IFCTRL_CLK_SEL line should be set high ready for data download.

2.3 Configuring the IFP using External Controller and External Clock

This section deals with an alternative method for configuring the FPGA using an external controlling device, such as a PC. Due to the length of configuration data that is downloaded into the FPGA a sufficiently high clock speed is required (<250kHz), this may be difficult to achieve using a PC.

2.3.1 Setting up the IFP Controller

The bitstream to be downloaded to the FPGA will be a certain length. This length, referred to as the 'length count', is stored in the bitstream. The bitstream consists of the following parts:

1. Eight dummy bits, all High
2. A preamble code of '0010'
3. A 24-bit length count
4. Four dummy bits, all High

The length count could be converted into a decimal number, for example

11111111**0010**00000011101001101111100**1111…**

The bit stream above would have a length count of 239353 bits. This length count determines the number of clock pulses that are required to download the configuration data.

2.3.2 Saving the Configuration Data

A suitable format may be required in which to save the configuration data so that any new versions of configuration data can be transferred over the Internet and used by our supplier.

2.3.3 Configuring the FPGA

The configuration of the FPGA consists of four steps. The following sections explain how to configure the FPGA.

2.3.3.1 Clearing Configuration Memory

The first step in the configuration process is clearing the configuration memory.

On power-up, once the supply voltage reaches the Power-On-Reset threshold the device automatically begins clearing configuration memory.

If it is necessary to clear configuration memory after power-up then it is possible to do this by the IFCFG_XLXPGM_N line. While IFCFG_XLXPGM_N is low the FPGA will continuously cycle through the clearing process when IFCFG_XLXPGM_N goes high one last clearing pass takes place. Do not hold IFCFG_XLXPGM_N low for more than 500µS, as this line should not be used to delay the configuration process. Should a delay be required the IFCFG_XLXINIT line should be held low.

The line IFCFG_RD_XLXINIT_N going high will confirm the end of the clearing configuration process.

2.3.3.2 Initialization

Now that IFCFG_RD_XLXINIT_N has gone high confirming that the memory is clear the FPGA will sample the state of IFCFG_CTRL. This line should be set high.

IFCFG_CTRL selects the serial slave mode of operation for configuring the FPGA.

Note that holding IFCFG_XLXINIT low can be used to delay the configuration step.

2.3.3.3 Configuration

After IFCFG_RD_XLXINIT_N has gone high, it is necessary for the controller to wait for a period between 55µS and 275µS before driving the IFCFG_XLXCLK input that transfers the bit stream into the FPGA.

IFCFG_XLXDIN is the input line for configuration data. The IFCFG_XLXDIN line is read on the rising edge of the clock (IFCFG_XLXCLK).

The IFCFG_XLXDONE line will go high indicating that the configuration data has been successfully downloaded. Three conditions must be met in order for IFCFG_XLXDONE to go high.

1. The length of the configuration data must match the length given at the beginning of the bit stream.
2. No bit errors detected.
3. All of the configuration data has been loaded into configuration memory.

2.3.3.4 Start-Up

Once IFCFG_XLXDONE has gone high, sufficient clock pulses must be provided on the IFCFG_XLXCLK line, TBD.

The FPGA O/P lines LDC (Low during configuration) and HDC (high during configuration) provide status on the device's progress. The status of the LDC line can be observed by LED1, indicating that the configuration process is complete.

2.4 IFP FPGA Message Structure

The FPGA on the IFP board will receive various message types during test. The data within these messages may also vary significantly depending upon the required set-up during test. This section defines messages (Data streams) that are used for data communications with the IFP.

IFP messages sent either to/from the IFP FPGA are as follows.

1 Timeslot Data

2 Delay Data

3 IFP Calibration Data

4 IFP Synthesiser Recalibration

5 General Status Message (output of FPGA)

Note that all messages are sent/received MSB first.

2.4.1 Timeslot Data Definitions

The IFP has a serial interface that is used for controlling all functions of the IFP, TRM and synthesiser. This is a 66-bit message defined in the table below. Bits that are not defined are to be set to '0'.

Field Name	*Field Size*	*Bit number*	*Previous identity*
Identifier = "0000"	*4*	*65 down to 62*	
SHARED_ATTENUATION	*5*	*61 down to 57*	*TXRXGAIN*
TX_ATTENUATION	*3*	*56 down to 54*	*TXGAIN*
Not Allocated	*1*	*53*	*LO calibration en*
TX_ENABLE	*1*	*52*	*TXEN*
TRM_SELECT	*1*	*51*	*MMMODULESEL*
TRM_ANTENNA_SELECT	*1*	*50*	*MM ANTENNA SEL*
Not Allocated	*1*	*49*	*RXGAIN[4]*
RX_ATTENUATION	*3([3:1])*	*48 down to 46*	*RXGAIN*
Not Allocated	*1*	*45*	*RXGAIN[0]*
RX_ENABLE	*1*	*44*	*RXEN*
REF_10M_VCO_DAC_WORD	*16*	*43 down to 28*	*REFDAC*
CHANNEL_NUMBER	*8*	*27 down to 20*	*CHANNEL*
CHANNEL_CAL_REQUEST	*1*	*19*	*CAL_ENABLE*
Not Allocated	*2*	*18 down to 17*	*TXPDOWN[1:0]*
Not Allocated	*1*	*16*	*RXPDOWN[1]*
LED2	*1*	*15*	*RXPDOWN[0]*
TRM_PA_DISABLE_DELAY	*15*	*14 down to 0*	*MM PA DISABLE DELAY*

Table 2-11 ***Time-Slot Data Definitions***

2.4.1.1 Message Identifier (bits 65 down to 62)

The FPGA will receive different message types. The message identify informs the FPGA which type of data it is about to process. The timeslot data as detailed in this section is 0_{16}.

2.4.1.2 SHARED_ATTENUATION (bits 61 down to 57)

This is a 5-bit register that controls the 4GHz attenuator **(U8)**. This attenuator is common in both transmit and receive paths.

	Bit				
Timeslot Bits	**61**	**60**	**59**	**58**	**57**
Min. Attenuation	1	1	1	1	1
Max. Attenuation	0	0	0	0	0
Usage	Tx/Rx	Tx/Rx	Tx/Rx	Tx/Rx	Tx/Rx
Freq	4GHz				
Att state (dB's)	1	2	4	8	16

Table 2-12 ***SHARED_ATTENUATION***

2.4.1.3 TX_ATTENUATION (bits 56 down to 54)

This is a 3-bit register that controls the 500MHz attenuator **(U12)** in transmit.

	Bits		
Timeslot Bits	**56**	**55**	**54**
Min. Attenuation	**1**	**1**	**1**
Max. Attenuation	**0**	**0**	**0**
Usage	**Tx**	**Tx**	**Tx**
Freq	**500MHz**		
Att state (dB's)	**16**	**8**	**4**

Table 2-13 ***TX_ATTENUATION***

2.4.1.4 TX_ENABLE (bit 52)

Transmit Enable. Set high to enable the transmit strip. NB the TX and Rx strips are controlled independently, TxEn has no effect on the Rx performance.

2.4.1.5 TRM_SELECT (bit 51)

The IFP has two 4GHz ports that each connect to a TRM, the module select bit selects the appropriate TRM.

	TRM Port 1	TRM Port 2
TRM_SELECT	0	1

Table 2-14 ***TRM_SELECT***

2.4.1.6 TRM_ANTENNA_SEL (bit 50)

Each TRM is connected to two antennas this bit selects the appropriate antenna

	Antenna 1	Antenna 2
TRM_ANTENNA_SELECT	**0**	**1**

Table 2-15 ***TRM_ANTENNA_SELECT***

2.4.1.7 RX_ATTENUATION(bits 48 down to 46))

This is a 5-bit register that controls the 500MHz **(U2)** attenuator in receive mode. Note that bits 20 and 16 are not implemented and should be set to 0.

	Bit		
Timeslot Bits	**48**	**47**	**46**
Min. Attenuation	1	1	1
Max. Attenuation	0	0	0
Usage	Rx	Rx	Rx
Freq	500MHz		
Att state (dB's)	16	8	4

Table 2-16 ***RX_ATTENUATION***

2.4.1.8 RX_ENABLE (bit 44)

Receive Enable. Set high to enable the receive strip. Transmit strip should be disabled.

2.4.1.9 REF_10M_VCO_DAC_WORD (bits 43 down to 28)

This is used to calibrate the synthesiser 10MHz reference. Default setting is $7FFF_{16}$

2.4.1.10 CHANNEL_NUMBER (bits 27 down to 20)

Channel number setting of the synthesiser, 00_{16} sets channel 0, and 43_{16} will set channel 67 (top of the band). The table below shows how channels are set.

Setting channel to FF_{16} or $7F_{16}$ is reserved for Ref. Synth. Calibration.

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Timeslot Bits	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**
Binary	1	1	0	0	0	0	1	0
Hex	**C**				**2**			

Table 2-17 ***CHANNEL_NUMBER***

2.4.1.11 CHANNEL_CAL_REQUEST (bit 19)

Used to calibrate a channel by the error value written to the feed forward DAC. When set, the channel that is selected should be calibrated.

2.4.1.12 LED2 (bit 15)

Setting high will illuminate LED2, this is useful for confirming that the FPGA has processed timeslot data, and is somewhat functional. Default setting is low.

2.4.1.13 TRM_PA_DISABLE_DELAY (bits 14 down to 0)

This delay determines the time duration that the PA in the TRM (Tx section) will be enabled, since the IFP will be transmitting data of varying lengths, this delay is part of the timeslot data rather than the delay data.

2.4.2 Delay Data Definitions

The delay data consists of 166 bits of data and is downloaded into the IFP FPGA via the same serial interface used for downloading timeslot data. The delay counter at each FPGA digital output is started by setting IFCTRL_SOTS_N low for one clock duration. The clock is kept running continuously at a known speed and the appropriate FPGA output will be enabled when the delay counter (incremented by every positive edge of IFCTRL_CLK) has elapsed. Two clock ticks are required to clock this digital bit to the output port.

Field Name	Field Size	Bit number	Previous identity
Identifier = "0001"	*4*	*165 down to 162*	
TX_ATTENUATION_DELAY	*9*	*161 down to 153*	*TXGAINDELAY*
Not Allocated	*9*	*152 down to 144*	*LODELAY[8:0]*
TX_ENABLE_DELAY	*9*	*143 down to 135*	*TXENDELAY*
IF_MODE_DELAY	*9*	*134 down to 126*	*TXRXDELAY*
TRM_SELECT_DELAY	*9*	*125 down to 117*	*MMMODULEDELAY*
Not Allocated	*9*	*116 down to 108*	*TXRXGAINDELAY[8:0]*
RX_ATTENUATION_DELAY	*9*	*107 down to 99*	*RXGAINDELAY*
RX_ENABLE_DELAY	*9*	*98 down to 90*	*RXENDELAY*
REF_10M_VCO_UPDATE_DELAY	*9*	*89 down to 81*	*REFDACDELAY[8:0]*
CHANNEL_INFO_DELAY	*9*	*80 down to 72*	*CHANNELDELAY*
TRM_MODE_DELAY	*9*	*71 down to 63*	*MMTRSELDELAY*
TRM_RX_ENABLE_DELAY	*9*	*62 down to 54*	*MM_RXENABLEDELAY*
TRM_PA_ENABLE_DELAY	*9*	*53 down to 45*	*MM_PA_DELAY*
Not Allocated	*9*	*44 down to 36*	*TXPDOWN0DELAY[8:0]*
Not Allocated	*9*	*35 down to 27*	*TXPDOWN1DELAY[8:0]*
LED2_DELAY	*9*	*26 down to 18*	*RXPDOWN0DELAY[8:0]*
Not Allocated	*9*	*17 down to 9*	*RXPDOWN1DELAY[8:0]*
TRM_PA_SAMPLE_DELAY	*9*	*8 down to 0*	*PADETDELAY*

The logic responsible for handling these delays is integrated into the FPGA logic. Delays shall not be tested in manufacturing. All delay fields are to be set to zero except TRM_PA_DISABLE_DELAY that is set in the timeslot data.

2.4.3 IFP Calibration Data Message

Containing information ***specific*** to an IFP build. This 15-bit message is used to calibrate out non-linearity's of the IFP board.

Field Name	Field Size	Bit number	Previous identity
Identifier = "0010"	*4*	*19 down to 16*	
Rx_MONOTONIC_OFFSET	*3*	*15 down to 13*	
Rx_CORRECTION_STEP	*2*	*12 down to 11*	
Tx_MONOTONIC_OFFSET	*3*	*10 down to 8*	
Tx_CORRECTION_STEP	*2*	*7 down to 6*	
RX_OFFSET	*3([3:1])*	*5 down to 3*	
TX_OFFSET	*3([3:1])*	*2 down to 0*	

2.4.3.1 Rx_MONOTONIC_OFFSET (bits 15 down to 13)

Offset is set in Tx and is used to compensate for the kink in the 4GHz attenuator that may be present between attenuator states 23 and 24.

2.4.3.2 Rx_CORRECTION_STEP (bits 12 down to 11)

Offset is set in Tx and is used to compensate for the kink in the 4GHz attenuator that may be present between attenuator states 15 and 16.

2.4.3.3 Tx_MONOTONIC_OFFSET (bits 10down to 8)

Offset is set in Tx and is used to compensate for the kink in the 4GHz attenuator that may be present between attenuator states 23 and 24.

2.4.3.4 Tx_CORRECTION_STEP (bits 7 down to 6)

Offset is set in Tx and is used to compensate for the kink in the 4GHz attenuator that may be present between attenuator states 15 and 16.

2.4.3.5 RX_OFFSET (bits 5 down to 3)

Offset set in Rx is used to set the gain of the receive section.

2.4.3.6 TX_OFFSET (bits 2 down to 0)

Offset set in Tx is used to set the gain of the transmit section.

2.4.4 IFP Synthesiser Reprogramming

The two IFP synthesisers are calibrated at power-up with a 56MHz ref. Once calibrated, they should remain locked. This message may be used for debugging purposes only and not used to attempt to lock a faulty synth. during testing.

Field Name	Field Size	Bit number	Previous identity
Identifier = "0011"	*4*	*3 down to 0*	

2.4.5 General Status Message

This is a 24-bit output message from the IFP FPGA that is read at power up, or any time during debugging. This message is used to determine the lock status of the synths and to read the output of the ADC.

Field Name	Field Size	Bit number	Previous identity
Identifier = "0000"	*4*	*23 down to 20*	
Synth PLL Cal. Required	*19*	*19*	*Reference synth cal required*
Synth PLL Locked	*18*	*18*	*Reference synth locked*
IFP LO3 Locked	*17*	*17*	*Tertiary/LO3 synth locked*
IFP LO2 Locked	*16*	*16*	*Secondary/LO2 synth locked*
PA Detect data	*8*	*15 down to 8*	
FPGA firmware version	*8*	*7 down to 0*	

2.4.5.1 SYNTH PLL CAL REQUIRED (bit 19)

Ref. Synth. cal required bit. Default value is '0' when no ref. synth fitted. Controlled by pin 37 of J8. Cal. required = '1'.

2.4.5.2 SYNTH PLL LOCKED (bit 18)

Lock status of ref. synth. This bit will default to a logic '1' when no Ref. synth. fitted. Controlled by pin 25 of J8. Locked = '1'.

2.4.5.3 IFP LO3 LOCKED (bit 17)

Tertiary synthesiser lock status. Locked = '1'.

2.4.5.4 IFP LO2 LOCKED (bit 16)

Secondary synthesiser lock status. Locked = '1'.

2.4.5.5 PA DETECT DATA (bits 15 down to 8)

This is an 8-bit analogue to digital converter function operating over the range 0 to +3.3V. An analogue d.c. voltage is applied to either pins 18 or 20 of J10. This voltage is applied to the ADC (U31). When timeslot data is downloaded into the FPGA followed by an assertion of IFCTRL_SOTS_N, the FPGA will instruct the ADC to perform a conversion, at this point the digital value will be transferred from the ADC to the FPGA. The value is stored in a FPGA register until either overwritten or powered down.

The conversion from binary to applied input voltage is as follows.

1. Binary value '0011 1010' = 58_{10}
2. 3.3/256*58 = 0.75 Volts.

2.4.5.6 FPGA FIRMWARE VERSION (bits 7 down to 0)

The firmware version should be read to determine that the communications from the IFP FPGA to the PC is working correctly. Value read depends on firmware version.

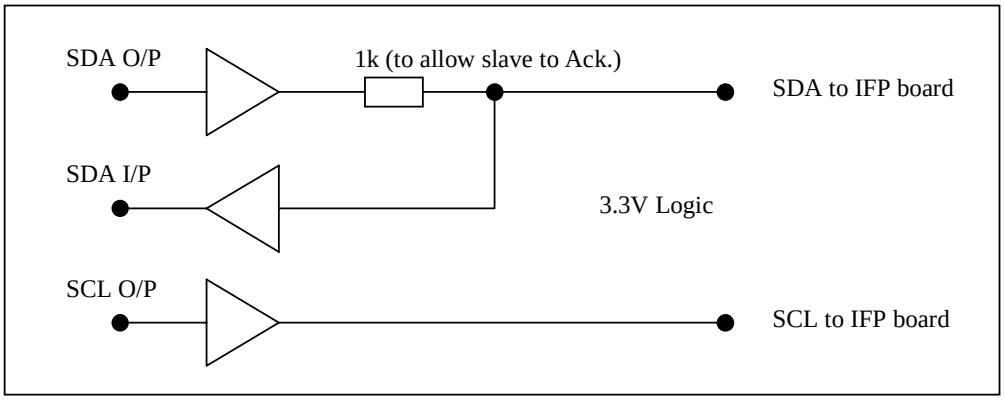
2.5 I^2C Programming Protocol

The IFP also has an I^2C bus that is totally independent of the FPGA. This is used for storing/recalling manufacturing and calibration data and for reading the board temperature. The I^2C bus may be located on the following connectors.

Connector	SDA	SCL
J6	45	49
J8	39	38
J10	18	7

Note that all messages are sent/received MSB first.

In order to write build status information, or read the temperature of the IFP board, I^2C protocol is used. The I^2C bus is a 2-wire interface (SCA and SDA) that is used to read and write to I^2C compatible devices on the IFP board. Typically, for test purposes a PC I/O card will be used for I^2C communications. When using an I/O card it may be necessary to use a 3-wire interface as it is necessary to read and write data. In this case the following connections should be made so that the IFP is able to pull the SDA line low during an acknowledge. For debugging, it is also useful to check that the SDA line is not shorted high or low by the IFP board by reading the logic level of the line back into the I/O card this may also be done with the clock line (SCL).



The I^2C controller (i.e. the PC) will be referred to as the master and the IFP as the slave.

Low voltage logic (3.3V) is used when writing to any device on the I^2C bus.

The SCL line must be kept running when saving build status information, for example additional clock pulses are required after the stop condition to clock data into appropriate memory locations when writing to the EEPROM.

2.5.1 Start Condition

An I^2C start condition is always used before writing to any I^2C compatible device. The SDA and SCL lines should be initially set high and should remain high when the I^2C bus is not in use.

A start condition is a High to Low transition of SDA when SCL is High.

2.5.2 Stop Condition

The stop condition is used at the end of all I^2C communications or to stop the bus under a No Ack condition.

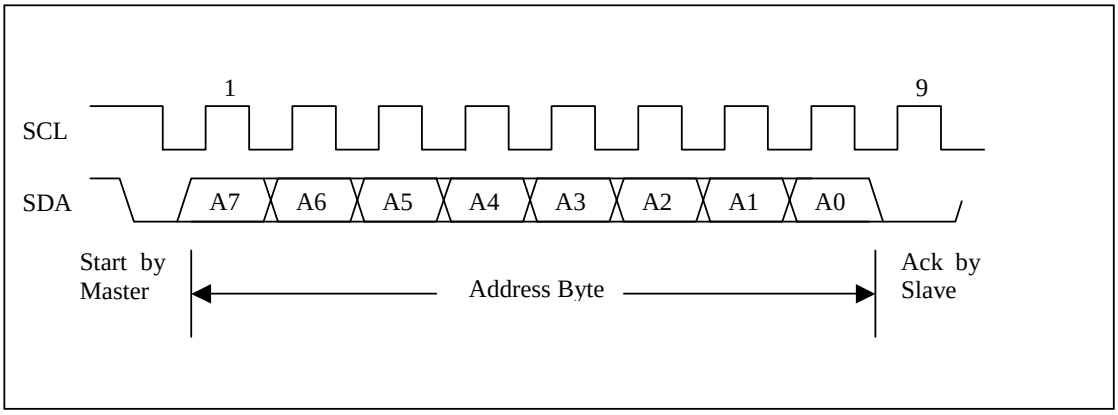
A stop condition is a Low to High transition of SDA when SCL is High.

2.5.3 Slave Address

The slave address is the 8-bit address of a device that is being written to and follows an I^2C start condition. The I^2C device that matches the slave address will pull the SDA line Low with an acknowledge signal and await further data transmissions.

2.5.4 Acknowledge

The Acknowledge (Ack) bit is pulled Low by the receiver (master or slave) for one clock duration to indicate that the data has been successfully received. When the slave does not receive an Ack by the master the slave will stop transmitting whether it has completed downloading the data or not in this case, the master should initiate a stop condition. No acknowledge (No Ack) typically indicates a fault condition the exception to this rule applies when the master has just received the last byte of data and is about to initiate a stop condition (No point to Ack the slave once the master has what it wants!).



2.5.5 Reading/Writing Data

All I^2C data communications to/from the IFP are 8 bits long (1 byte), MSB (most significant bit) first, a low Ack follows bytes transmitted by the receiver unless a stop condition is followed by the master.

2.5.6 Writing Calibration Data

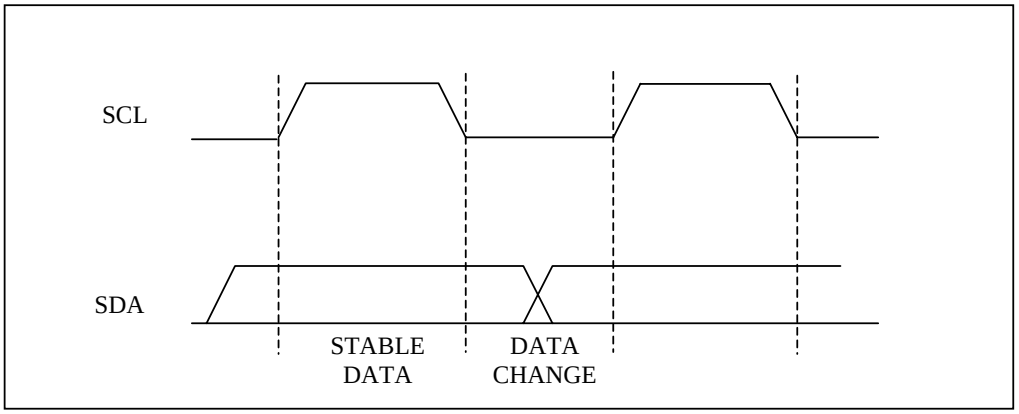
IIC protocol used for storing build status information and calibration data comply to the encoding specification 'Basic Encoding Rules'. Calibration data is stored LSB (least significant byte) first. The value 285_{10} (an attenuator setting of 28.5dB's * 10) in hex equates to $11D_{16}$, and is thus saved as:

memory location *n*: 0x1D

memory location *n+1:* 0x01.

2.5.7 Data Validity

Data states on the SDA line may only change while SCL is low, changing the SDA state while SCL is high is reserved for start and stop conditions.



2.6 Controlling the IFP

This section explains how to read to and write from the IFP boards FPGA and I^2C interface.

Information contained in this section regarding the I2C interface relates to section 'I^2C Programming Protocol'.

2.6.1 Parallel Lines used to Control the IFP

The following table shows lines that are used to transfer data to and from the IFP board. Following sections will show how these lines are used to transfer useable data.

Cct Desg. (where different)	FPGA Pin No.	Function	Logic	J6 Pin No.
IFCTRL_CLK	2	Free running clock at 1/16 of IFIF_CLOCK/16	Clock, '0' - internal clk	13
IFCTRL_TXFS_N	3	Frame Synch (Modem to FPGA)	Low during data transfer	15
IFCTRL_TXD	4	Transmit data (Modem to FPGA)	Data (read on +ve edge of clk)	17
IFCTRL_RXFS_N	5	Frame Synch	Low during data transfer	19
IFCTRL_RXD	10	Receive data (FPGA to Modem)	Data (read on +ve edge of clk)	21
IFCTRL_SOTS_N	9	Start of timeslot	Pulse low to init. delay, hold high until finished	23
IFCTRL_CLK_SEL	117	Select internal or external clock (CTRL CLK only)	'1' external clock	27
SDA		Temp Sensor. Build Status		45
SIN		Critical Temperature Alarm		47
SCL		Temp Sensor. Build Status		49
IFCTRL_CLK	2	Free running clock at 1/16 of IFIF_CLOCK/16	Clock, '0' - internal clk	13
IFCTRL_TXFS_N	3	Frame Synch (Modem to FPGA)	Low during data transfer	15

Table 2-18 ***Parallel Control Lines***

2.6.2 Writing Serial Data to the FPGA

Serial data is sent to the FPGA in the following format.

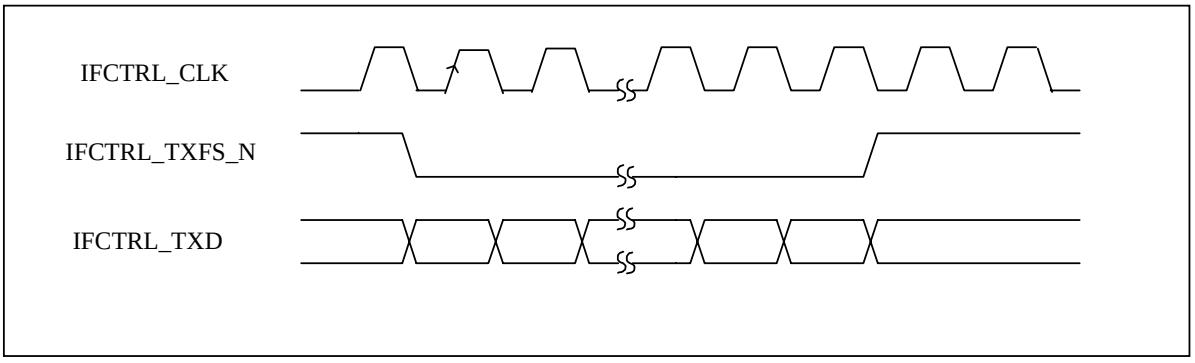


Figure 2-7 ***Serial Data Write Format***

2.6.3 Start of Timeslots

The FPGA on the IFP is essentially a double-buffered serial to parallel shift register. Once the timeslot data is downloaded into the FPGA through the serial link, it is necessary to pulse IFCTRL_SOTS_N ('_N' denotes

active low) low for one clock cycle in order to push the parallel data out of the FPGA. The timing diagram below indicates how to use IFCTRL_SOTS_N. Any changes made to the timeslot data will not take effect until the 'Start of Timeslots' is pulsed low.

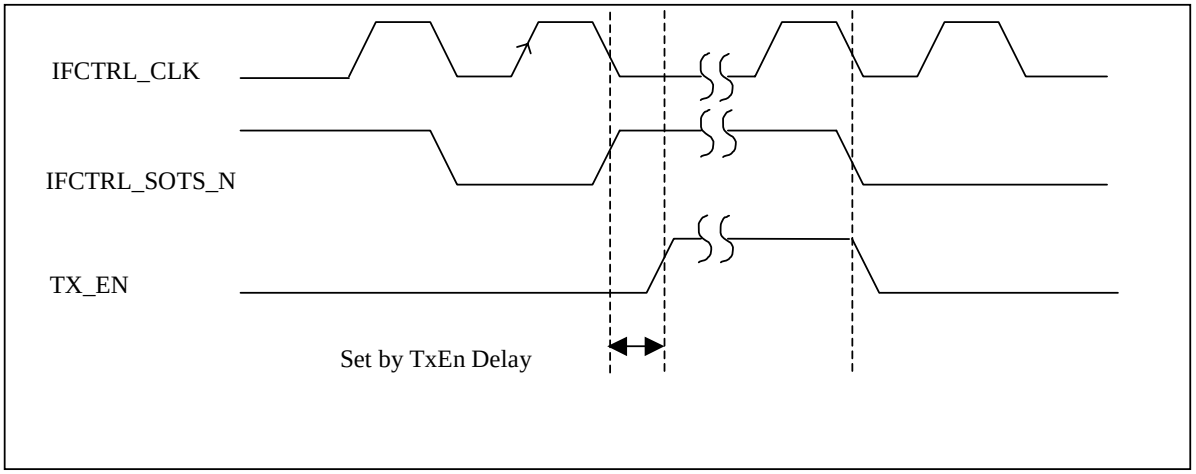


Figure 2-8 ***Start of Time-slots***

After sending timeslot data, the outputs from the FPGA will remain until IFCTRL_SOTS_N is set low and sufficient clock ticks provided for internal FPGA processing of data.

2.6.4 Reading Serial Data (General Status Message) from the FPGA

The diagram below shows the lines and logic required to read data from the FPGA.

Note that the FPGA requires one clock pulse after IFCTRL_RXFS_N has been set low, the data from the FPGA will follow on the second clock pulse, this can be observed in the diagram below.

The FPGA will output 24 bits of data.

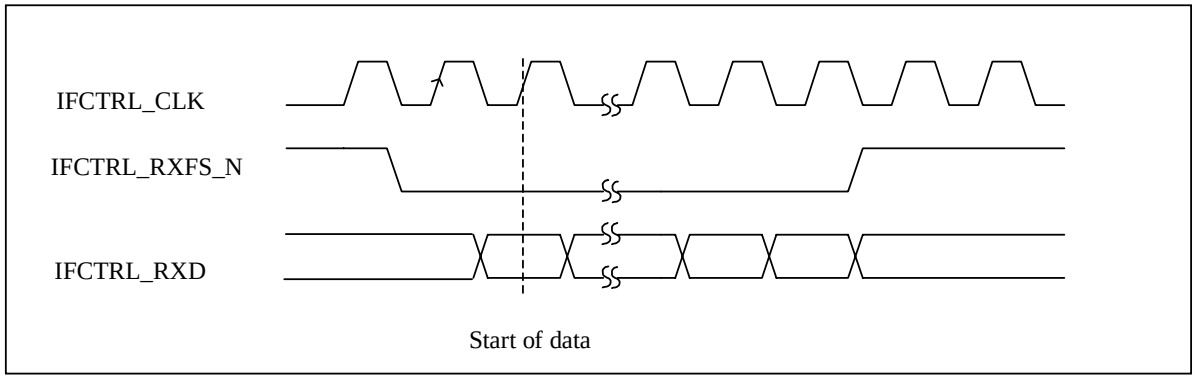


Figure 2-9 ***Serial Data Read Format***

2.6.5 Reading Board Temperature

The temperature sensor **(U28)** is an LM83 [10], the only function used is reading temperature from the local sensor (command 00_{16}).

I^2C Address of temperature sensor is '0101 001x'. 'x' – read/write bit.

Reading the IFP temperature is carried out as follows.

1. Generate a Start Condition on the I2C bus.
2. Send slave address hex 52. LM83 will Ack by pulling SDA Low.
3. Send command byte hex 00. LM83 will Ack.
4. Generate a Stop Condition.
5. Generate a Start Condition.
6. Send slave address hex. 53. LM83 will Ack.
7. Read LM83 local temperature data byte.
8. Generate a Stop Condition.

The following table shows temperature (degrees centigrade to hex) conversion.

Binary Value	Hex.	Decimal Value	Temperature (°C)
0000 0000	0x00	0	0
0000 1000	0x08	8	8
0010 0011	0x23	35	35
0100 0100	0x44	68	68

The received byte directly equates to the temperature in degrees centigrade.

2.6.6 Saving Build Status Information

The following steps are required to save build status information. All unused memory locations are to be set to zero.

1. Generate a Start Condition on the I^2C bus.
2. Send slave address hex AC. M24C02 will Ack by pulling SDA Low.
3. Send memory location byte starting at hex 00. M24C02 will Ack.
4. Send data byte (build status information). M24C02 will Ack.
5. Generate a Stop Condition.
6. Provide the M24C02 with 150 clock cycles on the SCL line to allow M24C02 to clock data into the desired memory location.
7. Increment memory location counter. Return to step 1.

EEPROM Parameter	EEPROM Specification
Write Control (TP280)	Write Protect = open or V_{IH} Write Enable = V_{IL}
EEPROM Size	256 Octets

Table 2-19 ***EEPROM Specification***

2.6.7 Recalling Build Status Information

It is necessary to be able to recall the build status information to check that the data has been downloaded correctly. To read the M24C02 device, follow the steps listed below. All unused memory locations should read zero.

1. Generate a Start Condition on the I^2C bus.
2. Send slave address hex AC. M24C02 will Ack by pulling SDA Low.
3. Send memory location byte starting at hex 00. M24C02 will Ack.
4. Generate a Start Condition on the I^2C bus.
5. Send slave address hex AD. M24C02 will Ack by pulling SDA Low.
6. Read data byte.
7. Generate a Stop Condition.

3 Test Specification

3.1 Test Firmware

The IFP has no none-volatile memory hence it will need to download firmware from the test system at PCB power up. The latest version of the firmware described in Table 2-1 will be used for all tests.

Band	Firmware
1	390030.xx
2	390010.xx

Table 3-1 ***Test Firmware***

Where xx = Version

This firmware will automatically configure the IFP for the frequency band. The version of the test firmware will be controlled by the production build instructions.

3.2 Limited Functional Test

These tests shall be performed on all units as part of the production process.

Specifications in this section are to verify correct production using the most economic test equipment and minimum time.

The recommended test flow is shown in Figure 3.1.

Tests should be carried out using the following nominal supply voltages

Nominal I/P Voltage	Maximum I/P Voltage	Minimum I/P Voltage
+6.50V	+7.15V	+5.85V
-8.00V	-7.20V	-8.80V

Table 3-2 ***Nominal Supply Voltages for LFT***

There is nothing within the IFP to stop both Tx and Rx enables occurring concurrently, although this will not cause any damage Tx and Rx enables should be mutually exclusive during all tests.

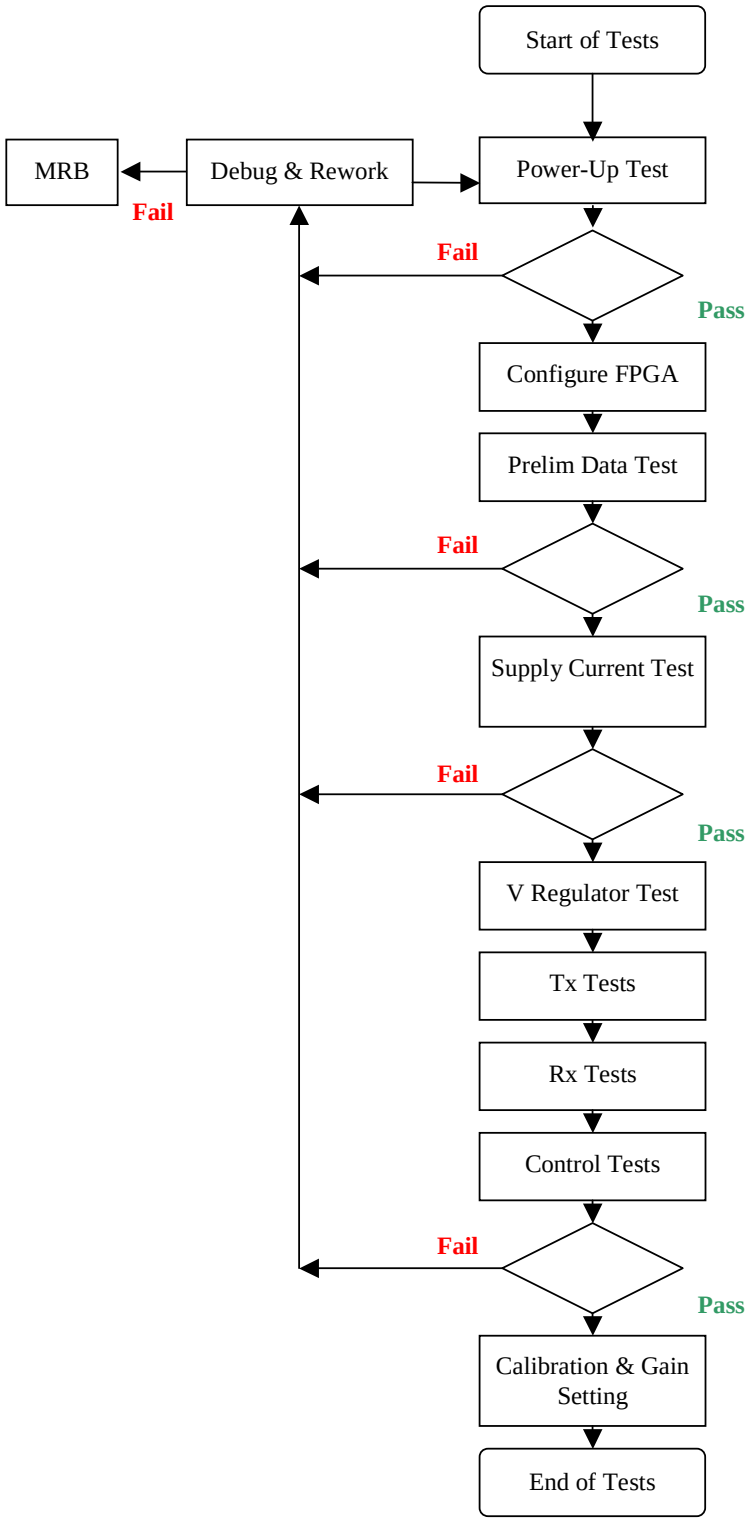


Figure 3-1 ***LFT Flow Chart***

3.2.1 Preliminary DC Tests

3.2.1.1 Pre-Power Up Test

Test Condition	Acceptance Criteria
I/P Connection	**Minimum Resistance to Gnd**
J7 Pin 4	4 Ohm
J7 Pin 6	4 Ohm

Table 3-3 ***Input Voltage Supplies***

WARNING
Do not proceed with other tests if unit fails at this stage!

3.2.1.2 Supply Current Test

NB This test requires the FPGA to be configured.

Supply currents for both Tx and Rx states should be measured in the maximum gain setting.

Test Condition		Acceptance Criteria	
State	**Nominal I/P**	**Maximum Current**	**Minimum Current**
Tx	+6.50V	0.720A	0.580A
Rx	+6.50V	0.770A	0.630A
Tx	-8.00V	0.030A	0.010A
Rx	-8.00V	0.030A	0.010A

Table 3-4 ***Input Supply Currents***

WARNING
Do not proceed with other tests if any current exceeds the maximum load by more than 10%!

3.2.1.3 Voltage Regulation Test

NB This test requires the FPGA to be configured.

Test Condition		Acceptance Criteria	
Test Point	**Nominal Voltage**	**Maximum Voltage**	**Minimum Voltage**
TP200	+5.0V	+5.25V	+4.75V
TP201	+5.0V	+5.25V	+4.75V
TP202	+5.0V	+5.25V	+4.75V
TP207	+5.0V	+5.25V	+4.75V
TP208	+5.0V	+5.25V	+4.75V
TP209	+5.0V	+5.25V	+4.75V
TP211	+5.0V	+5.25V	+4.75V
TP212	-5.0V	-4.75V	-5.25V
TP213	+3.3V	+3.40V	+3.20V

Table 3-5 ***Voltage Regulator Outputs***

3.2.2 Preliminary Tests

These tests should be carried out in the following order and before other tests are performed.

NB: These tests requires the FPGA to be configured.

3.2.2.1 'General Status Message' Feedback

Check FPGA is configured confirming J6 pin 7 is high, or by TP145 = LOW or LED1 (D2) = ON.

The FPGA feedback 'General Status Message' should be read to confirm the following status.

Test Condition		Acceptance Criteria	
Function	**Bit Number**	**Bit-stream data**	**Alternative Check**
IFP LO2 LOCKED flag	16	1	TP177 = High
IFP LO3 LOCKED flag	17	1	TP210 = High
FPGA FIRMWARE VERSION	7 down to 0	Note 1	

Table 3-6 ***Preliminary Data Check***

Note 1: Firmware version should that defined in the build instructions accompanying the order, this used to check data integrity and functionality of FPGA. The version data read during test should be recorded in the results.

WARNING
Do not proceed with other tests if unit fails at this stage!

3.2.2.2 LO Tuning Voltage

The LO2 and LO3 oscillator tuning voltages are to be checked to the following specification. Tuning voltage is to be recorded.

Oscillator	Test Point	Min. Volts	Max. Volts
LO2	TP176	0.7	3.8
LO3	TP149	0.7	3.8

Table 3-7

WARNING
Do not proceed with other tests if unit fails at this stage!

3.2.3 Transmit Tests

NB: All transmit tests require the FPGA to be configured.

All Transmit tests will be carried out at a single input frequency of 35 MHz output frequency will be 4070.5 MHz except for Tx Channel Slope. TxEn Should be 1 and RxEn 0.
A typical test equipment set up is shown in Figure 3.2.

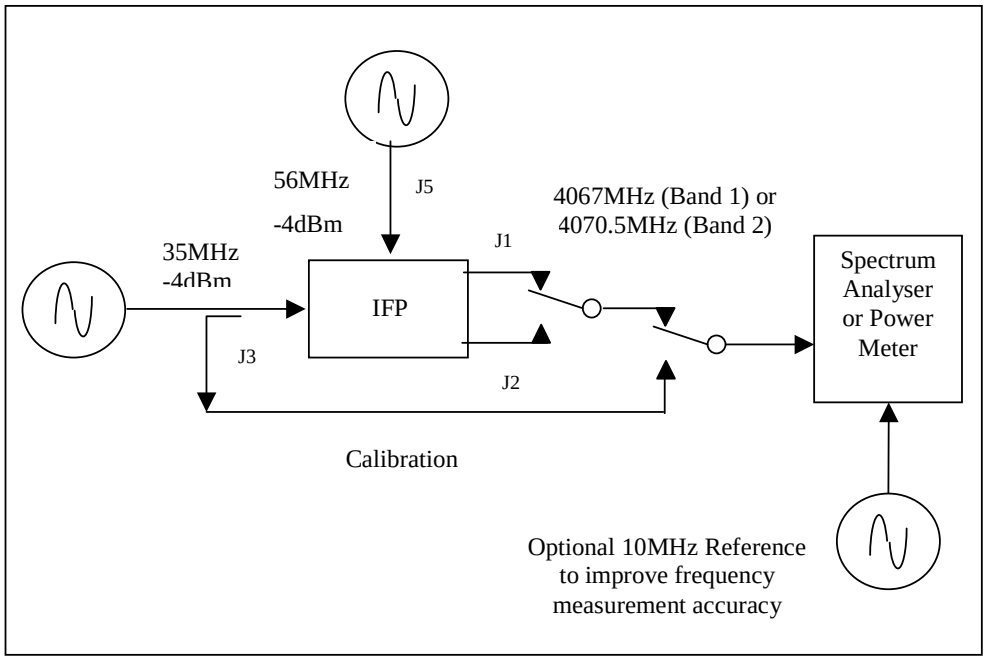


Figure 3-2 ***Transmit Test Set Up***

3.2.3.1 Setting and Testing Maximum Tx Conversion Gain (TG_{max})

The conversion gain specification may vary between release types. Tests shall be carried out using J1 (TRM_modulesel = 1) as the output port. TG_{max} occurs when TxRxGain = 11111 and TxGain = 111. It will be necessary to set the gain to the level shown in Table 3.8. This will be achieved by adjusting the Tx Offset control word until gain is in the acceptance window, this value will be used for all subsequent Tx tests and will be recorded with the calibration data.

Release	Min Acceptable TG_{max} (dB)	Max Acceptable TG_{max} (dB)
TR3/CR1	-4	-2

Table 3-8 ***Tx Gain Setting***

Gain setting should be performed within 4 minutes of switching on units from cold (cold = not powered up within last 30 min), warm units (those powered up for longer than 4 minutes) should be left to cool for 30 minutes before setting gain.

3.2.3.2 Full Tx Gain Control Staircase

Tests shall be carried out using J1 (TRM_modulesel = 1) as the output port. Input power at TG_{max} should be the same as used in section 3.2.3.1, input power should be kept constant for all attenuator states. Table 3-9 shows the test conditions and Tables3-10 and 3-11 show the acceptance criteria for Attenuators A and B respectively.

Attenuator A (4GHz) has two bad steps that require compensation before any further tests or calibration measurements are carried out. " Tx Correction step (TCS)" is set by measuring TA_{16} and increasing the correction step value until TA_{15}-TA_{16} is within the range shown in Table 3-10. This correction step value must be used for all subsequent tests. The "Tx Monotonic Offset (TMO)" is set by measuring TA_{23} and TA_{24} then increasing the TMO value until TA_{23}-TA_{24} is within the range shown in Table 3-10, TCS should be set to 0 while setting TMO. This monotonic offset value must be used for all subsequent Tx tests.

State	Attn A	Attn B	TxRxGain	TxGain	Comment
TG_{max}	0	0	11111	111	
TA_{01}	1	0	11110	111	
TA_{02}	2	0	11101	111	
TA_{03}	3	0	11100	111	
TA_{04}	4	0	11011	111	
TA_{05}	5	0	11010	111	
TA_{06}	6	0	11001	111	
TA_{07}	7	0	11000	111	
TA_{08}	8	0	10111	111	
TA_{09}	9	0	10110	111	
TA_{10}	10	0	10101	111	
TA_{11}	11	0	10100	111	
TA_{12}	12	0	10011	111	
TA_{13}	13	0	10010	111	
TA_{14}	14	0	10001	111	
TA_{15}	15	0	10000	111	
TA_{16}	16	0	01111	111	**Set Tx Correction Step**
TA_{17}	17	0	01110	111	
TA_{18}	18	0	01101	111	
TA_{19}	19	0	0100	111	
TA_{20}	20	0	01011	111	
TA_{21}	21	0	01010	111	
TA_{22}	22	0	01001	111	
TA_{23}	23	0	01000	111	
TA_{24}	24	0	00111	111	**Set Tx monotonic offset**
TA_{25}	25	0	00110	111	
TA_{26}	26	0	00101	111	
TA_{27}	27	0	00100	111	
TA_{28}	28	0	00011	111	
TA_{29}	29	0	00010	111	
TA_{30}	30	0	00001	111	
TA_{31}	31	0	00000	111	
TB_{01}	0	4	11111	110	
TB_{02}	0	8	11111	101	
TB_{03}	0	12	11111	100	
TB_{04}	0	16	11111	011	
TB_{05}	0	20	11111	010	
TB_{06}	0	24	11111	001	
TB_{07}	0	28	11111	000	

Table 3-9 ***Tx Conversion Gain Stair-Case Test Conditions***

	Acceptance Criteria	Acceptance Criteria
Math	**Min Attenuation dB**	**Max Attenuation dB**
TGmax - TA01	0.2	1.8
TA01 - TA02	0.2	1.8
TA02 - TA03	0.2	1.8
TA03 - TA04	0.2	1.8
TA04 - TA05	0.2	1.8
TA05 - TA06	0.2	1.8
TA06 - TA07	0.2	1.8
TA07 - TA08	0.2	1.8
TA08 - TA09	0.2	1.8
TA09 - TA10	0.2	1.8
TA10 - TA11	0.2	1.8
TA11 - TA12	0.2	1.8
TA12 - TA13	0.2	1.8
TA13 - TA14	0.2	1.8
TA15 - TA16	0.2	1.8
TA16 - TA17	0.2	1.8
TA17 - TA18	0.2	1.8
TA18 - TA19	0.2	1.8
TA19 - TA20	0.2	1.8
TA20 - TA21	0.2	1.8
TA21 - TA22	0 (*Note 1*)	1.8
TA22 - TA23	0 (*Note 1*)	1.8
TA23 - TA24	0 (*Note 1*)	1.8
TA24 - TA25	0 (*Note 1*)	1.8
TA251 - TA26	0 (*Note 1*)	1.8
TA26 - TA27	0 (*Note 1*)	1.8
TA27 - TA28	0 (*Note 1*)	1.8
TA28 - TA29	0 (*Note 1*)	1.8
TA29 - TA30	0 (*Note 1*)	1.8
TA30 - TA31	0 (*Note 1*)	1.8
TGmax - TAmin (note 2)	23	35

Table 3-10 ***Attenuator A Acceptance Criteria***

Note 1: Across the range covered by note 1 there is a maximum allowance of 1 non-monotonic step of up to –1.0dB.

Note 2: TAmin *= Attenuator State that provides minimum gain measurement, this will probably be in the range* TA21 to TA27.

	Acceptance Criteria	Acceptance Criteria
	Min Attenuation dB	Max Attenuation dB
TGmax - TB01	3.2	4.8
TB01 - TB02	3.2	4.8
TB02 - TB03	3.2	4.8
TB03 - TB04	3.2	4.8
TB04 - TB05	3.2	4.8
TB05 - TB06	3.2	4.8
TB06 - TB07	3.2	4.8
TGmax - TB07	27.0	29.0

Table 3-11 ***Attenuator B Acceptance Criteria***

The data should also be recorded as gain relative to TG_{max} (eg TB_{nn}-TG_{max}), this data will be required for calibration.

Additional Acceptance Criteria

Radiant will provide additional test code (Software Part Number TBD), this will check the attenuator calibration data will be acceptable to the Node Controller. The measured data must successfully pass through this checking code without errors.

3.2.3.3 Tx Conversion Frequency Accuracy

The conversion frequency provided by the local oscillators will be tested in the receive test, this does not need to be repeated in transmit.

3.2.3.4 Tx Spurious Outputs

Tests shall be carried out using J1 (TRM_modulesel = 1) as the output port using the same test set up as Tx gain control staircase (3.2.3.3) the output spurious described in Table 3.12 should be measured and compared to the wanted output signal measured in section 3.2.3.3. The in-band spurious test is best performed with no input signal applied. Spurious test should be carried out at gain setting $TA_{13.}$

Test Condition			Acceptance Criteria
Spurious	**Band 1 O/P freq (MHz)**	**Band 2 O/P freq (MHz)**	**Output Spurious level**
LO2-IF	3108	3111.5	<-40dBm
LO2	3587.5	3591.0	<-40dBm
LO3+LO2-35MHz	3997	4000.5	<-50dBc
LO3+LO2	4032	4035.5	<-50dBc
In-band	4068	4070.5	<-50dBc

Table 3-12 ***Tx Spurious Outputs***

NB: The first two acceptance criteria are dBm and the others are dBc!

3.2.3.5 Tx Channel Slope

Tests shall be carried out using J1 (TRM_modulesel = 1) as the input port. Using TG_{max} and the

frequencies specified in table 3-13, measure the three gain values across the channel and ensure the result complies with table 3-14.

Band	F1		F2		F3	
	Output	**Input**	**Output**	**Input**	**Output**	**Input**
1	4055.5MHz	23.5MHz	4067MHz	35MHz	4078.5MHz	46.5MHz
2	4059MHz	23.5MHz	4070.5MHz	35MHz	4082MHz	46.5MHz

Table 3-13 Tx Channel Slope Test Conditions

Math	Acceptance Criteria
Gain at F1 minus Gain at F2	< +/-3dB
Gain at F2 minus Gain at F3	< +/-3dB
Gain at F1 minus Gain at F3	< +/-3dB

Table 3-14 Tx Channel Slope Acceptance Criteria

3.2.4 Receive Tests

NB: All receive tests require the FPGA to be configured.

All receive tests will be carried out at a single input frequency of 4068.75 MHz output frequency will be 36.75 MHz for Band 1 and 33.25 MHz for Band 2. All tests except Rx frequency conversion accuracy and Rx Channel Slope should be carried out in Band-2 only. TxEn Should be 0 and RxEn 1.

A typical test equipment set up is shown in Figure 3.3.

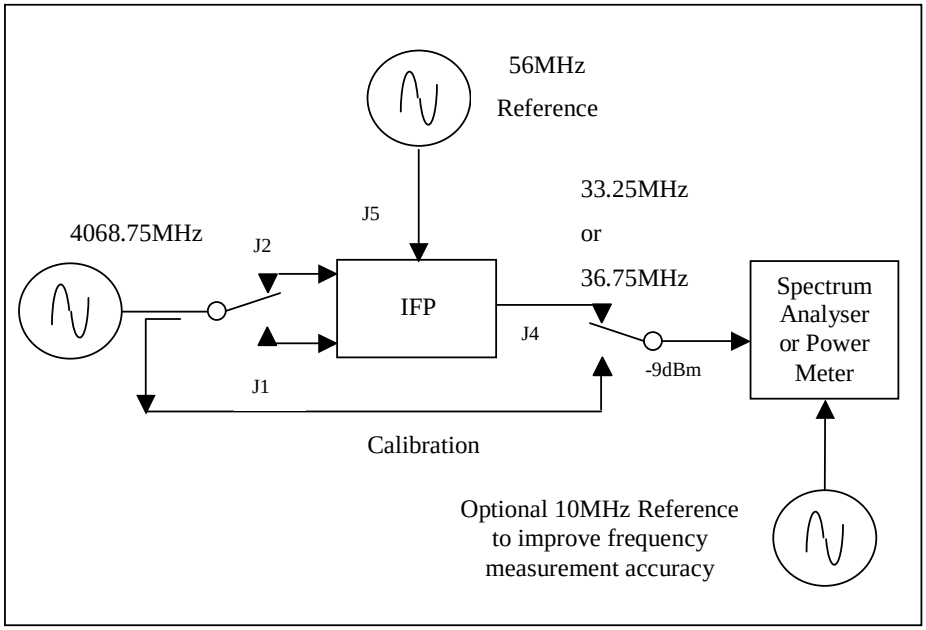


Figure 3-3 ***Receive Test Set-up***

3.2.4.1 Setting and Testing Maximum Rx Conversion Gain (RG_{max})

The conversion gain specification will vary between release types. Tests shall be carried out using Band-2 frequencies and J2 (TRM_modulesel = 0) as the input port. RG_{max} occurs when TxRxGain = 11111 and RxGain = 111. It will be necessary to set the gain to the level shown in Table 3.15. This will be achieved by adjusting the Rx Offset (RO) control word until gain is in the acceptance window, this value will be used for all subsequent Rx tests and will be recorded with the calibration data.

Release	Min Acceptable RG_{max} (dB)	Max Acceptable RG_{max} (dB)
TR3/CR1	+61.5	+63.5

Table 3-15 ***Setting Rx Conversion Gain***

This will be achieved by adjusting the Rx Offset control word until gain is in the range shown in Table 3-8, this value will be used for all subsequent Rx tests and will be recorded with the calibration data.

Gain setting should be performed within 4 minutes of switching on units from cold (cold = ambient room temperature), warm units (those powered up for longer than 4 minutes) should be left to cool for 30 minutes before setting gain.

3.2.4.2 Full Rx Gain Control Staircase

Tests shall be carried out using Band-2 frequencies and J2 (TRM_modulesel = 0) as the input port. Input power at RG_{max} should be the same as used in section 3.2.4.1. At system level, as the attenuators are increased the input power would also be increased to maintain a constant output power. This is the preferred condition for the IFP measurement however using a constant input power is also permissible. See Tables 3.16, 3-17 and 3-18 for details.

Attenuator A (4GHz) has two bad steps that require compensation before any further tests or calibration measurements are carried out. " Rx Correction step (RCS)" is set by measuring RA_{16} and RA_{16} and increasing the correction step value until RA_{15}-RA_{16} is within the range shown in Table 3-17. This correction step value must be used for all subsequent Rx tests. The "Rx Monotonic Offset (RMO)" is set by measuring RA_{23} and RA_{24} then increasing the RMO value until RA_{23}-RA_{24} is within the range shown in Table 3-17, RCS should be set to 0 while setting RMO. This monotonic offset value must be used for all subsequent Rx tests.

Test Condition				
State	**Attn A**	**Attn B**	**TxRxGain**	**RxGain**
RGmax	0	0	11111	111
RA01	1	0	11110	111
RA02	2	0	11101	111
RA03	3	0	11100	111
RA04	4	0	11011	111
RA05	5	0	11010	111
RA06	6	0	11001	111
RA07	7	0	11000	111
RA08	8	0	10111	111
RA09	9	0	10110	111
RA10	10	0	10101	111
RA11	11	0	10100	111
RA12	12	0	10011	111
RA13	13	0	10010	111
RA14	14	0	10001	111
RA15	15	0	10000	111
RA16	16	0	01111	111
RA17	17	0	01110	111
RA18	18	0	01101	111
RA19	19	0	0100	111
RA20	20	0	01011	111
RA21	21	0	01010	111
RA22	22	0	01001	111
RA23	23	0	01000	111
RA24	24	0	00111	111
RA25	25	0	00110	111
RA26	26	0	00101	111
RA27	27	0	00100	111
RA28	28	0	00011	111
RA29	29	0	00010	111
RA30	30	0	00001	111
RA31	31	0	00000	111
RB01	0	4	11111	110
RB02	0	8	11111	101
RB03	0	12	11111	100

RB04	0	16	11111	011
RB05	0	20	11111	010
RB06	0	24	11111	001
RB07	0	28	11111	000

Table 3-16 ***Rx Conversion Gain Stair-Case Test Conditions***

	Acceptance Criteria	**Acceptance Criteria**	
Math	**Min Attenuation dB**	**Max Attenuation dB**	**Comment**
RGmax - RA01	0.2	1.8	
RA01 - RA02	0.2	1.8	
RA02 - RA03	0.2	1.8	
RA03 - RA04	0.2	1.8	
RA04 - RA05	0.2	1.8	
RA05 - RA06	0.2	1.8	
RA06 - RA07	0.2	1.8	
RA07 - RA08	0.2	1.8	
RA081 - RA09	0.2	1.8	
RA09 - RA10	0.2	1.8	
RA10 - RA11	0.2	1.8	
RA11 - RA12	0.2	1.8	
RA12 - RA13	0.2	1.8	
RA13 - RA14	0.2	1.8	
RA15 - RA16	0.2	1.8	Set RCS
RA16 - RA17	0.2	1.8	
RA17 - RA18	0.2	1.8	
RA18 - RA19	0.2	1.8	
RA19 - RA20	0.2	1.8	
RA20 - RA21	0.2	1.8	
RA21 - RA22	0 (*Note 1*)	1.8	
RA22 - RA23	0 (*Note 1*)	1.8	
RA23 - RA24	0 (*Note 1*)	1.8	Set RMO
RA24 - RA25	0 (*Note 1*)	1.8	
RA251 - RA26	0 (*Note 1*)	1.8	
RA26 - RA27	0 (*Note 1*)	1.8	
RA27 - RA28	0 (*Note 1*)	1.8	
RA28 - RA29	0 (*Note 1*)	1.8	
RA29 - RA30	0 (*Note 1*)	1.8	
RA30 - RA31	0 (*Note 1*)	1.8	
RGmax - RAmin	22	35	

Table 3-17 ***Attenuator A Acceptance Criteria***

Note 1: Across the range covered by note 1 there is a maximum allowance of 1 non-monotonic step up to –1.0dB.

Note 2: RAmin *= Attenuator State that provides minimum gain measurement, this will probably be in the range* RA21 to RA27.

	Acceptance Criteria	Acceptance Criteria
Math	Min Attenuation dB	Max Attenuation dB
RGmax - RB01	3.2	4.8
RB01 - RB02	3.2	4.8
RB02 - RB03	3.2	4.8
RB03 - RB04	3.2	4.8
RB04 - RB05	3.2	4.8
RB05 - RB06	3.2	4.8
RB06 - RB07	3.2	4.8
RGmax - RB07	27.0	29.0

Table 3-18 ***Attenuator B Acceptance Criteria***

The data should be recorded as gain relative to RG_{max} (eg RA_{nn}-RG_{max}), this data will be required for calibration.

Additional Acceptance Criteria

Radiant will provide additional test code (Software Part Number TBD), this will check the attenuator calibration data will be acceptable to the Node Controller. The measured data must successfully pass through this checking code without errors.

3.2.4.3 Rx Conversion Frequency Accuracy

This test may be carried out at the same time as the maximum gain conversion in section 3.2.4.1, the same test conditions should be used.

Test Condition		Acceptance Criteria
Band	Measurement Accuracy (MHz)	Output frequency (MHz)
1	+/- 0.001	36.75 +/- 0.01
2	+/- 0.001	33.25 +/- 0.01

Table 3-19 ***Rx Conversion Frequency Accuracy***

It should be possible to calibrate out the effects of the two external frequency sources so it is unnecessary to specify their accuracy.

3.2.4.4 Rx Spurious Outputs

Tests shall be carried out using band-2 and J2 (TRM_modulesel = 0) as the input port. Using the same test set up as Rx gain control staircase (3.2.4.3) the LO generated output spurious described in Table 3.20 should be measured and compared to the wanted output signal measured in section 3.2.4.3. The test is best performed with no input signal applied.

Test Condition		Acceptance Criteria
Gain Setting	Output frequency (MHz)	Output Spurious level
RGmax	35.00	<-20dBm

Table 3-20 ***Rx Spurious***

3.2.4.5 Rx Channel Slope

Tests shall be carried out using J2 (TRM_modulesel = 0) as the input port. Using RG_{max} and the frequencies specified in table 3-21, measure the three gain values across the channel and ensure the result complies with table 3-22.

Band	F1		F2		F3	
	Input	**Output**	**Input**	**Output**	**Input**	**Output**
1	4055.5MHz	23.5MHz	4067MHz	35MHz	4078.5MHz	46.5MHz
2	4059MHz	23.5MHz	4070.5MHz	35MHz	4082MHz	46.5MHz

Table 3-21 Rx Channel Slope Test Conditions

Math	Acceptance Criteria
Gain at F1 minus Gain at F2	< +/-3dB
Gain at F2 minus Gain at F3	< +/-3dB
Gain at F1 minus Gain at F3	< +/-3dB

Table 3-22 Rx Channel Slope Acceptance Criteria

3.2.5 Calibration and Build Status EEPROM

The calibration and build status EEPROM should be loaded with a single bit-stream consisting the contents of the right hand column of table 3.23, reading from top to bottom and left to right using 'Basic Encoding Rules' (BER). All unused memory locations (octets) should be set to 00_{16}.

Information			EEPROM Data
Octet String Type	**Application Name**	**Number of Octets**	**Hex code for octets**
Application tag	IFPConfiguration	1	77
Length		1	80
Primitive Application Tag	PartNumber	1	40
Length of data		1	06
Part number		6	**37, 37, 30, 36, 30, 30 (Note1)**
Primitive Application Tag	IssueNumber	1	41
Length of data		1	02
Issue number		2	**20, 44 (Note 2)**
Primitive Application Tag	ModificationState	1	42
Length of data		1	02
Modification state		2	**20, 31 (Note 3)**
Primitive Application Tag	SerialNumber	1	43
Length of data		1	06
Serial number		6	**30, 30, 30, 30, 30, 31 (Note4)**
Primitive Application Tag	DateCode	1	44
Length of data		1	06
Date code		6	**30, 35, 30, 36, 30, 31 (Note 5)**
Primitive Application Tag	SiteCode	1	45
Length of data		1	01
Site code		1	**42 (Note 6)**
Primitive Application Tag	IfProcCalibrationData	1	49
Length of data		2	81, A6
Calibration Version		4	03, 00, 00, 00
Calibration data		162	**See Table 3-23**
End of contents marker		1	00
End of contents length		1	00

Table 3-23 ***Calibration and Build Status EEPROM Memory Map***

Note 1: Hex coded ASCII of 770600 (ie each decimal bit is converted into ASCII and then encoded into binary as if it was Hex.)

Note 2: Hex coded ASCII. Issue number will be as per bar-code label (' D' – Space followed by 'D').

Note 3: Hex coded ASCII. Modification state will be as per bar-code label (' 1' – Space followed by '1').

Note 4: Hex coded ASCII. Serial number will be as per bar-code label (000001).

Note 5: Hex coded ASCII. Date code will be DDMMYY (5 June 2002)

Note 6: Hex coded ASCII. Site code will be as per bar-code label (B).

Bar Code Label Example:

770600-D-1-B Ser no. 000001, where 770600 = part number, D = issue, 1 = modification, B = site code.

'Specification for Production Data Collection' [6] fully defines the bar-code label.

3.2.5.1.1 Calibration Data

Each calibration state will be encoded in the order shown in Table 3-22. Calibration states 1 to 80 use two octets each, relative attenuation will be stored as a positive number, zero is maximum gain and increasing number is reducing gain. The measured value will be multiplied by ten (10) and rounded to the nearest integer so the stored data resolution is a tenth of a decibel (0.10dB). Example: 30.44dB = $01,30_{16}$. Note that calibration data is stored LSB (least significant byte) first, refer to section 'Writing Calibration Data'. Calibration states 81 and 82 use one octet each.

	MSB							**LSB**
FO	X	X	Rx Offset3	Rx Offset2	Rx Offset1	Tx Offset3	Tx Offset2	Tx Offset1
TAO	X	X	X	TX_Mon2	TX_Mon1	Tx_Mon0	Tx_Step1	Tx_Step0
RAO	X	X	X	Rx_Mon2	Rx_Mon1	Rx_Mon0	Rx_Step1	Rx_Step0

Table 3-24 ***Calibration States 81 and 82***

Where Tx_Mon2, Tx_Mon1, Tx_Mon0 is the MSB to LSB of the "Tx_Monotonic Offset" word and Tx_Step1, Tx_Step0 are the MSB and LSB of the "Tx_Step Offset" word and Rx_Mon2, Rx_Mon1, Rx_Mon0 is the MSB to LSB of the "Rx_Monotonic Offset" word and Rx_Step1, Rx_Step0 are the MSB and LSB of the "Rx_Step Offset" word, all defined during the Tx Gain Control Staircase tests in section 3.2.3.3. Rx Offset3, Rx Offset2 Rx Offset1 is the MSB to LSB of the "Rx Offset" word defined during the Rx Gain Setting Test in section 3.2.4.2. Tx Offset3, Tx Offset2 Tx Offset1 is the MSB to LSB of the "Tx Offset" word defined during the Tx Gain Setting Test in section 3.2.3.2.

Cal State	Name	Description	No. Bytes	Cal State	Name	Description	No. Bytes
1	RG_{MAX}	Rx 4GHz 0dB	2	42	TG_{MAX}-TA_{01}	Tx 4GHz -1dB	2
2	RG_{MAX}-RA_{01}	Rx 4GHz -1dB	2	43	TG_{MAX}-TA_{02}	Tx 4GHz -2dB	2
3	RG_{MAX}-RA_{02}	Rx 4GHz -2dB	2	44	TG_{MAX}-TA_{03}	Tx 4GHz -3dB	2
4	RG_{MAX}-RA_{03}	Rx 4GHz -3dB	2	45	TG_{MAX}-TA_{04}	Tx 4GHz -4dB	2
5	RG_{MAX}-RA_{04}	Rx 4GHz -4dB	2	46	TG_{MAX}-TA_{05}	Tx 4GHz -]5dB	2
6	RG_{MAX}-RA_{05}	Rx 4GHz -5dB	2	47	TG_{MAX}-TA_{06}	Tx 4GHz -6dB	2
7	RG_{MAX}-RA_{06}	Rx 4GHz -6dB	2	48	TG_{MAX}-TA_{07}	Tx 4GHz -7dB	2
8	RG_{MAX}-RA_{07}	Rx 4GHz -7dB	2	49	TG_{MAX}-TA_{08}	Tx 4GHz -8dB	2
9	RG_{MAX}-RA_{08}	Rx 4GHz -8dB	2	50	TG_{MAX}-TA_{09}	Tx 4GHz -9dB	2
10	RG_{MAX}-RA_{09}	Rx 4GHz -9dB	2	51	TG_{MAX}-TA_{10}	Tx 4GHz -10dB	2
11	RG_{MAX}-RA_{10}	Rx 4GHz -10dB	2	52	TG_{MAX}-TA_{11}	Tx 4GHz -11dB	2
12	RG_{MAX}-RA_{11}	Rx 4GHz -11dB	2	53	TG_{MAX}-TA_{12}	Tx 4GHz -12dB	2
13	RG_{MAX}-RA_{12}	Rx 4GHz -12dB	2	54	TG_{MAX}-TA_{13}	Tx 4GHz -13dB	2
14	RG_{MAX}-RA_{13}	Rx 4GHz -13dB	2	55	TG_{MAX}-TA_{14}	Tx 4GHz -14dB	2
15	RG_{MAX}-RA_{14}	Rx 4GHz -14dB	2	56	TG_{MAX}-TA_{15}	Tx 4GHz -15dB	2
16	RG_{MAX}-RA_{15}	Rx 4GHz -15dB	2	57	TG_{MAX}-TA_{16}	Tx 4GHz -16dB	2
17	RG_{MAX}-RA_{16}	Rx 4GHz -16dB	2	58	TG_{MAX}-TA_{17}	Tx 4GHz -17dB	2
18	RG_{MAX}-RA_{17}	Rx 4GHz -17dB	2	59	TG_{MAX}-TA_{18}	Tx 4GHz -18dB	2
19	RG_{MAX}-RA_{18}	Rx 4GHz -18dB	2	60	TG_{MAX}-TA_{19}	Tx 4GHz -19dB	2
20	RG_{MAX}-RA_{19}	Rx 4GHz -19dB	2	61	TG_{MAX}-TA_{20}	Tx 4GHz -20dB	2
21	RG_{MAX}-RA_{20}	Rx 4GHz -20dB	2	62	TG_{MAX}-TA_{21}	Tx 4GHz -21dB	2
22	RG_{MAX}-RA_{21}	Rx 4GHz -21dB	2	63	TG_{MAX}-TA_{22}	Tx 4GHz -22dB	2
23	RG_{MAX}-RA_{22}	Rx 4GHz -22dB	2	64	TG_{MAX}-TA_{23}	Tx 4GHz -23dB	2
24	RG_{MAX}-RA_{23}	Rx 4GHz -23dB	2	65	TG_{MAX}-TA_{24}	Tx 4GHz -24dB	2
25	RG_{MAX}-RA_{24}	Rx 4GHz -24dB	2	66	TG_{MAX}-TA_{25}	Tx 4GHz -25dB	2
26	RG_{MAX}-RA_{25}	Rx 4GHz -25dB	2	67	TG_{MAX}-TA_{26}	Tx 4GHz -26dB	2
27	RG_{MAX}-RA_{26}	Rx 4GHz -26dB	2	68	TG_{MAX}-TA_{27}	Tx 4GHz -27dB	2
28	RG_{MAX}-RA_{27}	Rx 4GHz -27dB	2	69	TG_{MAX}-TA_{28}	Tx 4GHz -28dB	2
29	RG_{MAX}-RA_{28}	Rx 4GHz -28dB	2	70	TG_{MAX}-TA_{29}	Tx 4GHz -29dB	2
30	RG_{MAX}-RA_{29}	Rx 4GHz -29dB	2	71	TG_{MAX}-TA_{30}	Tx 4GHz -30dB	2
31	RG_{MAX}-RA_{30}	Rx 4GHz -30dB	2	72	TG_{MAX}-TA_{31}	Tx 4GHz -31dB	2
32	RG_{MAX}-RA_{31}	Rx 4GHz -31dB	2	73	TG_{MAX}-TB_{00}	Tx 0.5GHz 0dB	2
33	RG_{MAX}-RB_{00}	Rx 0.5GHz 0dB	2	74	TG_{MAX}-TB_{01}	Tx 0.5GHz -4dB	2
34	RG_{MAX}-RB_{01}	Rx 0.5GHz -4dB	2	75	TG_{MAX}-TB_{02}	Tx 0.5GHz -8dB	2
35	RG_{MAX}-RB_{02}	Rx 0.5GHz -8dB	2	76	TG_{MAX}-TB_{03}	Tx 0.5GHz -12dB	2

36	RG_{MAX}-RB_{03}	Rx 0.5GHz -12dB	2	77	TG_{MAX}-TB_{04}	Tx 0.5GHz -16dB	2
37	RG_{MAX}-RB_{04}	Rx 0.5GHz -16dB	2	78	TG_{MAX}-TB_{05}	Tx 0.5GHz -20dB	2
38	RG_{MAX}-RB_{05}	Rx 0.5GHz -20dB	2	79	TG_{MAX}-TB_{06}	Tx 0.5GHz -24dB	2
39	RG_{MAX}-RB_{06}	Rx 0.5GHz -24dB	2	80	TG_{MAX}-TB_{07}	Tx 0.5GHz -28dB	2
40	RG_{MAX}-RB_{07}	Rx 0.5GHz -28dB	2	81	FO	Factory Gain Offset	1
41	TG_{MAX}	Tx 4GHz 0dB	2	82	TAO	Tx Attenuator Offset	1
				83	RAO	Rx Attenuator Offset	1

Table 3-25 ***Calibration Data***

3.2.6 Control and TT&C

3.2.6.1 I²C Temperature Sensor

Read and record temperature sensor data. The entire automatic test sequence should be performed immediately after switching on units from cold, warm units should be left to cool for 30 minutes before retesting. The Maximum limit for acceptance is a temperature reading equivalent to 32 degrees centigrade (hex. 20). Refer to 'Reading Board Temperature' for conversion table.

3.2.6.2 TRM TT&C Interface

Confirm the following truth table.

Test Condition				**Acceptance Criteria**					
Input: Modem to IFP Bit-stream on J6 pin 17				**Output: IFP to mmW Unit on J10**					
Bit 13	**Bit 14**	**Bit 15**	**Bit 21**	**Pin1&11**	**Pin2&12**	**Pin5&15**	**Pin6&16**	**Pin3&13**	**Pin4&14**
1	0	1	0	11>1	12>2	15>5	16>6	3>13	14>4
0	0	1	1	1>11	12>2	5>15	16>6	13>3	14>4
1	1	0	0	11>1	2>12	15>5	16>6	13>3	4>14
0	1	0	1	1>11	2>12	15>5	6>16	13>3	14>4

Table 3-26 ***mmW Module Commands***

I/P Message identifier should be 0_{16} and bits 51 to 65 should be low unspecified parts of the bit-stream are 'don't care'.

Outputs on J10 are differential pairs, 11>1 indicates voltage on pin 11 is higher than voltage on pin1.

All other outputs on J10 are un-buffered versions of inputs from J6, these will be tested at ICT/Flying Probe.

3.2.6.3 Synth TT&C Interface

Confirm the following truth table.

Test Condition			**Acceptance Criteria**									
I/P: Bit-stream on J6 pin 17			**Output: IFP to Synth on J8**									
Bit 22-37	**Bit 38-45**	**Bit 46**	**Pin 8 (Serial)**	**Pin 17**	**Pin 18**	**Pin 19**	**Pin 20**	**Pin 21**	**Pin 22**	**Pin 23**	**Pin 24**	**Pin 7**

$AAAA_{16}$	55_{16}	1	$AAAA_{16}$	0	1	0	1	0	1	0	1	1
5555_{16}	AA_{16}	0	5555_{16}	1	0	1	0	1	0	1	0	0

Table 3-27 ***Synthesiser Commands***

I/P Message identifier should be 0_{16}, unspecified parts of the bit-stream are 'don't care'.

All other outputs on J8 are un-buffered versions of inputs from J6, these will be tested at ICT/Flying Probe.

3.2.6.4 MODEM TT&C Interface

Confirm the following truth table.

Test Condition			**Acceptance Criteria**		
Inputs to IFP			**Output: bit-stream on J6 pin 21**		
J8 Pin 37	**J8 Pin 25**	**J10 pin 18**	**Bit 4**	**Bit5**	**Bits 8 to 15**
1	1	+3.2V+/- 0.005V	1	1	F716 to F916
0	0	+0.49V+/- 0.005V	0	0	2516 to 2716

Table 3-28 ***Testing Return Bit-Stream to MODEM***

Message identifier on return bit-stream should be 0_{16}, all unspecified bits should be ignored.

All input commands on J6 will be proven by the other tests in this specification.

3.3 Recording of Test Data

All test data shall be recorded electronically and made available in a database for statistical analysis at a later date. Results files shall be in Excel comma separated variable format and should contain all the relevant results as well as the following information:

Date

Unit Serial No.

Temperature

Test Specification No. and Issue

Test Stage

The following file naming convention shall be used for production test results electronic data files

File=ifp_xxxxxxyyyzzz.csv

Where:

xxxxxx	is the unit serial no.
yyy	is the nominal temperature of the test
zzz	is the Test Stage (i.e. LFT, FFT, EFT or DVT)

The recorded data file shall contain a copy of the file written to the calibration EEPROM in addition to the other results.

Full format (memory map) for test record file is TBD.

END OF DOCUMENT