Radiant Broadband Wireless Access Network

Production Test Specification for Synthesiser (Band II) Boards

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7.0	JWM	24/07/02	Changes to Table 9 & 12 and para 4.7 and addition of section 5

Change History:

Page No.	Change Detail
18 & 27	Output Power Level requirements changed.
10 & 11	Synth Cal. data : Channel Spacing; Start/Stop Freq & VCO Sensitivity
10 & 11	Synth Cal. Data: VCO Sensitivity
21	Output Power measurement details
28	Remove 100MHz offset measurement
18	Improve –8Volt supply tol. with respect to current drawn.
24	Add Fault Finding Section

Whilst we have endeavoured to ensure that the contents of this document are as accurate as possible,

Radiant Networks take no liability for any errors or omissions within this document.

The ongoing development of our products and systems means that we reserve the right to update these documents at any time.

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HEALTH AND SAFETY

Attention is drawn to the Health and Safety at Work etc. Act 1974 as amended by the Consumer Protection Act 1987.

All testing related to this document shall be based upon adequate safety procedures including, but not limited to, safety designed and regularly maintained test equipment.

Written test instructions based upon this document shall contain warnings in respect of all potential hazards, where applicable.

CONTENTS

TABLES

FIGURES

REFERENCES

[1] RBWAN: 05_203, "Radiant Node Phase-1 IF Module Engineering Specification, ETSI Variant for Bands I and II". (V06 or later)

[2] ETS300 019-1-4: ETSI "EE; Environmental conditions and environmental test for telecommunications equipment; Part 1-4: Classification of environmental conditions stationary use at non-weather protected locations.

[3] RBWAN: Band-2 Synthesiser Specification 06-260Vxx

[4] RBWAN: Band-2 Synthesiser Test Specification 07-261Vxx

[5] RBWAN: Environmental Requirements Specification 02-206Vxx

[6] RBWAN: Synthesiser Board Specification 06-260Vxx

[7] ITU 'Series X: Data networks and open systems communications IT – ASN.1 encoding rules, ITU-T X.690.

[8] Radiant Networks, 'Specification for Production Data Collection' 000101-02

[9] Philips Semiconductors 'The I^2C-Bus Specification', Version 2.1, Jan 2000

[10] National Semiconductor, LM83 Triple-Diode input and local digital temperature sensor with two wire interface, DS101058.

[11] Refer to Dallas data sheet DS1669 for details of setting Digital Potentiometers.

1 General Description

The Radiant Networks Broadband Wireless Access System uses mm-Wave radio links that form the backbone on which the data payloads are carried. These RF links require a Digital Modem, Up / Down conversion Tx/Rx IF paths and frequency source module. The frequency source generates the agile local oscillator, which drives the mm-wave module. The equipment is required to operate in two frequency bands as indicated in Table 1.

Frequency Band	Frequency Coverage	Band Definition
I	24.563GHz to 26.439GHz	64 x 28MHz + Guard Band
II	27.5625GHz to 29.4385GHz	64 x 28MHz + Guard Band

Table 1: Band Definition

1.1 Functional Description

1.1.1 Synthesiser Assembly (770500)

The printed circuit board assembly consists of the Indirect second order type two phase locked loop and an auxiliary multiplier arrays that produces the necessary pre-scaling frequencies within main loop. Optional voltage controlled oscillators tuning from 5.1GHz to 5.6GHz for band I and 5.8GHz to 6.4GHz for band II are at the heart of the main loop. These are maintained in phase lock, via loop error signal derived from stable frequency clock of 10MHz. The frequency accuracy of this source is trimmed by the reception of 'Off- Air' standard from GPS source, as well as being temperature controlled. The loop error signal is derived from the comparison of 14MHz signal that tracks the 10MHz standard and the pre-scaled loop divide by N output of VCO input. The resultant error signal from the Phase / Frequency comparator feeds a Charge Pump and via Transitional Lead Lag filter (forming the second order loop filter) thereby subsequently controlling the VCO set frequency.

Due to the non-linear aspects within the main synthesizer, a calibration arrangement maintains loop management. The loop corner frequency is normalized at around 1.5MHz and the loop damping factor is controlled, so as not to exceed Single Side Band Phase Noise requirements. This wide loop bandwidth in conjunction with loop pre-tuning ensures fast switching and agility and reduces the synthesizer susceptibility to microphony sources.

Table 2 below indicates the frequency coverage of the Synthesizer output forming the Local Oscillator drive to the mm-Wave module.

Frequency Band	Frequency Coverage	Number Of Channels
I	10.248GHz to 11.186GHz	64
II	11.746GHz to 12.684GHz	64

Table 2: Frequency Coverage

Each frequency band consisting of a lower and upper segmented band consisting of 32 channels. See para 4.4.2 & 4.4.3 for details.

1.1.2 Interface Connections For Synthesiser

1.1.2.1 Control Signals between IFP and Synthesiser.

J2 Pin Number	Function	J2 Pin Number	Function
1	CH Strobe	2	0V
3	0V	4	TXRX_REF_DAC_CLK
5	TXRX_REF_DAC_CS	6	IFCFG_XLXDOUT
7	Cal Enable	8	TXRX_REF_DAC_DATA
9	0V	10	0V
11	0V	12	0V
13	0V	14	10MHz _REF
15	0V	16	0V
17	CH 7 (82)	18	CH 6 (42)
19	CH 5 (22)	20	CH 4 (12)
21	CH 3 (81)	22	CH 2 (41)
23	CH 1 (21)	24	CH 0 (11)
25	Ld synth Ref	26	0V
27	0V	28	IFCFG_XLXPGM_N
29	IFCFG_XLXCLK	30	IFCFG_XLXINIT_N
31	IFCFG_XLXDONE	32	IFCFG_RESET
33	SPARE 0	34	SPARE 1
35	SPARE 2	36	IFCFG_XLXM0
37	CAL_REQUIRED	38	SCL
39	SDA	40	N/U

Table 3: Control Signals between IFP and Synthesiser

Note: N/U is not used.

1.1.2.2 Supply Connections between IFP and Synthesiser.

J4 Pin Number	Function
1	-8V
2	+6.5V
3	0V
4	0V
5	+13.5V

Table 4: Supply Connections between IFP and Synthesiser

1.1.3 Factory Set Link Positions

Ensure J2 pin 36 of Reference Synthesiser is connected to ground (0V). Alternatively link pins 1 & 2 of J1.

1.1.4 Test Firmware

The Synthesiser has no none-volatile memory hence it will need to download firmware from the test system at PCB power up. Each unit will only be tested for one band. The latest version of the firmware described in Table 5 will be used for all tests. Firmware may be added to PROM U13 if remote system not available.

Band	Firmware Doc.
1	390040.XX
2	390020.XX

Table 5: Test Firmware

XX = Latest Version

1.1.5 External Trimming of 10MHz Clock Reference By I^2C Port

10MHz Clock Reference that is a VTCXO (Y2 or Y3) is held to tolerance frequency by means of decoded I^2C port data input. The VCXO has a tuning range of ±10ppm of nominal frequency with control voltage of 2.5Volts ±2Volts. The I^2C port data input defines full scale as $(FFFF)_H$ for 4.4999Volts tuning voltage, $(8000)_H$ as mid range 2.25Volts, $(0001)_H$ as 68.6645µVolts and $(0000)_H$ as 0Volts. See para 1.6.9.

The following defines the I^2C port connection details for tuning input.

J2 Pin Number	Function	Signal Designation
8	Data	TXRX_REF_DAC_DATA
4	Clock	TXRX_REF_DAC_CLK
5	Chip Select	TXRX_REF_DAC_CS
2	0V	Ground

Table 6: I^2C Port Connection Details for Tuning Input

1.1.6 Build Status I^2C Port

The calibration and build status EEPROM should be loaded with a single bit-stream consisting the contents of the right hand column of table 7, reading from top to bottom and left to right. The EEPROM specification is provided in table 8. The Bit-stream format conforms to ITU-T X.690 see para 1.6.7.

Byte String Type	Application Name	Hex code
Application tag	Synthesiser Configuration	7C
Length		80
Primitive Application Tag	Part Number	40
Length of data		06
Part number		37,37,30,35,30,30 (Note 1)
Primitive Application Tag	Issue Number	41
Length of data		02
Issue number		30,31 (Note 2)
Primitive Application Tag	Modification State	42
Length of data		02
Modification state		30,30 (Note 3)
Primitive Application Tag	Serial Number	43
Length of data		06
Serial number		30,30,30,30,30,31(Note 4)
Primitive Application Tag	Date Code	44
Length of data		06
Date code		30,35,30,36,30,31(Note 5)
Primitive Application Tag	Site Code	45
Length of data		01
Site code		41 (Note 6)
Primitive Application Tag	If Synth Calibration Data	4B
Length of data		1C
Version		03, 00, 00, 00
VCO Sensitivity		16, 2F, 99, 4E (Note 12)
Channel Spacing		8C, 00, 00, 00 (Note 9)
Start Frequency		D4, CA, 01, 00 (Note 7)
Stop Frequency		78, EF, 01, 00 (Note 8)
IF Frequency		01, 9F, 00, 00 (Note 10)
10MHz Calibration Ref.		5A, 98, 00, 00 (Note 11)
End of contents		00
End of contents length		00

Table 7: Calibration and Build Status EEPROM Memory Map

Each decimal bit is converted into ASCII and then encoded into Hex.

Note 1: Part number will be as per bar-code label - 770500.

Note 2: Issue number will be as per bar-code label - 01.

Note 3: Modification state will be as per bar-code label - 00.

Note 4: Serial number will be as per bar-code label - 000001.

Note 5: Date code will be DDMMYY - 5th June 2002.

Note 6: Site code will be as per barcode label -A.

Note 7: Synthesiser (Start) Lower frequency as specified – 11.746GHz.

Note 8: Synthesiser (Stop) Upper frequency as specified – 12.684GHz.

Note 9: Synthesiser channel size as specified – 14MHz.

Note 10: IF Frequency as specified – 4.0705GHz.

Note 11: 10MHz Calibration Ref. DAC as measured – 39002

Note 12: VCO Sensitivity range as specified – 5.1E-5 parts

Bar-Code Label Example:

770500-01-00-A Ser No. 000001

Where: 770500 = Assy Part Number
01 = Issue
00 = Modification State
A = Production Site Code.

Refer to 'Specification for Production Data Collection' see para 1.6.8 fully defines the bar-code label.

J2 Pin Numbers	EEPROM Parameter	EEPROM Specification
39	SDA (Serial Data/Address)	Standard I^2C (See para 1.6.8)
38	SCL (Serial Clock)	Standard I^2C (See para 1.6.8)
	I^2C Address	1010111
	Start offset address for data	00
	Write Control (TP# TBD)	Write Protect = open or VIH Write Enable = VIL
	EEPROM Size	256 Bytes

Table 8: EEPROM Specification

1.2 Mechanical Description

1.2.1 Mechanical Overview

The complete IFP and Synthesiser board assemblies are mounted in a screen enclosure consisting of a aluminium box with lids. Both the IFP and Synthesiser boards have surface mounted components mounted on top and underside. The IFP underside components have defined areas individually screened from adjacent circuitry by welled areas in the bottom of the mating enclosure. The topside of board like wise has welled areas in the covering lid.

The Synthesiser board assembly is mounted on the opposite side of enclosure bulkhead with the RF surface facing towards side mounting panel lid. Individual areas on the RF side of board have screening cans and lids. This arrangement enhances the EMC/RFI performance of inter-stage topologies.

DC connection between each board is via 5 way plug and socket. The command and control signals via 40 way board mounting plug socket arrangement. All the RF connections to the IFP and Synthesiser boards are via SMA PCB mounted micro strip transition connectors.

Partial access on the IFP side of the integrated module allows setting of DIL switches for local control and connection to 6 way socket for input DC supplies. A 20 way right angle mounting PCB socket protrudes through the side enclosure of the box from the IFP board enabling connection to Modem.

1.2.2 Maximum Overall Dimensions of IFP / Synthesiser Module Assembly

Height	35.5mm
Width	134mm
Length:	173.2mm

1.2.3 Weight

777.6gm

1.3 Electrical Specification

See Engineering Defining Specification for general electrical specification (06_260Vxx).

1.4 Mechanical Specification

For further details refer to the Engineering Defining Specification for Synthesizer (06_260Vxx).

1.5 Environmental Specification

1.5.1 Operating Temperature

-35 °C to +65 °C (This includes 20°C rise in temperature)

1.5.2 Storage Temperature

-40°C to +85°C

1.5.3 Test Conditions

For the purposes of these Production Acceptance Tests, the normal factory environmental conditions shall be within the following limits:

Temperature +15ºC to +28ºC

1.6 Mechanical Tests Conditions

1.6.1 General

Inspection procedures shall be carried within the framework of the assembly house's internal Quality Procedure.

1.6.2 ICT Testing

Each Board shall require ICT testing. Using fixtureless Flying Probe test systems that are available with very fine accuracies, optical positioning systems and high probing rates. Radiant Networks shall provide adequate information to allow the flying probe test to be programmed (e.g. gerber data & schematic). With the up to 6 high speed independently moving probes the Flying Probe test system allows to test up to 70 - 80 tests per second, shorts and opens data will be supplied to the CAD system. When the Board tests will be completed the operator will have the pass/fail indication. The test system shall allow a failure report on tested sub assemblies to help with the diagnostics and repair.

1.7 Special Handling Precautions

1.7.1 ESD

Ensure that precautions are taken regarding static sensitive components on all PCB assemblies.

1.7.2 Heat

Ensure that exposed skin does not come in contact with U10 (TO 220 Package) when the board is powered up as the device is not mechanically fitted to heat sink and will get hot!

1.8 Safety Requirements

1.8.1 Health and Safety

The Health and Safety at Work etc Act 1974 as amended by the Consumer Protection Act 1987 and all applicable regulations made under them e.g. The Control of Substances Hazardous to Health Regulations 1988, and The Electricity at Work Regulations 1989.

1.8.2 Standards

In addition to the above, by reference to the Functional Requirement the relevant National or International Standards shall be used to establish the detailed safety requirements appropriate to the product, especially those that require special tests and formal records.

The above shall equally apply to all test equipment and facilities used, and the product under test. Any hazardous activity shall be carried out subject to a detailed Written Safe System of Work and only by suitably qualified staff.

1.8.3 WARNING

ALL WARNING MESSAGES INDICATE A RISK TO LIFE. APPLY THE REQUIRED SAFETY PRECAUTIONS WHEN WORKING WITH THIS UNIT.

1.8.4 CAUTION

1.8.4.1 All Caution messages indicate a risk of personal injury or possible damage to equipment.

1.8.4.2 Under certain fault conditions parts of this unit can run hot. Wear the appropriate protective clothing.

2 TEST EQUIPMENT

2.1 General Conditions

All test equipment in this section shall be in a valid calibration state when used and shall display a current calibration label to this effect. Suitable alternative equipment may be used where appropriate.

2.2 Standard Test Equipment

Item	Number	Title	Example
2.2.1	1	Oscilloscope 1GHz Sample Rate	LeCroy LC584AL
2.2.2	1	Synthesised Generator	HP E4422B or similar
2.2.3	1	Spectrum Analyser 9KHz to 26GHz Including Phase Noise Utility	HP8563E 85671A
2.2.4	1	Dual Power Supply	Farnell LT30-2 or similar
2.2.5	1	Single Power Supply	Farnell LT 30-1 or similar
2.2.6	1	Digital Voltmeter	Fluke 45 or similar
2.2.7	1	X10 Oscilloscope Probe	General Elektronik GmbH GE1511
2.2.8	1	Probes for Voltmeter	Radio Spares (Stock No. 340-2421)
2.2.9	1	SSB Phase Noise Kit	Aeroflex / Comstron PN9000B or similar
2.2.10	1	Power Meter	HP EPM-441A
2.2.11	1	Power Head Sensor	HP ECP-E18A
2.2.12	1	Frequency Counter	HP5343A
2.2.13	1	Off Air Frequency Standard	Quartzlock 2.A
2.2.14	1	Personnel Computer	DAN or similar
2.2.15	1	Active Probe 300KHz to 3GHz	HP 85024A + Opt W30

2.3 Miscellaneous Test Items

Item	Number	Title	Example
2.3.1	2	SMA Socket to N Plug Adapter	Rosenberger Pt.No. 53S132-K00D3
2.3.2	2	SMA Socket to SMA Socket Adapter	Rosenberger Pt. No. 32K101-K00D3
2.3.3	2	SMA Plug to SMA Plug Adapter	Rosenberger Pt. No. 32S103-S00S3
2.3.4	2	1Meter SMA to SMA Plug to Plug	Rhophase P4724
2.3.5	2	SMA Plug to N Plug Adapter	Rosenberger Pt. No. 32S153-S00D3
2.3.6	1	SMA Plug 50ohm Load 1 Watt	Rosenberger

			Pt. No. 32S15A-1.0D3

2.4 Special Test Equipment

Item	Number	Title	Example
2.4.1	1	Interface Test Jig	In House Design
2.4.2	1	Cable Assembly [A]	See para 6.1
2.4.3	1	Cable Assembly [B]	See para 6.2
2.4.4	1	Cable Assembly [C]	See para 6.3
2.4.5	1	Cable Assembly [D]	See para 6.4
2.4.6	1	Cable Assembly [E]	See para 6.5
2.4.7	1	Battery Box	In House Design or similar
2.4.8	1	Switching Time Kit	In House Design or similar
2.4.9	1	Cable Assembly [F]	See para 6.6

3 INTERPRETATION OF RESULTS

3.1 Accuracy

In compiling this document, due allowance has been made for the inherent inaccuracy of the particular test equipment specified and the figures and limits quoted are the actual indications to be obtained.

3.2 Recording of Results

3.2.1 Quantitative

Record the indicated measured value where applicable.

3.2.2 Non-Quantitative

If the observed result fulfils the test requirements, record as '✔'.

3.2.3 Test Results

All test results must be entered on a Test Record Sheets (see pages 14 to 16) paying particular attention to the serial number of the UUT, and any authorised concession(s) and/or Inspection/Test Record.

Ensure the test results are within the list of limits detailed in Section 6.

4 ALIGNMENT & ELECTRICAL TESTS OF SYNTHESISER ASSY

4.1 Preliminary Tests

4.1.1 Connect Multi-meter Item 2.2.6 set to measure resistance on the 200ohm range between the 0V pins 3 & 4 of J4 and the three supply rails +13.5V, +6.5V & -8V, these being pins 5, 2 & 1 of J4 respectively. Ensure the measured resistance is not less than 10ohms.

4.1.2 Connect Test Jig Item 2.4.1, 40 way header via IDC socket of Cable Assembly [C] Item 6.3 to J2 ensuring correct orientation with pin 1 of socket. Connect supply Cable Assembly [D] Item 6.4 to two Power Supplies Items 2.2.4 & 2.2.5 set for +13.5V, +6.5V & -8V and position the 5 way socket end onto J4 again ensuring the correct orientation with pin 1 of socket. Both pin's 1 of J2 & J4 are defined by the square pad on underside of PCB.

4.1.3 Ensure shorting link is fitted between pins 1 & 2 of J1.

4.1.4 The controls on the Test Jig Item 2.4.1 should be set as follows. Set both channel defining hexadecimal switches to $(10)_H$, set **Calibration Enable** switch to **OFF** (Cal is performed: Logic HIGH) and place shorting link onto J5 of Test Jig.

4.1.5 Connect J3 on Test Jig to COM Port 1 of Computer Item 2.2.14 using Cable Assembly [E] Item 6.5.

4.2 Initial Tests

4.2.1 Switch power supplies **ON** and press **Reload FPGA** button on Test Jig Item 2.2.12. Check the metered currents on each supply line fall between the limits specified in Table 9.

Supply Rails	Min. Current	Typ. Current	Max. Current
+13.5 volts	30mA	40mA	62mA
+6.5 volts	0.897A	1.056A	1.215A
-8 volts	25mA	33mA	59mA

Table 9: Initial Tests – Supply Rails

4.2.2 Check the following sub-regulator outputs with Digital Multi-meter Item 2.2.6 set to appropriate range at the points defined below.

TP30 or positive end of C245 will be +5.0V ±200mV.

TP31 or positive end of C86 will be +3.3V ±200mV.

TP29 or positive end of C50 will be +5.0V ±200mV.

TP28 or positive end of C80 will be +12.5V ±200mV.

TP27 or the negative end of C42 will be –5.5V ±200mV.

4.2.3 Connect Frequency Counter Item 2.2.12 to the 10MHz monitor point on Test Jig J3. Connect External 10MHz Reference of Frequency Counter to Off Air Frequency Standard Item 2.2.13. Monitor voltage level at TP 35. Adjust for 2.5 Volts ± 100mV by tapping on the **Page Up/Page Down** keys of Computer Item 2.2.14 for course setting and +/- keys for fine (nominal Hex value of 985A).

4.2.4 Adjust mechanical trimmer on Y2 or Y3, so that the monitored 10MHz on Test Jig J3 is set to within ±2Hz.

4.2.5 Press the Reload FPGA button on Test Jig. Both **Load Synthesiser Reference** & **CAL Required** LED's (RED & GREEN respectively), and the three LED's on the Synthesiser Reference board will go **OFF**. When the button is released, the RED & GREEN LED's on Test Jig will be ON, D2 & D4 on the Synthesiser Reference board will be **ON** and D1 **OFF**.

4.3 Loop Management Settings

4.3.1 Connect Frequency Counter Item 2.2.12 to SYN_1 port. Ensure SYN_2 is terminated. Press the **Channel Strobe** button as required so that monitored frequency indicates 11.97GHz (this may involve a few Channel Strobes). Next observe the status of the following Test Jig LED's:

RED LED will be **OFF** at this stage
GREEN LED will be **ON** at this stage

The Synthesizer Reference Board will indicate the following LED's:

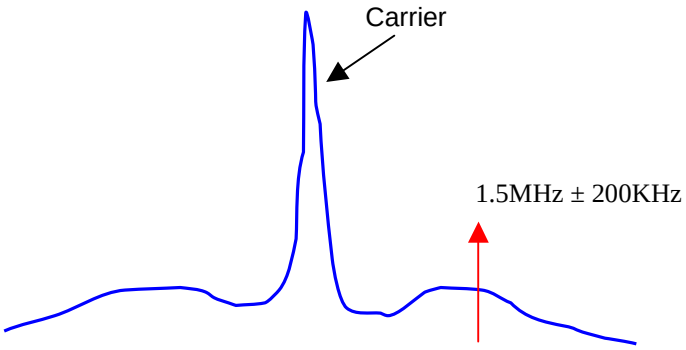
D4 will be **ON**
D1 & D2 will be **OFF** at this stage.

4.2.2 Connect the negative probe of Digital Multi-meter Item 2.2.6 on to a convenient ground point and probe **TP109** with positive probe. Adjust **U78** Digital Potentiometer (refer para 1.6.11) via J7 adjustment interface Item 2.4.9 for an indicated reading of 0.15V ±50mV.

4.3.3 Monitored **SYN_1** Output on Spectrum Analyser Item 2.2.3 and set Analyser as follows:

Centre Frequency	11.97GHz
Span	10MHz
Resolution Bandwidth	10KHz
Video Bandwidth	100Hz
Manuel Attenuator	20dB
Reference Level	10dBm

4.3.4 Adjust **U78** Digital Potentiometer (refer para 1.6.11) so the '**Hump**' (see below) as viewed either side of the Carrier centre frequency is set for 1.5MHz ±200KHz. The correct adjustment is at the point when the noise just falls away.



4.3.5 Connect the negative probe of Digital Multi-meter Item 2.2.6 on to a convenient ground point and probe **TP89** with positive probe. Adjust **U29** Digital Potentiometer via J8 for an indicated reading of -0.3V ±50mV.

4.3.6 Connect a square wave source to Channel Strobe connector J2 on Test Jig. Probe **TP74** (Drain of Q15) with Digital Multi-meter and note reading. Next probe **TP69** with Item 2.2.6 and re-adjust **U29** for the previously noted voltage plus 0.5Volt ±50mV.

4.3.7 Remove square wave source from Test Jig and repeat para 4.3.3 & 4.3.4.

4.3.8 Check that D1 & D2 on Synthesizer Board are both **OFF** and the **Load Synthesiser Reference** & **CAL Required** LED's(RED & GREEN respectively) are **OFF** & **ON**.

4.3.9 Select channel code **$(FF)_H$ or $(7F)_H$** and press the **Channel Strobe** button on Test Jig. Note this paragraph should be repeated after any subsequent power up, before making any measurements of Synthesiser performance.

4.4 Check Frequency Coverage

4.4.1 Remove Spectrum Analyser from SYN_1 output and re-connect Frequency Counter Item 2.2.12. Set the Channel switches as indicated in Tables 10 & 11 (to save time note the lower, middle and top frequencies of Lower & Upper band's), noting output frequency when Channel Strobe button is pressed. Ensure LED's D1 & D2 are extinguished on releasing Channel Strobe button. The Red LED

on the Test Jig (LD Synth Ref.) will be **OFF** and the GREEN LED (Cal Required) will be **ON**. Note para 4.2.3 may need refining to meet output frequency grid requirements.

4.4.2 Band 2 Lower Channels.

Channel No. (Hex)	Output Frequency (GHz)	Channel No. (Hex)	Output Frequency (GHz)
00	11.746	10	11.97
01	11.76	11	11.984
02	11.774	12	11.998
03	11.788	13	12.012
04	11.802	14	12.026
05	11.816	15	12.04
06	11.83	16	12.054
07	11.844	17	12.068
08	11.858	18	12.082
09	11.872	19	12.096
0A	11.886	1A	12.11
0B	11.9	1B	12.124
0C	11.914	1C	12.138
0D	11.928	1D	12.152
0E	11.942	1E	12.166
0F	11.956	1F	12.18

Table 10: Band 2 Lower Channels

4.4.3 Band 2 Upper Channels.

Channel No. (Hex)	Output Frequency (GHz)	Channel No. (Hex)	Output Frequency (GHz)
24	12.25	34	12.474
25	12.264	35	12.488
26	12.278	36	12.502
27	12.292	37	12.516
28	12.306	38	12.53
29	12.32	39	12.544
2A	12.334	3A	12.558
2B	12.348	3B	12.572
2C	12.362	3C	12.586
2D	12.372	3D	12.6
2E	12.39	3E	12.614
2F	12.404	3F	12.628
30	12.418	40	12.642
31	12.432	41	12.656
32	12.446	42	12.67
33	12.46	43	12.684

Table 11: Band 2 Upper Channels

4.5 Spurious

4.5.1 Remove Frequency Counter from **SYN_1** output and reconnect Spectrum Analyzer appropriately set. Set Channel switches to $(00)_H$, $(10)_H$ and $(1F)_H$ respectively, ensuring Channel Strobe is pressed for each setting. Ensure all spurious components are better than 50dBc over offset frequency coverage of ±100KHz out to ±100MHz.

4.5.2 Repeat para 4.5.1 for Channel settings of $(24)_H$, $(34)_H$ and $(43)_H$.

4.6 Phase Noise Measurement

4.6.1 Set channel for $(43)_H$ ensuring **Channel Strobe** is pressed. Remove Spectrum Analyser from **SYN_1** output and reconnect to Single Side Band Phase Noise measuring kit Item 2.2.9. Ensure resultant profile is no greater than 10dB of the limits specified in Table 12. Remove Phase Noise measuring kit from **SYN_1** output

4.7 Output Power Level

4.7.1 Ensure Synthesiser PCB assembly is fully fitted to screen enclosure with all fixing screws fitted and tightened before continuing. Connect to the Power Meter Sensor Head Items 2.2.10 & 2.2.11, terminating **SYN_2** output in 50 ohms. Repeat para 4.5.1 channel settings, noting output power level. Ensure measured level is not less than +5dBm. Repeat for para 4.5.2 channel settings.

4.7.2 Repeat para 4.7.1, but with the Power Meter connected to **SYN_2** output with **SYN_1** output terminated in 50 ohms. Ensure measured level is not less than +5dBm. Repeat for para 4.5.2 channel settings.

4.8 Reference Output

4.8.1 Monitor **TP116** or J5 on the Synthesiser board with the Power Meter and appropriate connector arrangement. Ensure the monitored level is –1.4dBm ±1dB.

4.9 Loop Switching Time

4.9.1 With the Switching Time measuring Kit Item 2.4.8 appropriately connected, measure the lock time while exercising the Synthesizer from channel $(00)_H$ to $(43)_H$. Ensure measured settling time is less than 5µSec for a better than 15KHz ±5KHz settling frequency.

4.10 Temperature Sensor

4.10.1 Read temperature sensor via I^2C port (see table 8 for details) check this is within +/- 4ºC of the ambient temperature of the PCB close to U28. The temperature sensor is set by command $(00)_H$ only to read temperature from the local sensor. Refer to para 1.6.9 & 1.6.10 for details of I^2C and data format.

I^2C Address of temperature sensor is 0101010.

5 FAULT FINDING PROCEDURE OF ASSEMBLY

5.1 General

If a fault situation exists while testing an individual circuit block, proceed as follows.

5.1.1 Check power supply connections and correct sub regulator outputs. See para 4.2.4 for details.

5.1.2 Check the circuit under test for incorrectly mounted components, wrong value or type of components, solder shorts, broken or missing components and broken tracks.

5.1.3 If more than one circuit block is being tested check all interface signals and confirm they are still valid. Use of the block diagram is most useful in understanding flow of circuits diagrams.

5.1.4 All the relevant circuits diagrams have interface signal levels defined.

5.1.5 When testing the Synthesiser a working model would be an advantage in comparative testing.

5.1.6 Component failures should be noted and reported back to manufactures.

5.2 Fault Finding Scenarios

5.2.1 Unlock LED D2 does not extinguish after subsequent Strobe pulses on power up.

5.2.1.1 448MHz loop not locking

First check that pin 14 of U25 is V_{HIGH} (Lock Detector) and tuning voltage to 448MHz SAWO is typically 2.2Volts at TP193.

- ***If not proceed as follows***

Remove L43 and inject variable voltage source Item 2.4.7 into TP194. Monitor TP250 with FET Active Probe Item 2.2.15 and Spectrum Analyser Item 2.2.3. Set voltage on TP194 to 2.2Volts, so that a 448MHz carrier is observed on Spectrum Analyser on narrow Span. If no carrier is present Y1 or associated circuit is likely to be at fault.

The 448MHz carrier is present. Monitor TP193 with X10 Probe Item 2.2.7 and Oscilloscope Item 2.2.1. When the injected voltage at TP194 is adjusted about the 448MHz carrier position, the monitored signal at TP193 should integrate from a V_{HIGH} to a V_{LOW} state or visa versa with a rather slow time constant wave shape. If not, U25 or associated circuitry is likely to be faulty.

Set input channel switches on Test Jig Item 2.4.1 to $(10)_H$ and Strobe a few times. If D2 then fails to extinguish the fault is in main loop. The monitored voltage at U18 pin 1(Sample_Error) should be approximately 2.2Volts. Thresholds defined within the FPGA of ±1.9Volts around the monitored level on U18 pin 1 determine lock status of main loop.

5.2.1.2 Main loop not locking

Set input channel switches on Test Jig Item 2.4.1 to $(FF)_H$ (Auto Cal. mode) and Strobe twice. Both D1 (CAL_REQUIRED) & D2 (UNLOCK) should extinguish.

- ***If not proceed as follows***

5.2.1.3 Check ÷N & ÷R operation

Set channel switches to $(10)_H$ and double Strobe. Remove LK1 and connect variable voltage source Item 2.4.7 to LK1 pins 2 & 3 using cable assembly Item 2.4.2. Monitor J21 with Frequency Counter Item 2.2.12 and set voltage source so that output frequency is set for 11.97GHz. Using X10 Probe and Oscilloscope monitor U9 pin 19 (÷N output). The waveform should be a PECL signal of 14MHz repletion rate that is variable with source voltage input. Note this signal tends to be rather jittery in nature when viewed open loop, so a hold or freeze function on Oscilloscope is useful feature. Monitor U8 pin 19 (÷R output), the signal should have a similar wave shape, but have a fixed frequency of 14MHz.

5.2.1.4 Check both Heterodyne Prescalers in main Synthesiser loop

If there is no signal present at U9 pin 19 monitor U1 pin 7 with FET Active Probe Item 2.2.15 and Spectrum Analyser Item 2.2.3. Set Spectrum Analyser to Centre Frequency 322MHz, Span to 100MHz, Resolution Bandwidth to 100KHz and Video Bandwidth to 10KHz. The signal present should be approximately +6dBm.

This signal can be traced back to the output of U21 pin 1 (Second Down Converter Mixer). The level measure here is approximately –7dBm.

The LO input to U21 pin 5 should be 1.218GHz at a level of approximately –1dBm.

The RF input to U21 pin 4 should be 896MHz at a level of approximately –10dBm. The switch (SW2) that proceeds the RF input of Mixer U21 pin 4, switches between two fixed frequencies of 896MHz and 1.344GHz. The transition between the two sources occurs between channels $(23)_H$ and $(24)_H$ and is defined by truth table on Sheet 3.

The First Down Converter in main loop consists of a Harmonic Mixer made up of D13 and associated circuitry. The LO drive to this circuit consists of a fixed frequency of 5.376GHz at a level of approximately –4dBm. With the voltage source set for output frequency of 11.97GHz (Channel 10_H) the resultant output of this mixer is 1.218GHz = {11.97GHz – (2 ∗ 5.376GHz)}.

Note all the fixed frequencies used in the Double Heterodyne down conversion within the main loop of the Synthesiser are derived from the 448MHz SAWO with appropriate multiplication.

- 448MHz ∗ 2 = 896MHz
- 896MHz ∗ 2 = 1792MHz
- 1792MHz ∗ 3 = 5376MHz

5.2.1.5 Check loop Phase Detector

While set to channel $(10)_H$ monitor the gate waveform on Q15 with Oscilloscope. Adjust source control voltage to LK1 pins 2 & 3, so as to slightly change output frequency of 11.97GHz. The signal monitored on the gate of Q15 will integrate between 0Volts and –5Volts and visa versa at the set frequency point of 11.97GHz.

5.2.2 Loop will not Auto_Cal

5.2.3 Connect continuous Strobe to Synthesiser Test Jig and set hex switches to Auto Calibration $(FF)_H$. Monitor U12 pins 1 & 7 with X10 Probe and Oscilloscope. The waveforms present should be of a ramp nature, which have a degree of symmetry but are not uniform. If there are discontinuities in the ramps then suspect fault. A similar ramp waveform is also present at LK1 pins 1 & 2. Look at Gold standard board to confirm shapes of waveforms if in doubt.

5.2.4 Problems previously noted

5.2.4.1 Main loop still does not locking

- ***If not proceed as follows***

When an external control voltage is applied to LK1 pins 2 & 3 to exercise the VCO (5.873GHz to 6.342GHz) {see Sheet 8}, as in previous paragraphs, ensure voltage range for frequency coverage is as follows: -

1. 5.873GHz (11.746GHz Channel 00_H) set control voltage approximately +3Volts ±1Volt.
2. 6.342GHz (12.684GHz Channel 43_H) set control voltage approximately +8Volts ±1Volt.

If the control voltage falls below (1) or above (2) then replace D16 Varactor.

Note if the output frequency appears stuck at 14GHz and will not respond to control voltage source then replace D16.

5.2.4.2 Main loop locks after Auto_Cal, but does not lock to curtain channels.

- ***If not proceed as follows***

Connect LK1 pins 2 & 3 via cable Item 2.4.2 to Function Generator. Set Function Generator for Ramp output, with output voltage swing of +2Volts to +9Volts at a repetition rate of 10Hz. Monitor U15 pin 6 (Gain stage output after Harmonic Mixer) with Active FET Probe Item 2.2.15 and Spectrum Analyser Item 2.2.3. Set START FREQ on Analyser for 990MHz, STOP FREQ for 1.43GHz and set trace for MAX HOLD. The waveform that is built up over band of 994MHz to 1.428GHz should be nominally flat with approximate level of -8dBm. If there is a 'notch out' or 'drop off' in any part of band waveform displayed then problem could be due to following circuit element: -

Coupled Amplifier/Filter stage driving RF port of Harmonic Mixer.

Harmonic Mixer (D13) and associated circuitry.

Buffer Amplifier (U15) and associated circuit proceeding Harmonic Mixer.

- ***If not proceed as follows***

Set channel to $(23)_H$ [Switches SW2 into 896MHz position].

Monitor U1 pin 3 (Line Receiver driving ÷N) with Active Probe. Set Spectrum Analyser START FREQ for 90MHz, STOP FREQ for 590MHz and set trace to MAX HOLD. The waveform that is built up over band of 98MHz to 588MHz should be nominally flat with approximate level of +1dBm. If there is a 'notch out' or 'drop off' in any part of band waveform displayed then problem could be due to following circuit element: -

U21 Second Down Converter.

U27 and associated circuit (Buffer Amplifier).

Set channel to $(24)_H$ [Switches SW2 into 1344MHz position].

Press TRACE 'A' CLEAR and then press MAX HOLD. The waveform that is built up while still monitoring U1 pin 3 over band of 154MHz to 588MHz should be nominally flat with approximate level of +1dBm. If there is a 'notch out' or 'drop off' in any part of band waveform displayed then problem could be due to following circuit element: -

U21 Second Down Converter.

U27 and associated circuit (Buffer Amplifier).

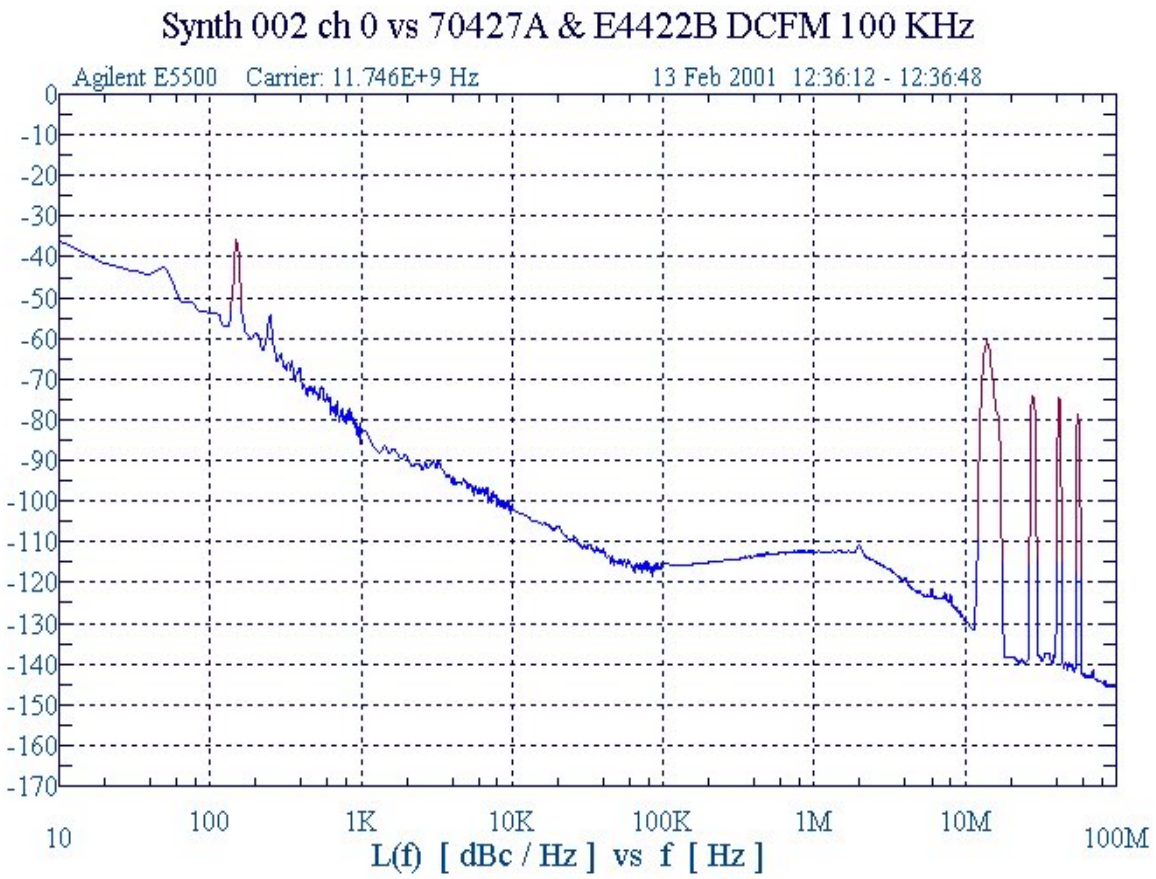


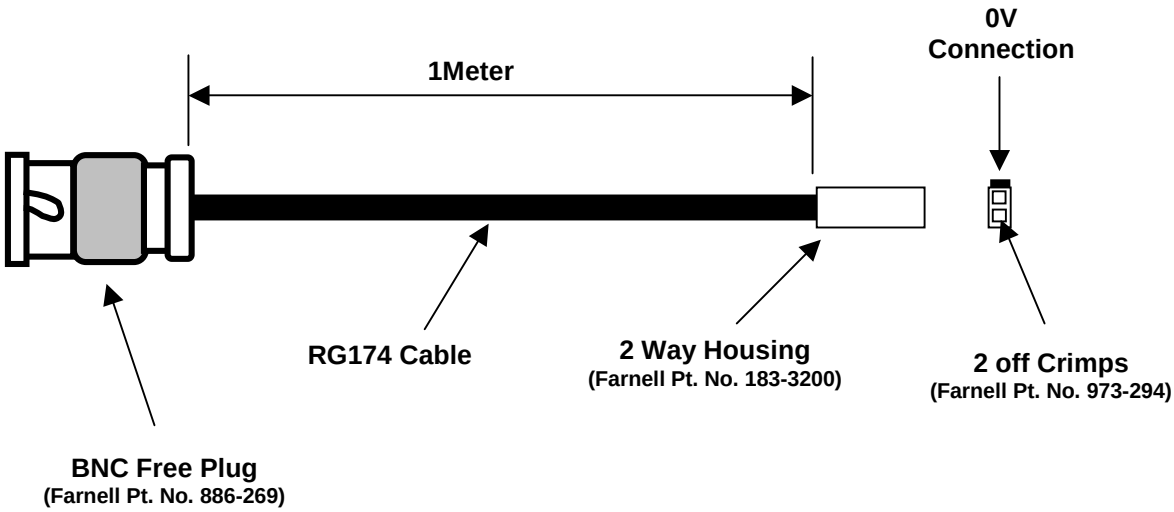
Figure 1: Typical SSB Phase Noise Plot At Channel $(00)_H$

Offset Frequency	Typical SSB Phase Noise (dBc)	Specification Limits
100Hz	-55	Not Specified
1KHz	-82	**-77**
10KHz	-102	**-97**
50KHz	-115	**-109**
100KHz	-116	**-109**
1MHz	-112	**-106**
10MHz	-130	**-123**

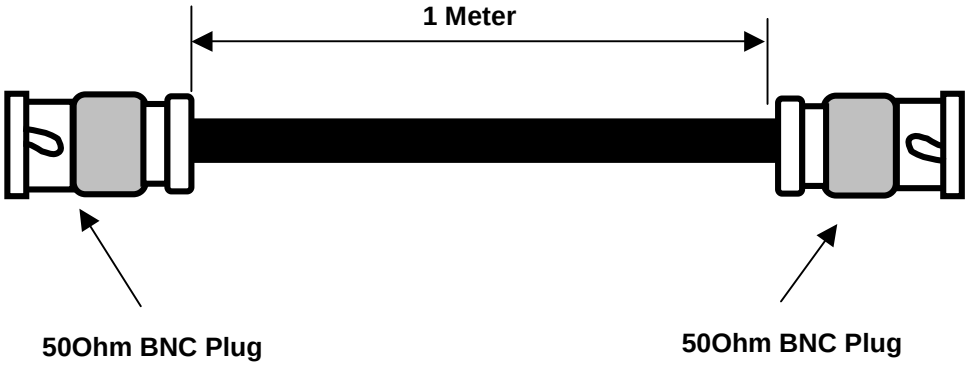
Table 12: Phase Noise Limits

6 Cable Assemblies

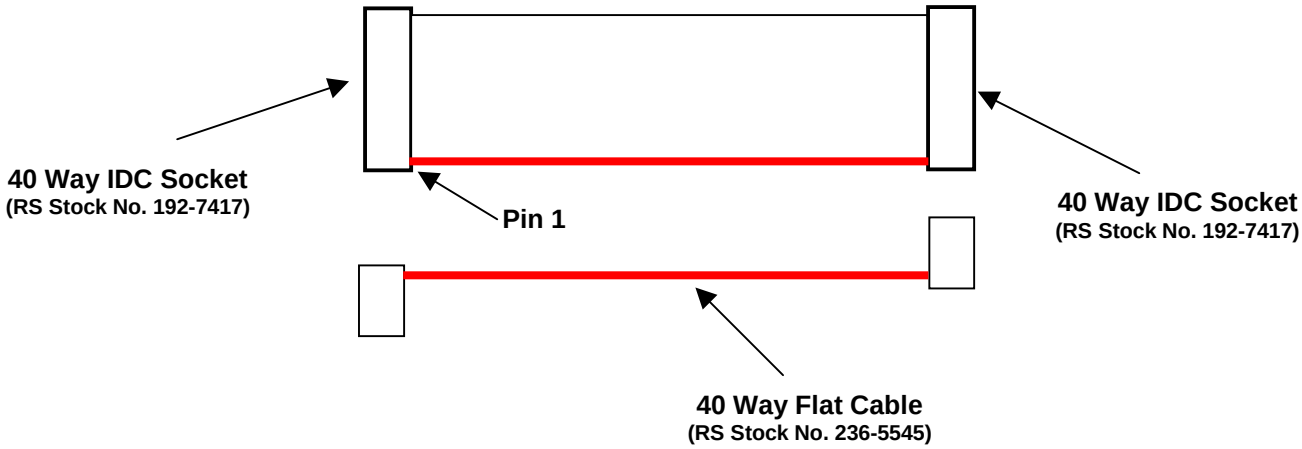
6.1 Cable Assembly [A] Construction Details



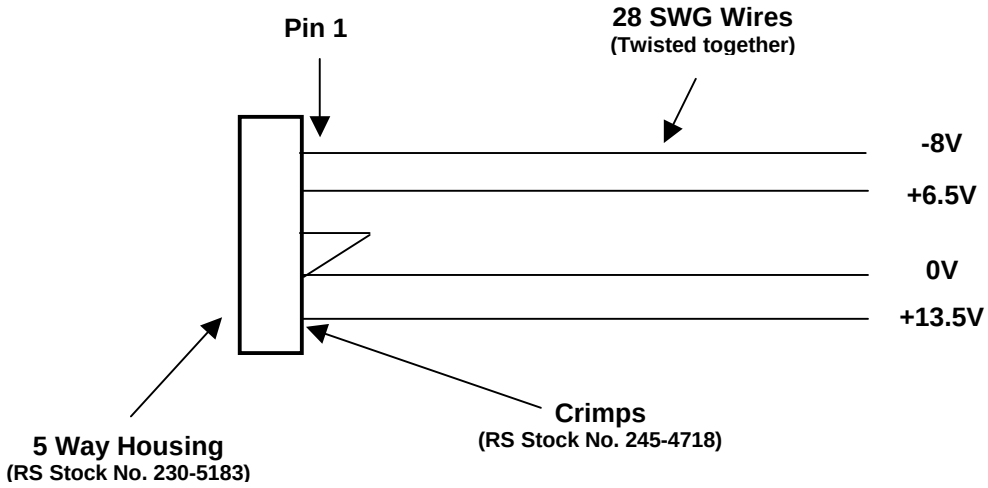
6.2 Cable Assembly [B] Construction Details



6.3 Cable Assembly [C] Construction Details



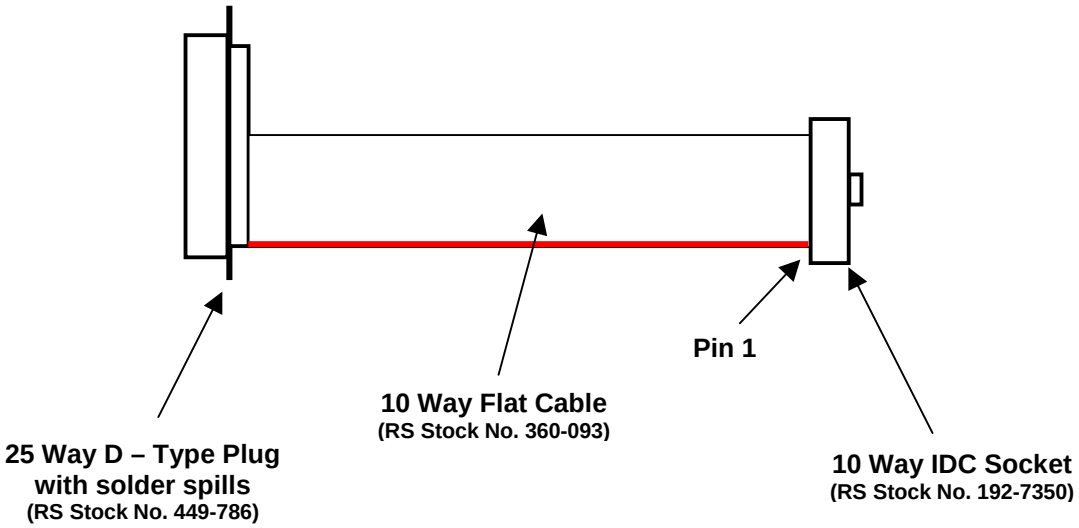
6.4 Cable Assembly [D] Construction Details



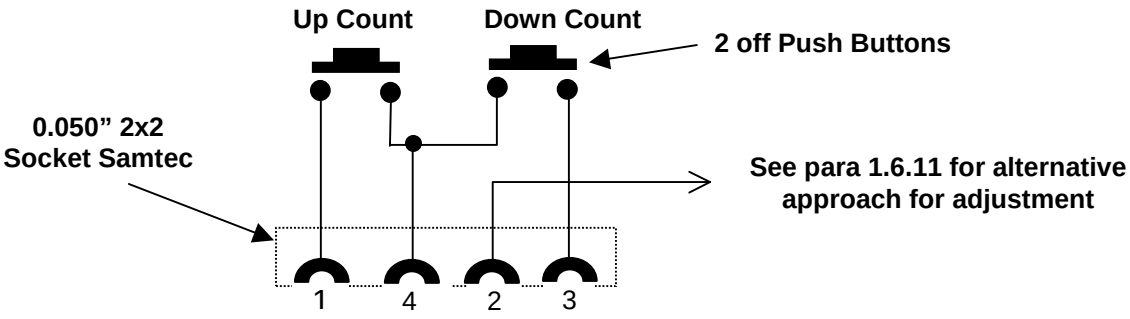
Pin No.	Description	Wire Colour
1	-8V	Violet
2	+6.5V	Orange
3	0V	Black
4	0V	Black
5	+13.5V	Red

6.5 Cable Assembly [E] Construction Details

25 Way D-Type Plug	10 Way IDC Socket	Function
2	1	TXRX_REF_DAC_DATA
3	2	TXRX_REF_DAC_CLK
4	3	TXRX_REF_DAC_CS
22	4	0V
22	5	0V
22	6	0V
	7	Not Used
	8	Not Used
	9	Not Used
	10	Not Used



6.6 Digital Potentiometer Interface [F]



7 TEST RECORD REQUIREMENTS

Sheet 1 of 4

Equipment: Synthesiser Reference Identity:

Test Procedure: Issue: Serial No:

Mod State

Customer/Project/Works No:

Tested By: Date: Stamp:

Test Para No.	Description and Limits	Results
4.2.1	**Supply Currents:** +13.5V 30mA min. 62mA max. +6.5V 865mA min. 1.215A max. -8V 25mA min. 59mA max.	
4.2.2	**Sub-Regulators Output Voltages:** TP30 +5V ±200mV TP31 +3.3V ±200mV TP29 +5V ±200mV TP28 +12.5V ±200mV TP27 -5.5V ±200mV	
4.2.3	**Monitor 10MHz Reference:** TP35 set level 2.5V ±100mV	
4.2.4	**Monitor 10MHz Reference:** 10MHz ±2Hz	
4.2.5	**Status Indicators:** **Test Jig** LD Synth Ref **ON** ‘✓’ Cal Required **ON** ‘✓’ **Synthesizer Board** D4 **ON** ‘✓’ D1 **OFF** ‘✓’ D2 **ON** ‘✓’	

TEST RECORD SHEET Continue… **Sheet 2 of 4**

Test Para No.	**Description and Limits**	**Results**
4.3.1	**Loop Management:** **Test Jig** LD Synth Ref (RED LED) **OFF** ‘✓’ Cal Required (GREEN LED) **ON** ‘✓’ **Synthesizer Board** D4 **ON** ‘✓’ D1 **OFF** ‘✓’ D2 **OFF** ‘✓’	
4.3.2	**Loop Management:** Set U78 +0.15V ±50mV Noted voltage at TP 109	
4.3.4	**Loop Management:** **Second Order Loop Corner** Set U78 1.5MHz ±200KHz	
4.3.5	**Loop Management:** Set U29 -0.3V ±50mV Noted voltage at TP 89	
4.3.8	**Status Indicators:** **Test Jig** LD Synth Ref **(RED LED)** **OFF** ‘✓’ Cal Required **(GREEN LED)** **ON** ‘✓’ **Synthesizer Board** D1 **OFF** ‘✓’ D2 **OFF** ‘✓’	

TEST RECORD SHEET Continue… **Sheet 3 of 4**

Test Para No.	Description and Limits	Results
4.4.2	**Frequency Coverage:** **Lower Band** Channel $(00)_H$ 1.746GHz ±23.5KHz " $(10)_H$ 11.97GHz ±23.9KHz " $(1F)_H$ 12.18GHz ±24.4KHz D1 & D2 **OFF** '✓' LD Synth Ref **OFF** '✓' Cal Required **ON** '✓'	
4.4.3	**Frequency Coverage:** **Upper Band** Channel $(24)_H$ 12.25GHz ±24.5KHz " $(34)_H$ 12.474GHz ±24.9KHz " $(43)_H$ 12.684GHz ±25.4KHz D1 & D2 **OFF** '✓' LD Synth Ref **OFF** '✓' Cal Required **ON** '✓'	
4.51	**Spurious 100KHz to 100MHz:** **Lower Band** Channel $(00)_H$ " $(10)_H$ >50dBc " $(1F)_H$	
4.5.2	**Spurious 100KHz to 100MHz :** **Upper Band** Channel $(24)_H$ " $(34)_H$ >50dBc " $(43)_H$	
4.6.1	**SSB Phase Noise:** Channel $(43)_H$	See attached plot

TEST RECORD SHEET Continue… **Sheet 4 of 4**

Test Para No.	Description and Limits	Results
4.7.1	**Output Power Level SYN_1:** Channel $(00)_H$ " $(10)_H$ +5dBm min. " $(1F)_H$ " $(24)_H$ " $(34)_H$ " $(43)_H$	
4.7.2	**Output Power Level SYN_2:** Channel $(00)_H$ " $(0F)_H$ +5dBm min. " $(1F)_H$ " $(24)_H$ " $(34)_H$ " $(43)_H$	
4.8.1	**Reference Output:** -1.4dBm ±1dB	
4.9.1	**Switching Time:** From channel $(00)_H$ to $(43)_H$ Switching Time <5µSec. Settling Freq. 15KHz ±5KHz	
4.10	**Temperature Sensor:** 1. Measured Ambient Temperature. 2. Temperature Sensor Output 2 – 1 = x°C ±4 °C	

END OF DOCUMENT