Circuit Description
For
RF900 Wireless remote

FCC ID

RF section:
The RF900 transceiver uses OOK (on/off keying) of a carrier, which can vary from 903 to 918 MHz in 1 MHz channel spacing with 15us bit times as it's signaling means. The carrier is derived from a PLL (phase lock loop) circuit that is controlled from the microcontroller (CPU). The same 4.000MHz crystal that is used to run the CPU is also used as the reference clock for the PLL.

The PLL has a lock detect output that is monitored by the CPU to ensure the carrier is on frequency before transmission is enabled.

As a message is built from data set to it from an external device such as a weight indicator, the CPU stores the message until all 105 bits have been received. The message then has a CRC calculated for it. The CPU then enables the transmitter circuit contained in the RF2915 transceiver chip. It then shifts out a serial command code by modulating the final power amp on and off.

Logic 1 is represented by carrier on and logic 0 by carrier off. When the amp is powered off during the 0 bits, the signal level drops by about 50dB. When both the transmitter IC and amp are disabled, the signal drops to less than -75dBm. The harmonics are kept low by way of a SAW filter on the output of the final power amp.

As the transmission occurs, the receiver end captures the transmitted bits. After all bits have been received, the CRC is calculated and compared to the CRC encoded in the data stream. If the CRC is determined valid, the message is processed for display. If the CRC is erroneous, a counter is started, if a sufficient number of bad messages are received, the "NODATA" message is displayed. After transmission is complete the transmitter goes into receive mode to listen for a request for button command. A request for button command will only occur if the user on the receiver end presses a button on the front panel.

Antenna:
The antenna is a copper plated wire. The antenna is permanently soldered to the PC board. The antenna input is designed around 50 ohms for easy production testing.

Receiver:
In receiver mode, the CPU enables an external LNA and internal mixer built into the RF2915 transceiver chip. The RSSI (received signal strength indicator) is monitored by the CPU's internal analog comparator to look for proper bit patterns from the transmitter.

The PLL is set 10.7 MHz below the frequency that is being monitored. As can be assumed from the previous sentence the IF frequency is 10.7 MHz. A SAW filter designed for the 903-918 MHz band allows for improved frequency rejection for out of band interferers.

A shield covers the entire RF section of the PC board to eliminate any signal leakage from the PLL to the outside. Surface mounted ferrite beads are used to isolate the inputs and outputs to prevent them from becoming part of the antenna system.

Power:
The unit uses a voltage regulator IC to maintain 3.3V internal from the 12-volt system on the vehicle.