- BATTERY

DC
Regulator

RF
TRANSCEIVER

RF (451.1875MHz)

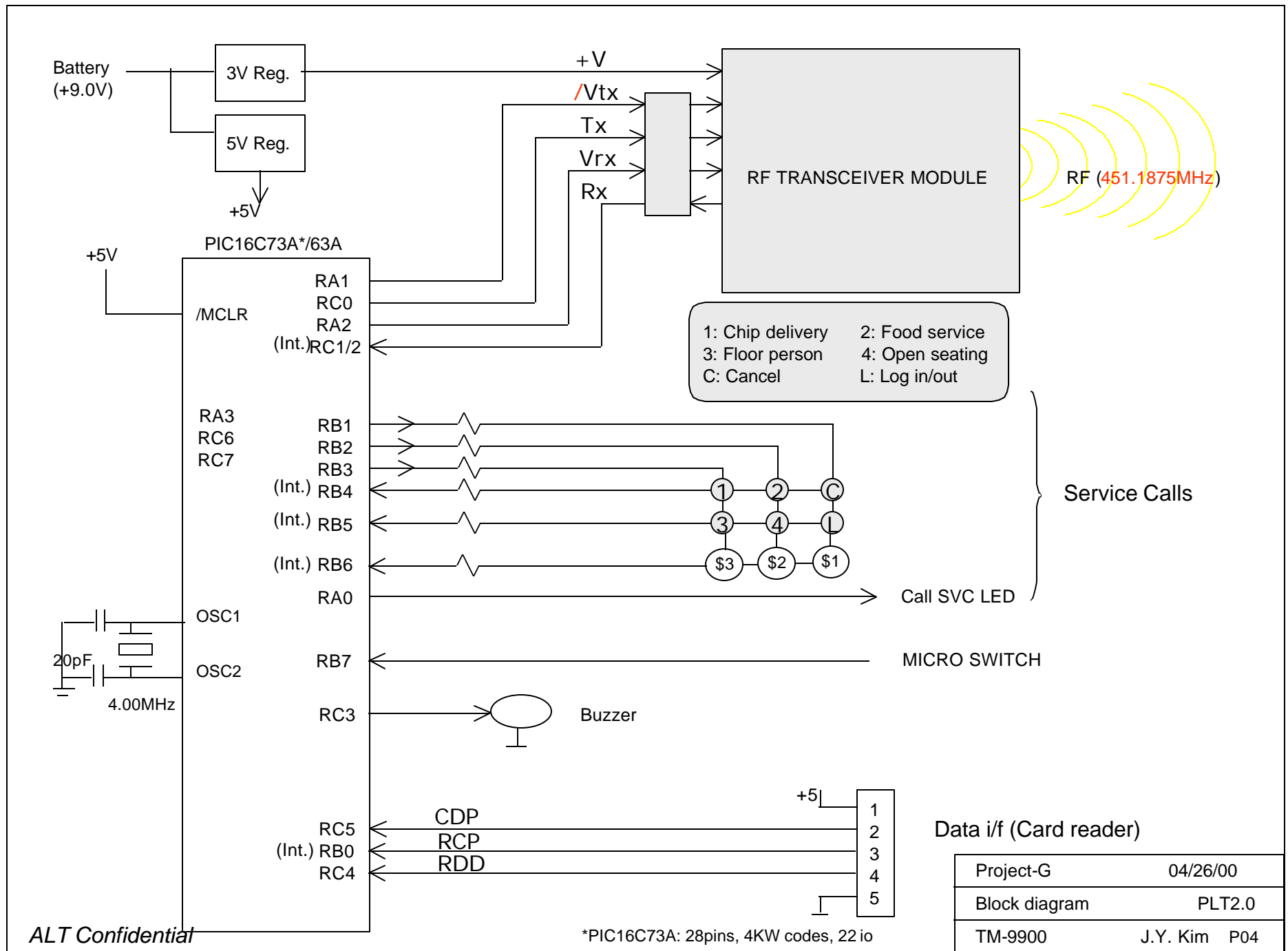- TO CHIP SENSOR

- TO CARD READER

CPU

- BUTTONS

- The battery type is selected to provide power to the device for six months.
- To save power, manually sliding magnetic card reader is used.
- A micro-switch is used to detect a chip drop.
- MAC protocol will be developed such that minimum power consumption is also considered.
- MAC will handle data collision.
- The CPU with A/D, I/O ports, RAM and ROM will be used.

Battery (+9.0V)

3V Reg.

5V Reg.

+5V

+V

/Vtx

Tx

Vrx

Rx

RF TRANSCEIVER MODULE

RF (451.1875MHz)

+5V

/MCLR

PIC16C73A*/63A

RA1
RC0
RA2
(Int.) RC1/2

1: Chip delivery   2: Food service
3: Floor person   4: Open seating
C: Cancel   L: Log in/out

RA3
RC6
RC7

RB1
RB2
RB3
(Int.) RB4
(Int.) RB5
(Int.) RB6
RA0

① ② C
③ ④ L
$3 $2 $1

Service Calls

Call SVC LED

20pF

OSC1

OSC2

4.00MHz

RB7

MICRO SWITCH

RC3

Buzzer

+5

RC5
(Int.) RB0
RC4

CDP
RCP
RDD

1
2
3
4
5

Data i/f (Card reader)

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*PIC16C73A: 28pins, 4KW codes, 22 io

Project-G	04/26/00
Block diagram	PLT2.0
TM-9900	J.Y. Kim P04

connector1 (CNT1)
pin 1 : GND
pin 2 : Tx Data (Tx)
pin 3 : Tx Power1 (Vtx1)
pin 4 : Tx Power2 (Vtx2)
pin 5 : Carrier Sense
pin 6 : Antenna (ANT)

Vtx   1.5 - 5.0V

connector2 (CNT2)
pin 12 : GND
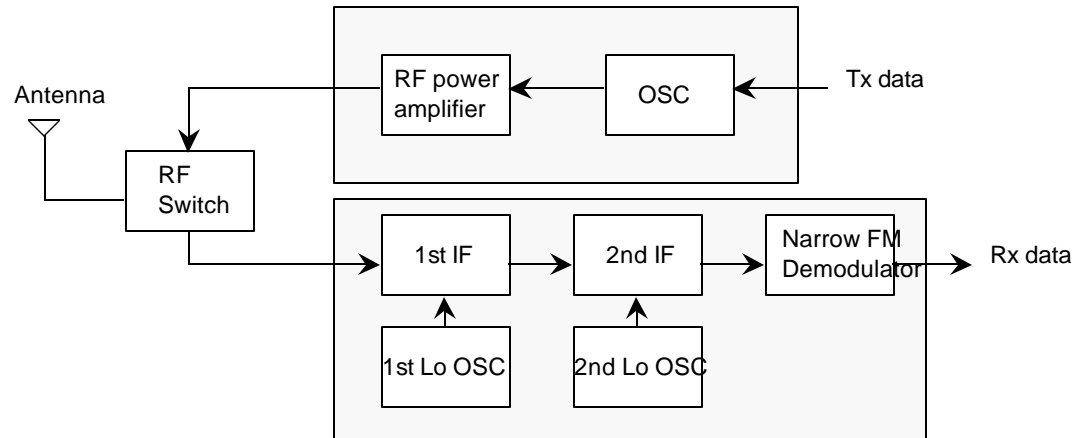pin 11 : Rx Power ctrl(BS)
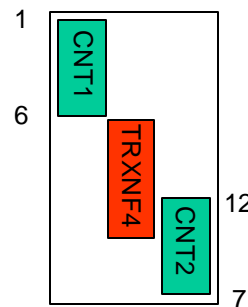pin 10 : Rx data (Rx)
pin 9 : NC (AF)
pin 8 : Rx Power (Vrx)
pin 7 : NC (AL)

Rx   open collector out
(10K pull-up).
Vrx   1.5 - 4.0V

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Antenna

RF Switch

RF power amplifier

OSC

Tx data

1st IF

2nd IF

Narrow FM Demodulator

Rx data

1st Lo OSC

2nd Lo OSC

RF transceiver

1

6

CNT1

TRXNF4

CNT2

12

7

Top view of
Automan RF module

Project-G	04/26/00
RF transceiver	PLT2.0
RF Module	J.Y. Kim P05

- GTMS Revenue
- GTMS Guest's Comp

- GTMS Service Call

PM

PM

Table A24 calls food service.
Table B30 calls a floorperson.
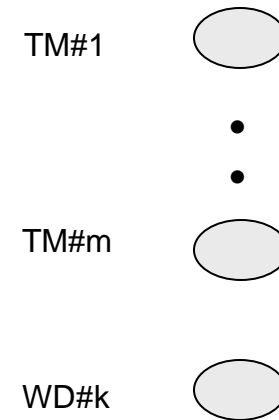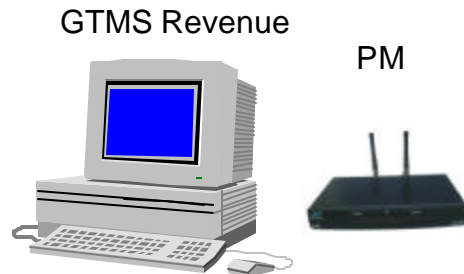Table A12 needs a new battery

TM#1

TM#m

WD#1

WD#k

• • • •

• • • •

The Table Module(TM)

The Wand(WD)

Project-G	04/26/00
Overall	PLT2.0
Protocols	J.Y. Kim P06

TM#1 ◯

•
•

TM#m ◯

WD#k ◯

GTMS Revenue

PM

- PC Module is a master and
  Table Modules are slaves.
- Collision may happen due to multiple
  TM's.
- CA (collision avoidance) is needed.
- TM sends a packet first, then TM waits for con-
  firm packet from the PM.
- If confirm packet doesn't arrive for predefined
  time, collision happened.
- GTMS Revenue PC s/w downloads TM & WD id table
  and a list of [appl], here this is {0x11, 0x12}

From TM to PM:

```
MAC format
[tm0]..[tm2][cmd][lng][d0]..[dn][chk]
   [tm0]..[tm2] 23 bits with b7 of tm0=0
   [cmd] 0x11 for TM, 0x12 for Wand
   [lng] length of application packet
```

PHY format
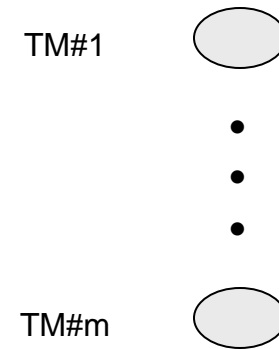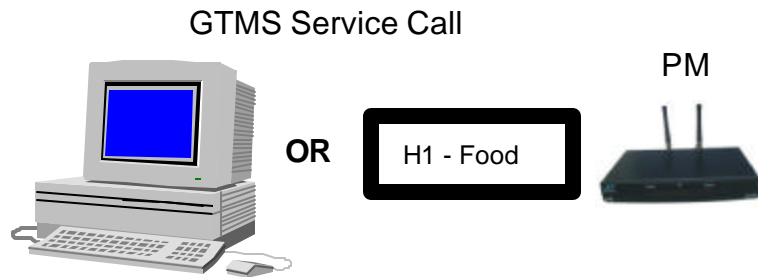<Preamble><SIF><MAC data>

From PM to TM:

MAC format
```
[tm0]..[tm2][cmd][0][chk]
```

PHY format
<Preamble><SIF><MAC data>

Preamble = 0011001100110001 = 0x3331

GTMS Service Call

OR H1 - Food PM

TM#1

TM#m

- PM receives call service information.
- PM responds by sending confirm packet.
- Collision may happen due to multiple
  TM's.
- CA (collision avoidance) is needed.
- TM sends a packet first, then TM waits for con-
  firm packet from the PM.
- If confirm packet doesn't arrive for predefined
  time, collision happened.
- GTMS Service Call PC s/w downloads TM id table
  and a list of [appl], here this is {0x12}
- PM supports 'Simple Display' mode where dummy
  terminal or LED display can be used.

From TM to PM:

```
MAC format
[tm0]..[tm2][cmd][1][data][chk]
   [tm0]..[tm2] 23 bits with b7 of tm0=0
   [cmd] 0x12 for GTMS Service Call
   [lng=1] length of application packet
```

PHY format
<Preamble><SIF><MAC data>
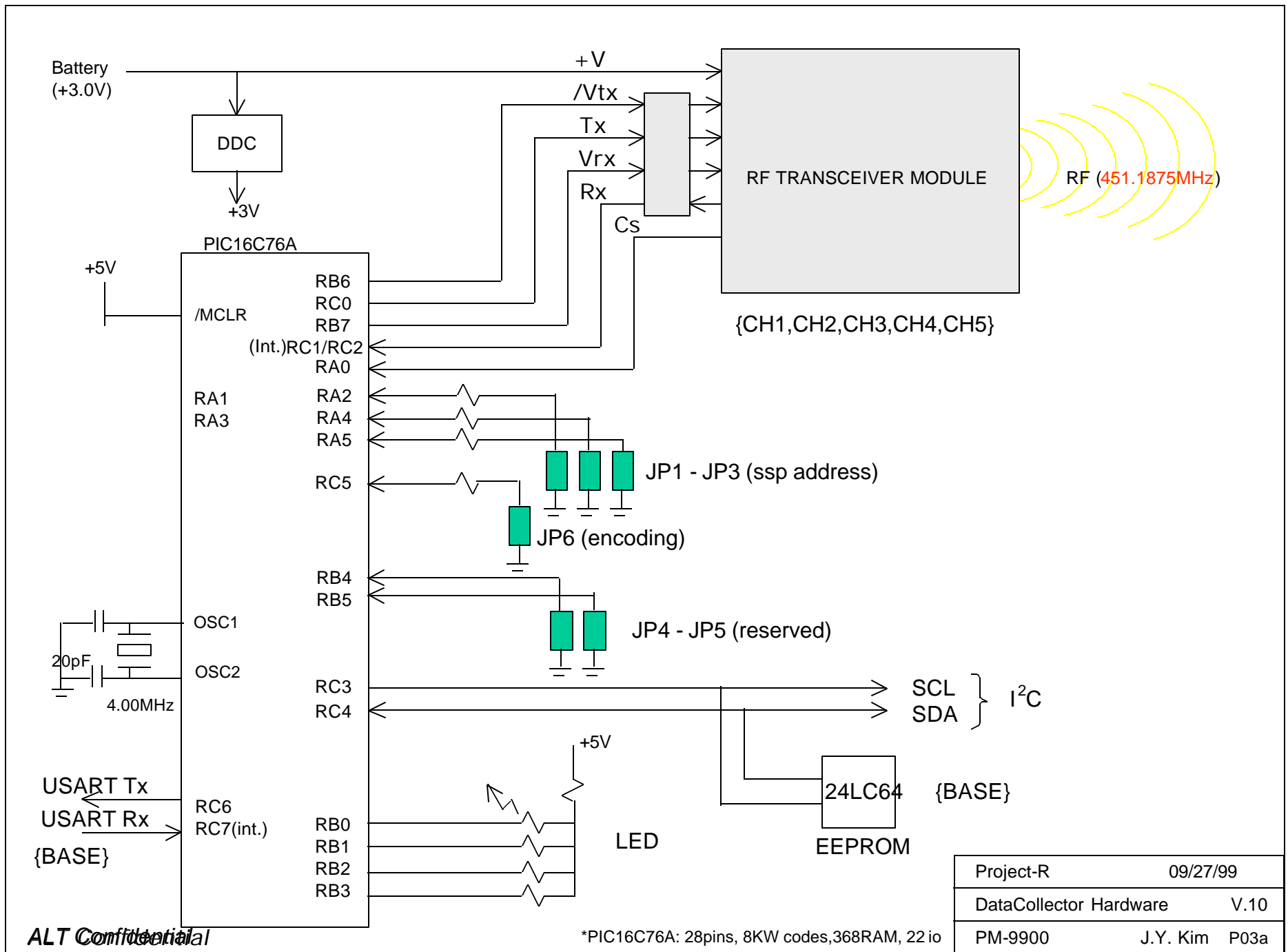
From PM to TM:

MAC format
```
[tm0]..[tm2][cmd][0x0][chk]
```

PHY format
<Preamble><SIF><MAC data>

DATA:
> 0x1 : Chip delivery
> 0x2 : Food service
> 0x4 : Change battery
> 0x8 : Open seating
> 0x10: Cancel
> 0x20 : Floor person call

Battery
(+3.0V)

DDC

+3V

+5V

PIC16C76A

/MCLR

RA1
RA3

20pF

4.00MHz

OSC1

OSC2

USART Tx
USART Rx
{BASE}

RC6
RC7(int.)

RB6
RC0
RB7
(Int.)RC1/RC2
RA0

RA2
RA4
RA5

RC5

RB4
RB5

RC3
RC4

RB0
RB1
RB2
RB3

+V
/Vtx
Tx
Vrx
Rx
Cs

RF TRANSCEIVER MODULE

RF (451.1875MHz)

{CH1,CH2,CH3,CH4,CH5}

JP1 - JP3 (ssp address)

JP6 (encoding)

JP4 - JP5 (reserved)

SCL
SDA
I^2C

+5V

LED

24LC64   {BASE}

EEPROM

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*PIC16C76A: 28pins, 8KW codes,368RAM, 22 io

Project-R	09/27/99
DataCollector Hardware	V.10
PM-9900	J.Y. Kim P03a