Transceiver Theory of Operation

The transceiver is a half-duplex type using a single-pole double throw switch to duplex the transmitter and the receiver in the time domain.

The transmitter architecture is a single non-inverting (low-side LO injection) image-rejection type. The first intermediate frequency VCO is frequency modulated with a spreading code at 1 Mcps and a peak frequency deviation of 250 kHz to produce a Minimum-Shift-Keyed Signal. The first intermediate frequency (IF) is 110.59 MHz. The local oscillator is tuned to produce a frequency-translated spectrum within the 902-928 MHz band using a non-inverting image-reject converter (Upper Side-Band). The signal is further amplified to the transmitter power level of 200 mW or 400 mW.

The receiver architecture is dual-conversion with the first conversion being an non-inverting (low-side LO injection) image-rejection type. The first intermediate frequency (IF) is 110.59 MHz. The second conversion is an inverting conversion (high-side LO injection) to a second IF of 13 MHz. The signal is amplified by a limiting amplifier to produce a constant output to the modulator, independent of input signal level. The frequency plan is spectrally inverting, but the transmitter is spectrally inverting as well to make the overall system non-inverting. Secondly, the data is differentially encoded (not shown in baseband block diagram) which makes the processing invariant to logic or frequency inversions. The signal is demodulated using a non-coherent frequency discrimination. The demodulated output is presented to a comparator to make bit decisions.

Baseband Theory of Operation

Baseband uses Siliconian SS1101C Spread Spectrum Chip. This chip is programmed using a PIC 16F877 microprocessor.

Direct sequence spreading is done in a half duplex mode using quaternary baseband modulation. SS1101C operates at 16 chips/bit or 32 bits/symbol resulting to a processing gain of 12dB. Transmitted DSS signal is at 850kHz. The receiver samples incoming baseband signal at two samples per PN chip. The samples are correlated with four PN sequences in 128-bit parallel correlators.