CH. 3 SD-5200 circuit

1. SD-5200 circuit

SD-5200 circuit is composed of RF and MPU. (RF determines communication quality and performance. MPU controls terminal performance.) RF is composed of TX and RX. TX is composed of synthesizer(Synthesizer generate TX frequency.), VCO, Data ALC(Automatic Level Control), Power Drive, final amplification and antenna switch.
RX is composed of front-end, mixer, local drive, crystal filter. IF amplifier, IF IC and Data conduct.
MPU is composed of EEPROM storing parameter of every kind and controls SD-5200.

2. Transmit

2.1 SYNTHESIZER

Synthesizer is consist of TCXO, PLL IC, Charge Pump, LPF and VCO. See illustration 2-1.
TCXO(U17) plays a key role to make usable frequency for terminal and use 14.4MHz(-30 ℃ ~ +60 ℃, 2.5ppm) of VX-23VA in JVC co. It uses resistance R65, R66 and VR13 externally for accuracy of frequency and modulation of low frequency data signal. When VR13 is turned to '+', voltage increases and frequency lowers. When VR13 is turned to '-', frequency rises.
If TX or RX frequency deviation occur, you can control with VR13.
Inside of PLL IC, there are 4 Divider Registers(CH1, CH2 Programmable Divider, Reference Divider and Option Control). Now, SD-2000N/5200 use only CH1 Programmable Divider

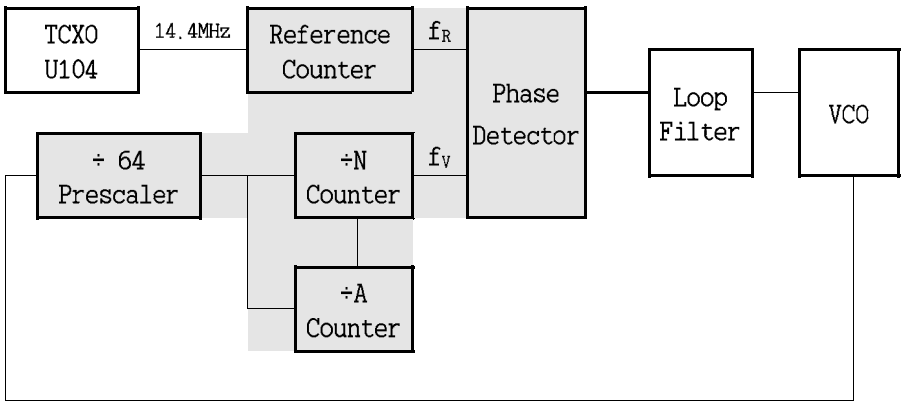

Illustration 2-1 Composition of Synthesizer

2.1.1 Cpmposition of Divider Register

Inside of PLL IC is consist of 4 Registers and is set with code.

CODE	ITEM
1 0	Number of dividers by CH1 Programmable divider(Fin1)
0 1	Number of dividers by CH2 Programmable divider(Fin2)
1 1	Number of dividers by reference divider(Xin)
0 0	Option control

1) Programmable divider

LSB MSB

A0	A1	A2	A3	A4	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	1	0

Calculation for generating 450.0125 MHz frequency, as below.

Set basic channel as 6.25 KHz.

450.0125 MHz ÷ 6.25 KHz = 72002

N and A Countor values are 72002 ÷ 64 = 1125. 03125

N value = 1125 → 465 hex

A value = 0.3125 → 0.3125 x 64 = 20 → 14 hex

LSB 4 1 5 6 4 MSB

0	0	1	0	1	1	0	1	0	0	1	1	0	0	0	1	0	1	0

2) Reference Divider

LSB MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	1	1

Calculation for basic frequency of 6.25 KHz with TCXO frequency

14.4 MHz ÷ 6.25 KHz = 2304 → 900 hex

LSB 0 0 9 MSB

0	0	0	0	0	0	0	0	1	0	0	1	1	1

3) Option Control

T	CP	CP1	CP2	SB1	CP1	CP2	SB2	SBR	LD1	LD2	SW	0	0

T : Test Mode (always "0")

CP : Charge pump output polarity

CP	Output Polarity
0	Normal
1	Reverse

Charge Pump Output Current

Control bit		Charge pump output current
CP1	CP2	
0	0	± 100 μA
0	1	± 200 μA
1	0	± 400 μA
0	0	± 800 μA

Lock detector output

Control bit				Lock detector output state
SB1	SB2	LD1	LD2	
0	0	0	0	L
		0	1	CH2 only detector
		1	0	CH1 only detector
		1	1	CH1, CH2
0	1	0	0	L
		0	1	H
		1	0	CH2 only detector
		1	1	CH1 only detector
1	0	0	0	L
		0	1	CH2 only detector
		1	0	H
		1	1	CH1 only detector
1	1	0	0	L
		0	1	H
		1	0	H
		1	1	H

Filter Switch Control

SW	Output
0	OFF
1	ON

On CH1, data for checking PLL Lock, as below.

0	0	1	1	0	0	0	1	0	1	0	0	0	0

2.2 VCO

VCO is circuit with Colpitts Oscillator, oscillates with control voltage by synthesizer and consist of TX and RX.

RX VCO is operating when RX VCO power Switch, TR(Q28) turns on. TX VCO is operating when TX VCO power Switch, TR(Q27) turns on. Control voltage of VCO change pulse voltage generated in Charge Pump of PLL IC to DC voltage as passing Low Pass Filter (C70, C71, C72, R69, R70).

Frequency range by control power, as table 3.1

table3.1) Control power and frequency

MODEL	PLL Control Power Range		frequency range	remark
SD-5200	TX	1.3 ~ 4.5 V	450 ~ 470 MHz	
	RX	1.3 ~ 4.5 V	428.6 ~448.6MHz	

Operation for transmit Mode is oscillated by Q21, C84, C85, C86, C87, C88, C89, C90, C91, VC12, D15, D16 and L26(They are consist of Colpitts Oscillator.).

R7 and C86 are circuit to remain 450 ~ 470 MHz frequency stable.

Varicap Diode determines frequency range for D15. D16 alters Data.

Operation for Receive Mode is oscillated by Q20, C73, C74, C75, C76, C77, C78, C79, D14 and L21.

Q22 and extra parts are buffers to amplify RF carrier which is oscillated by TX VCO and RX VCO, remain final output $0dB_m \pm 2dB$ and prevent amplified reverse power from output part.

2.3 Input Data ALC(Automatic Level Control)

User can use different input signal level.

Input Data ALC(Automatic Level Control) is designed to use every digital signal whose input signal range is 05V~0.6V.

Input signal data provided by D-sub Connector No. 4 pin amplify 47times as U16A and is provided to U16B Limiting circuit.

Output of U16B restricts every signal as 1.4V and provide to VCO and TCXO.

TCXO(U17) alters data signal(0~350Hz) with R63 and C64 and does not alter more than 350Hz with VCO. R60 is used as bypass, not using input Data ALC(Automatic Level Control)circuit.

2.4 POWER DRIVE

TX Drive(Q24, Q25) amplify RF power occurring VCO to meet final AMP input and restrict influence of reverse power.

First amp(Q24) operate as A level and amplify VCO output about 15dB. Second amp(Q25) amplify about 10dB to amplify final AMP(Q26) about 5W and to remain final output of C107 24~25dB. When P2.6 Port of MPU(U13) is high, Q24 and Q25 turn Q31 on and TR(Q30) provide power to TX drive.

This power provide power to ANT S/W and turn on D10 and D11 to emit TX carrier through antenna.

2.5 Final AMP and APC

Final TR(Q26) amplify RF Carrier as much as around 15dBm in the finial part of amplification. R96, VR14 and Q33 decide TX Power. Q33 and VR alter SD-5200 from 5W to 2W. When MPU(U13) becomes high, Q33 will be "ON" by dropping the gate power of TR(Q26).

When MPU(U13) P1.0 Port becomes High, Q33 will be ON, and alter power form 5W to 2W by dropping gate power of final TR(Q26) VR14 will control 2W RF power.

APC is designed to be operated when power is 2W

APC sense RF carrier from Final AMP and low supply power when RF Power is higher more than 2W. When RF Power is less than 2W, APC increase supply power of power Drive in order to make RF Power maintain 2W.

APC(Automatic Power Control) consist of RF Carrier sensor, amplification part that compare with standard voltage and schematic that switch the checked voltage.

RF Carrier sensor will be changed to DC voltage by using C116, D20, C134 in order to supply base voltage of Q36 in the amplification part.

The voltage which is suppled to Q36 is arrange low power(2W) with VR14, High Power(5W) control Q33(when Base is high).

Q36 in the amplification compare base voltage of Q36 which come from sensor part with base standard voltage which is supplied to Q36 and control Q35 which control RF power to be 2W by controling base voltage of Q30.

2.6 Antenna Switch

Antenna switch is consist of TX carrier, switching part and low pass filter. Switching part choose RF RX signal and low pass filter eliminate spurious at TX.

TX and RX switching part is operated by Pin Diode D10, D11.

At TX, when TX+8V provide power to L36, R98 and C113, D10 and D11 turn on, RF carrier flowing receiving direction is isolated and emit to antenna. At RX, when power providing to Pin diode of TX+8V turn off, D10 and D11 turn off and RF carrier is provided to receiving direction.

Low Pass Filter eliminate needless spurious and is consist of 2 steps.

3. Receive

3.1 FRONT-END

Front-end choose and amplify band width of RF signal. Front end is consist of filter and LNA(Low Noise Amp).

LNA is consist of two Transistor(Q10, Q11) and amplify about 20dB. Filter use two SAW Filter(F9. F10) to remain band width of 450~470MHz.

When P0.1 is high, TR Q4 turn on, Band Switching Diode(D18, D19) turn off, F9 turn off and F10 turn on.

Band Width of SAW Filter, as below.

SAW Filter	P0.1	frequency range
F9	Low	460~470 MHz
F10	High	450~460 MHz

3.2 Mixer

Mixer(Q12) mix received RF signal and local signal from synthesizer and then generate 21.4MHz, IF frequency. Volume of local signal is -4dBm at maximum and Conversion Gaini about 2dBm.

Medium frequency is determined, as below.

$F_{IF} = F_{RF} \pm F_{LOCAL}$

For preventing spurious. n-Channel Dual Gate MOS-FET, BF998 is used and spurious level of Local and RX RF is less than $-70dB_{m.}$

3.3 Crystal filter and IF AMP

Pass Band Width of 21.4MHz X-TAL filter(F11) is ±6KHz and can use 12.5KHz and 25KHz Spec of MCF : Ripple - 1dB, Insertion Loss - 3dB, MCF reduce about -35dB far from ±20KHz.

IF AMP(Q13) amplify X-TAL filter in 21.4MHz as 25dB. Consumption of voltage is less than 5mA.

3.4 IF IC

IF IC(U11) is consist of second Mixer, Ceramic Filter, 455KHz Resonator, Noise Squelch and SRRI.

Second Mixer generate 455KHz, mixing IF 21.4MHz and 2nd Local 20.945MHz(X10). This signal catch Ceramic Filter(F13, F14) with 12.5/25KHz swich(D12, D13) and determine adjacent channel fitting with 12.5/25KHz.
Channel selection in 12.5/25KHz is operated by MPU(U13) P0.4.
When P0.4 is high, 25KHz(F13) is selected. When P0.4 is low, 12.5KHz(F14) sis selected.
455KHz Resonator eliminate Carrier between received second IF Carrie and data signal and detect signal. In 25KHz, Q14 turn on and reduce 455KHz Resonator to remain data signal stable volume of 12.5/25KHz.
Noise Squelch signal identically detect noise squelch signal in 12.5/25KHz. RSSI signal alters to voltage according to signal strength inside of IF IC and provide D-SUB connector No. 8 pin..

3.5 Data Handling

Data handling part reverse or de-reverse signal at 2V with OP AMP(U12).
If users use TX data at 1/2 VCC voltage, user can use U12A No.1 pin(Invert Signal) or U12B No.7pin(Normal Signal).
After eliminating DC part, user can use as C48.

3.6 MPU(U13)

MPU operates after down loading RF status with D-SUB Connector No. 6 pin(S_I/O).
EEPROM(U14) stores Parameter of every kind and provide information.
Each port for MPU as following table

Port 0	기 능	Port 0	기 능
P0.0	S_CLOCK	P2.0	H/L_POW
P0.1	S-DATA/H/L_BAND	P2.1	PLL_LOCK
P0.2	S_I/O	P2.2	EEPORM DATA
P0.3	PTT	P2.3	PLL_CLOCK/ EEPROM CLOCK
P0.4	12.5/25KHz	P2.4	PLL_DATA
P0.5	RX_CON	P2.5	PLL_ENABLE
P0.6	TX_VCO	P2.6	TX_POW
P0.7	RX_VCO		

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