Re: Certification for DSA GIGA3 Transceiver
Model: GIGA3
FCC ID: PJY003
CANADA:

USER'S MANUAL INFORMATION

(PRELIMINARY)

The User's Manual is in preparation. The following material will be contained in the manual:

This device contains internal transceiver module FCC ID: PJY003

This device complies with Part 15 of the FCC Rules and with RSS-210 of Industry Canada. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

WARNING: Changes or modifications not expressively approved by the party responsible for compliance could void the user's authority to operate the equipment.

GIGA 3

RF Module

- Technical Handbook -

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for devices to Part 15 of FCC rules, which are designed to provide reasonable protection against such interference in a residential installation.
However, there is no guarantee that interference will not occur in a particular installation.

Modifying the equipment without DSA's written authorization may result in the equipment no longer complying with FCC requirements. In that event, your right to use the equipment may be limited by FCC regulations, and you may be required to correct any interference to radio or television communications at your own expense.
You can determine whether your equipment is causing interference by turning it off. If the interference stops, it was probably caused by the DSA equipment or one of its peripheral devices. If the equipment causes interference to radio or television reception, try to correct the interference by using one or more of the following measures:
• Turn the television or radio antenna until the interference stops.
• Move the equipment to one side or the other of the television or radio.
• Move the equipment farther away from the television or radio.
• Plug the equipment into an outlet that is on a different circuit from the television or radio. (That is, make certain the equipment and the television or radio are on circuits controlled by different circuit breakers or fuses.)
Modifications to this product not authorized by DSA could void the FCC approval and negate your authority to operate the product.

Inhalt

1 General Description

The GIGA3 HF transceiver board is designed to allow a full radio communication at 1Mbits/s provided by the WL800/WL600 integrated communication products produced by Mitel Semiconductor.

Its external interfaces are a 40 way AMP connector (EC1), and a Radial RF antenna connector (ANT).
These are all situated on the component side of the PCB.

The antenna connector is used in conjunction with the TXRX switch (IC6), and can be configured for transmitting, or receiving.

All input signals were buffered and the internal supply is regulated. The output power is independent from power supply and input signal level.

1.1 Features

Operation Range	2.403GHz to 2.481GHz
Supply Range	4.75V to 5.25V
Internal Supply	3V
Supply current	< 200mA
Number of Channels	78
Channels spacing	1MHz
Ouput IERP power	1mW

1.2 Device Description

WL600

The WL600 IC is a 48 pin LQFP package, and is basically an RF/IF circuit for use in digital radio. The receiver part contains a low noise amplifier, a down converter / quadrature

demodulator which generates the 43MHz IF, and an IF limiting strip which provides the IF gain and the RSSI output. The IC also contains a power amplifier driver stage with a ramp facility which controls the drive level to the external power amplifier.

WL800

The WL800 is a 32 pin TQFP packaged device, and contains a frequency synthesizer. The reference frequency is generated using a external 20MHz crystal which is divided by 20 to produce the 1MHz reference required. The divide ratios of the A and M counters are programmable to allow the external oscillator to be tuned over the required frequency range of 144 channels (1MHz spacing).

1.3 Circuit Operation

1.3.1 Transmit (TXD)

In transmit, the formatted (5V, 1Mbits/s) balanced data from the controller is applied to the TXD input. This feeds through a 20K Ohm resistor to the WL800 where it is buffered and fed to a current source. This current output (IDOUT) then goes through the modulation filter, and is applied to the resistor on the anode of the varactor (D1) which controls the frequency of the local oscillator.

This discrete local oscillator circuit is used to drive both the WL600 and the WL800, and is separated on board by a delta configures 6dB splitter. The oscillator is phase locked, and is tunable (IN TX) between 2.4GHz and 2.5GHz. A 1 MHz reference frequency used by the phase locked loop is generated using an internal divider (÷20), a 20MHz crystal and an on-chip oscillator maintaining circuit.

To correct for the shift in oscillator frequency due to the low frequency content of the data, an anti-modulation circuit is incorporated within the WL800. This circuit applies an opposing current into the PLL to cancel out the attempted correction.

The modulated signal drives the LO_IN port of the WL600, where it is amplified and used to produce the DRIVE output to the power amplifier. Ramping of this signal is performed

by the WL600. The PA switches on simultaneously with the output being ramped up, and switches off as the output is being ramped down.

This is achieved on the radio demonstration board by connecting the PA_ON signal to the driver circuit for the PA and the TXRX switch.

The discrete single stage power amplifier uses a Hewlett Packard MMIC device, and produces an output level of around 1 mW.

The signal is passed through a Murata Low pass filter to help reduce harmonic levels at the output of the radio, and is then fed through the NEC transmit/receive switch (IC6) and onto the antenna (ANT) via the TOKO filter (FILT2).

1.3.2 Receive(RXD)

In receive, the signal arrives at the antenna (ANT) and goes back through the TOKO filter and NEC TXRX switch. It is then fed into the RF_IN port of the WL600, the internal image reject mixer uses the local oscillator signal to produce the down converted 43MHz IF signal.

The local oscillator frequency must be set 43MHz lower than the received signal, and hence is tuned between 2.357GHz and 2.457GHz for receive. It should be noted that the synthesizer should be reprogrammed at the beginning of every TX cycle and every RX cycle. This should occur directly after TXRXB signal to the radio is switched.

Due to this necessary change in LO frequency, the TXRX time to valid data Hop times are specified as <200µs.

The differential signals (IF_OUT +/-) from the WL600 are amplified by a discrete amplifier, and then filtered using a Thomson 43MHz SAW filter, which is coupled via

matching networks to produce the correct filter response. The signals are then returned to the WL600 where it is amplified in the limiting log amplifier strip.

The differential IF signals are demodulated, fed through the demodulator filter and the returned to the WL600 where they are buffered, and used to produce the RXD_H and RXD_HB signals. These two signals drive inputs of voltage comparator, the MAX941 (IC7), whose output is the RXD signal (TTL compatible).

The Demodulator levels are set by a trimmer Quad tank circuit (Quad+/-) on the WL600.

The sensitivity of the GIGA3 board is typically better then –85dBm.

1.3.3 Control Signals

The level of all input control signals has be switched from +5V TTL to +3.3V LV TTL by the octal buffer, the MC74VHC541 (IC8).

There are several signals which need controlling on the board. These should be provided at the following levels. (VCC = 5V)

Logic low voltage = 0V (0.8V max)

Logic High Voltage = VCC (VCC-0.7 min)

TXRXB

This signal is used by the WL600. It controls whether the device is in transmit or receive.

Transmit Mode = Logic 1

Receive Mode = Logic 0

STDBY

This controls whether the board is in standby or active mode.

Standby Mode = Logic 0

Active Mode = Logic 1

PA -ON

This signal is used by the Wl600, and controls the ramping of the RF output to the power amplifier. This line also controls the logic the TXRX switch and the power amplifier.

Switch in TX / Ramped Output & PA ON = Logic 1

Switch in RX / Ramped Output & PA Off = Logic 0

SYNLOK

This signal is produced by the WL800 and gives an indication to the controller that the phase locked loop is locked, and that the oscillator is at the correct frequency. This prevents any transmissions occurring on illegal frequencies.

PLL Locked = 0V

PLL Unlocked = 2.2V

CCAB

This signal is produced by the WL600, and can be used by the controller to see if a channel is clear, or if there is a carrier present. The levels are set by the external components on the clamp set pin of the device.

Channel Clear = Logic 0

Carrier Present = Logic 1

SYSCLK

This is a 20MHz signal which is produced by the WL800 in conjunction with the crystal. The signal is buffered with a transistor TR6. Clock levels provided are approximately 280mV pk-pk, with improved drive levels of around 10mA.

CS-LOADB

This signal is used to enable the counters in the WL800. It is taken low at the start of a programming sequence, and should remain low for the period of the CS_DATA (8 serial bits).

Enable Counters = Logic 0

Reset Counters = Logic 1

CS-DATA

This is the serial 8 bits channel programming data, used to program the WL800 synthesizer. A table of the channel select data is included in Appendix B of this document.

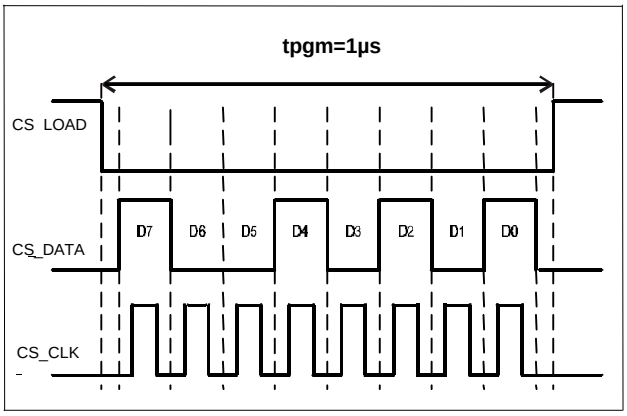
D7	D6	D5	D4	D3	D2	D1	D0

M Counter	A Counter

CS-CLK

This is the WL800 channel select clock, and it is used to clock in the 8 serial bits of the Channel select data. Each bit is clocked into the counter on the positive going edge of the clock pulses.

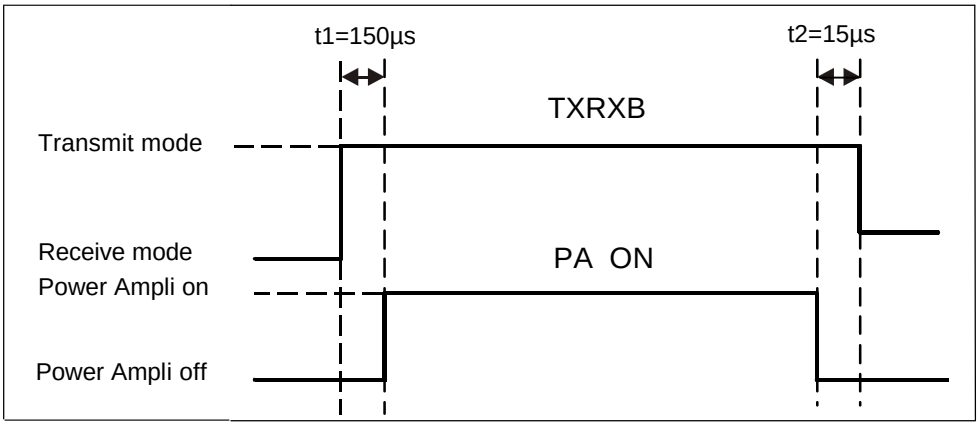
Programming Control Sequence



WL800 programming sequence: sequence

tpgm : the WL800's counter programming time.

Transmit Control Sequences



Transmit control sequence: sequence 2

t1 : PLL Locked period.

t2 : Ramp down period.

1.4 Installation Hints

The RF Module has to be used with a shielding housing. Only the approved Antenna has to be used.

1.5 Getting started:

Ensure that the logic levels to the board are as follows :

STDBYB = Low

PA_ON = Low

TXRXB = Low

Set board Logic levels as required :

Signal	Transmit	Receive
STDBYB	High	High
PA_ON	High	Low
TXRXB	High	Low

To switch between reception and emission mode, the sequences 1 and 2 should be respected.

At T=0 Switch TXRXB to Tx mode.
Reprogram synthesizer (emission canal).
T=150µs Switch PA_ON to logic 1 Start preamble (data).

At end of Data string,
Switch PA_ON to logic 0

After ramp down period (15µs),
Switch TXRXB to RX mode.
Reprogram synthesizer (shift 43MHz to the bottom).

2 Appendix A: 40 way Connector Pin Out

PIN	SIGNAL	DESCRIPTION
1,10,11,13,14,.. 16,18,19,20,23, 24,33.	GND	All pins connected to the Ground Plane
2,4,6	VCC	5V supply to 3V regulator
7	TXRXB	Transmit/Receive
9	RXD	Receive Data
12	PA_ON	Power Amplifier Control
25	SYSCLK	20MHz clock out
26	VOUT	3V regulator out
27	CCAB	Clear Channel Assessment
28	SYNLOK	PLL Lock Detect
29	TXD	Transmit Data
30	STDBY	Board Standby
31	RSSI	Received signal level
32	CS_LOADB	Channel Select Load
34	CS_DATA	Channel Select Data
35	CS_CLK	Channel Select Clock
40	CS_CLK	Pin not used
3,5,8,15,21,22,. 36,37,38,39	Not connected	

3 Appendix B: WL800 Programming Data

Freq MHz	M	A	d7-d0
2357	49	5	00000101
2358	49	6	00000110
2359	49	7	00000111
2360	49	8	00001000
2361	49	9	00001001
2362	49	10	00001010
2363	49	11	00001011
2364	49	12	00001100
2365	49	13	00001101
2366	49	14	00001110
2367	49	15	00001111
2368	49	16	00010000
2369	49	17	00010001
2370	49	18	00010010
2371	49	19	00010011
2372	49	20	00010100
2373	49	21	00010101
2374	49	22	00010110
2375	49	23	00010111
2376	49	24	00011000
2377	49	25	00011001
2378	49	26	00011010
2379	49	27	00011011
2380	49	28	00011100
2381	49	29	00011101
2382	49	30	00011110
2383	49	31	00011111
2384	49	32	00100000
2385	49	33	00100001
2386	49	34	00100010
2387	49	35	00100011
2388	49	36	00100011
2389	49	37	00100101
2390	49	38	00100110
2391	49	39	00100111
2392	49	40	00101000
2393	49	41	00101001
2394	49	42	00101010
2395	49	43	00101011
2396	49	44	00101100
2397	49	45	00101101
2398	49	46	00101110
2399	49	47	00101111
2400	49	48	00110000
2401	50	1	01000001
2402	50	2	01000010
2403	50	3	01000011
2404	50	4	01000100
2405	50	5	01000101
2406	50	6	01000110
2407	50	7	01000111
2408	50	8	01001000
2409	50	9	01001001
2410	50	10	01001010
2411	50	11	01001011
2412	50	12	01001100
2413	50	13	01001101
2414	50	14	01001110
2415	50	15	01001111
2416	50	16	01010000
2417	50	17	01010001
2418	50	18	01010010
2419	50	19	01010011
2420	50	20	01010100
2421	50	21	01010101

Freq MHz	M	A	d7-d0
2422	50	22	01010110
2423	50	23	01010111
2424	50	24	01011000
2425	50	25	01011001
2426	50	26	01011010
2427	50	27	01011011
2428	50	28	01011100
2429	50	29	01011101
2430	50	30	01011110
2431	50	31	01011111
2432	50	32	01100000
2433	50	33	01100001
2434	50	34	01100010
2435	50	35	01100011
2436	50	36	01100100
2437	50	37	01100101
2438	50	38	01100110
2439	50	39	01100111
2440	50	40	01101000
2441	50	41	01101001
2442	50	42	01101010
2443	50	43	01101011
2444	50	44	01101100
2445	50	45	01101101
2446	50	46	01101110
2447	50	47	01101111
2448	50	48	01110000
2449	51	1	10000001
2450	51	2	10000010
2451	51	3	10000011
2452	51	4	10000100
2453	51	5	10000101
2454	51	6	10000110
2455	51	7	10000111
2456	51	8	10001000
2457	51	9	10001001
2458	51	10	10001010
2459	51	11	10001011
2460	51	12	10001100
2461	51	13	10001101
2462	51	14	10001110
2463	51	15	10001111
2464	51	16	10010000
2465	51	17	10010001
2466	51	18	10010010
2467	51	19	10010011
2468	51	20	10010100
2469	51	21	10010101
2470	51	22	10010110
2471	51	23	10010111
2472	51	24	10011000
2473	51	25	10011001
2474	51	26	10011010
2475	51	27	10011011
2476	51	28	10011100
2477	51	29	10011101
2478	51	30	10011110
2479	51	31	10011111
2480	51	32	10100000
2481	51	33	10100001

4 Appendix C: WL800 Counters

Within the WL800 are 2 counters (A&M) and a prescaler (N). These are used together to generate a divider reference frequency which is used by the PLL to correctly control the frequency of the VCO.

The A-counter
This is a programmable counter which can be programmed for values of 1 to 64. However for our
purposes, 48 is the maximum used. The counter programming occupies 6 Data bits of the CS_DATA string, and hence the 8 Bit data Buffer.

The M counter
The M counter is also programmable, and can be programmed for values of 49 to 52.
Since this only requires 4 separate states, it is possible to use the remaining 2 data bits of the 8 Bit data Buffer.

State	Data
40	00
50	01
51	10
52	11

However, the M-counter requires 3 data Bits to operate correctly, and an internal M-Bit counter decoder converts the 2 data bits into the 3 counter bits.

The N Prescaler
The N prescaler has 2 modulus states (N) and (N+1) . The N prescaler will produce 1 pulse for every (N) or (N+1) pulses seen at its input. The prescaler modulus is used to facilitate a complete division of the incoming VCO signal, and prevent any remainder.

WL800
Channel Programming Sequence

1) CS_LOADB input is taken low.
2) The 8 programming data bits (Appendix B) are fed into the CS_DATA input.
3) Each data bit is clocked into the 8 Bit Data Buffer by the CS_CLK input.

4) The 6 A-counter bits are fed directly to the 9 Bit data store, whilst the 2 M-counter bits are fed into the M-Bit count decoder and converted into the 3 data bits required. These are then fed onto the inputs of the 9 Bit Data Store.
5) CS_LOADB input is taken high, which triggers the Pre-set Decoder and produces a pulse (RESET) which resets the A & M Counters.
6) A second pulse (DATA) is then generated, and the contents of the 9 Bit Data Store are transferred to the A & M counters.
7) The counters are now programmed for operation.

Counter Operation
Once the channel data is programmed, the operation is as follows:
The Prescaler modulus is controlled by the A-counter, and initially, when the A-counter is empty, divides by (N+1). As previously mentioned, this means that one counter pulse is generated for ever 49 pulses the prescaler sees.

These pulses are fed to both the A-counter and the M-counter, and both counters start to count down from their original programmed values.

Once the A-counter has finished its programmed count, the prescaler modulus changes, and now divides by (N).
This continues until the M counter is complete.
The A-counter sees the equivalent of(N+1)*A pulses. Whilst the M-counter sees N(M-A) pulses.
The total divider ratio = P = (N+1)A + N(M-A), **P = (NM+A)**.

The divider output should be a 1MHz signal which can be compared with the reference frequency of the PLL. Adjustments are then made as necessary.