N77-GL

Hardware User Guide

Issue 1.1 Date 2025-01-17

Notice

This document is specifically for N77-GL.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to N77-GL.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2023-04	Initial draft	Yin Xiaoliang
1.1	2023-10	Added the design note for the UART interface and optimized the recommended circuit for UART voltage level translation.	Yin Xiaoliang

Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

Related Documents

Neoway_N77-GL_Datasheet

Neoway_N77_AT_Command_Mannual

Neoway_N77_EVK_User_Guide

1 Safety Recommendations

Please read carefully and strictly adhere to the following safety recommendations to ensure that the product complies with national and environmental requirements, and to prevent threats to personal safety and potential damage to the product and workplace:

- Do not use in places where fire or explosion may occur.

  Using the product in locations with flammable gases, dust, or substances like propane, gasoline, or flammable aerosols may lead to explosions or fires.

- In areas where wireless communication is prohibited, please disable the wireless communication function.

  If the product is used in medical institutions or on airplanes, electromagnetic waves emitted by this product may interfere with surrounding equipment.

Follow the requirements below in design and use of the application for this module:

- Do not dismantle the product on your own, or you will lose after-sales warranty service.
- Design the product correctly according to the Hardware User Guide. Connect the product to a stable power voltage, and ensure wiring complies with safety and fire prevention requirements.
- Avoid touching the product pins to prevent static damage.
- Do not insert or remove USIM cards or mobile storage cards while the device is not turned off.

2 About N77-GL

This chapter introduces product overview, block diagram and basic features of N77-GL.

2.1 Product Overview

The N77-GL module is a 4G industrial-grade module with dimensions of (29.0±0.1) mm × (32.0±0.1) mm × (2.4±0.2) mm. It utilizes LGA packaging and features a total of 144 pins. The module provides connectivity on GSM/EDGE, WCDMA, FDD-LTE (Cat 4) and TDD-LTE (Cat 4) networks. It is suitable for the development of wireless meter reading terminals, industrial routers, and other IoT communication devices.

N77-GL possesses the following features:

- ARM Cortex-A7 processor, with CPU clock speed of up to 1.0 GHz, 64 KB L1 and 128 KB L2 cache.
- Supported network modes: LTE Cat. 4, WCDMA, GSM.
- Supported interfaces: USIM, USB, UART, SDIO, I2C, SPI, PCM, ADC.

Table 2-1 lists the frequency bands that N77-GL supports.

Table 2-1 Band information

Model	Region	Category	Band
N77-GL	Global	Cat4	FDD-LTE: B1, B2, B3, B4, B5, B7, B8, B12 B13, B17, B18, B19, B20, B26, B28, B66 TDD-LTE: B34, B38, B39, B40, B41 WCDMA: B1, B2, B5, B8 GSM/EDGE: 850/900/1800/1900 MHz

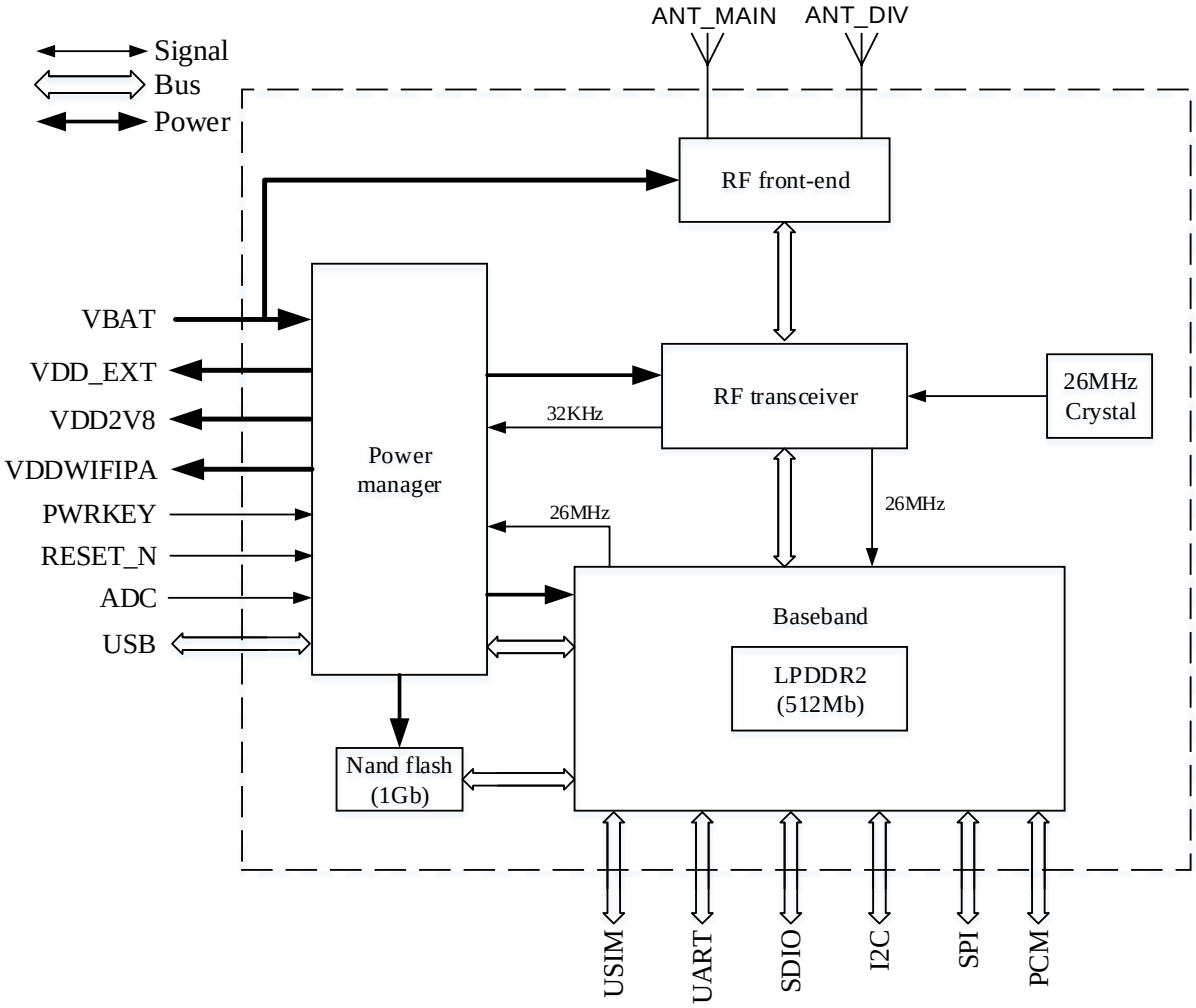
MiFi Base Version: Does not support GSM voice functionality, only supports GPRS/EDGE data functionality.
Module Base Version: Supports both GSM voice functionality and GPRS/EDGE data functionality.

2.2 Block Diagram

N77-GL includes the following functional units:

- Baseband chip
- 26 MHz crystal
- Power management
- Radio frequency unit
- Storage unit
- Digital interface (USIM, USB, UART, SDIO, I2C, SPI, PCM)
- Analog interface (ADC)

Figure 2-1 Block diagram



2.3 Basic Features

Features	Description
Physical features	• Dimensions: (29.0±0.1) mm × (32.0±0.1) mm × (2.4±0.2) mm • Package: 144-pin LGA • Weight: 5.4 g
Temperature ranges	Operating: -30°C to +75°C Extended: -40°C to +85°C Storage: -40°C to +90°C
Operating voltage (DC)	VBAT: 3.4 V to 4.2 V, typical value: 3.6 V
Operating current (DC)	Sleep mode[1]: TBD
	Standby mode[2]: TBD
	Operating mode[3] (LTE mode): ≤ 730 mA (Wi-Fi consumes around 55 mA)
Application processor	ARM Cortex-A7 processor, with CPU clock speed of up to 1.0 GHz, 64 KB L1 and 128 KB L2 cache.
Memory	RAM: 512 Mb ROM: 1 Gb
Band	See Table 2-1.
Wireless rate	GPRS: Max 85.6 kbps (DL)/Max 85.6 kbps (UL) EDGE: Max 236.8 kbps (DL)/Max 236.8 kbps (UL) WCDMA: HSDPA, Max 21 Mbps (DL)/ Max 5.76 Mbps (UL) LTE-FDD: Cat4, Max 150 Mbps (DL)/ Max 50 Mbps (UL) LTE-TDD: Cat4, Max 130 Mbps (DL)/ Max 30 Mbps (UL)
Transmit power	GPRS 850/900 MHz: 33 ± 2 dBm (Power Class 4) GPRS 1800/1900 MHz: 30 ± 2 dBm (Power Class 1) EDGE 850/900 MHz: 27 ± 3 dBm (Power Class E2) EDGE 1800/1900 MHz: 26 ± 3 dBm (Power Class E2) WCDMA: 24+1/-3 dBm (Power Class 3) LTE: 23 ± 2 dBm (Power Class 3)
Application Interfaces	2G/3G/4G main antenna, 4G diversity reception antenna The characteristic impedance of each antenna is 50 Ω.
	Three UART interfaces, one of which is a Debug interface.
	Two I2C interfaces, for master mode only.
	One SPI interface
	Two USIM interfaces, 1.8 V/3.0 V self-adaptive.
	One USB 2.0 interface
	Two SDIO 3.0 interfaces, with SDC1 used for WLAN and SDC2 used for

	SD cards.
	Two 11-bit ADC interfaces, with voltage detection ranging from 0.1 V to VBAT.
AT commands	3GPP Release 11 Neoway extended AT commands
SMS	PDU, TXT
Data	PPP, ECM
Protocols	TCP, UDP, FTP, HTTP*/HTTPS*
Certification approval	CCC*, CE*、FCC*

* means under development.

"Current in sleep mode[1)]": means the current drawn by the module when in sleep mode, a low power consumption state, in which its RF function is active while peripheral interfaces are disabled. If an incoming call or SMS is detected, the module will exit sleep mode. After the call or voice instant messaging ends, the module will re-enter the sleep mode.

"Current in standby mode[2)]": means the current drawn by the module in a normal operating mode, without processing any data service. This mode is typically used when the module is powered on but not actively engaged in data communication.

"Current in operating mode[3)]": means the current drawn by the module during active data communication. The operating mode represents the module actively processing and communicating data, necessitating higher power consumption. Only the currents in LTE mode are listed here. For details about currents under other network standards, see N77-GL current test report.

3 Reference Standard

N77-GL is designed by referring to the following standards:

- 3GPP TS 36.521-1 V9.10.0 User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Radio Resource Management (RRM) conformance testing
- 3GPP TS 21.111 V9.0.0 USIM and IC card requirements
- 3GPP TS 31.102 V9.19.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V9.12.2 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V9.9.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V9.0.1 Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

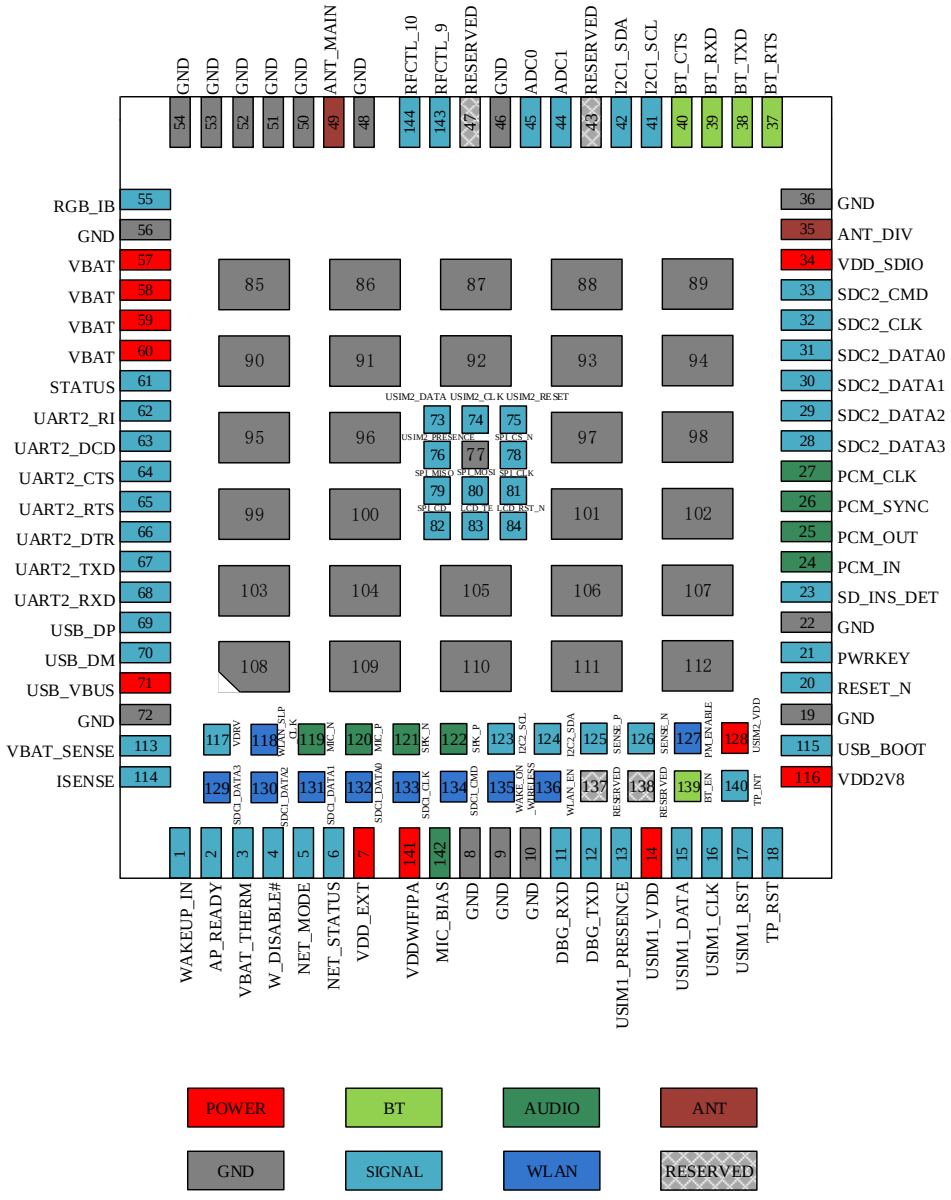
4 Pad Layout

N77-GL series modules are equipped with 144 pads, which are introduced in LGA package.

4.1 Pad Layout

Figure 4-1 shows the pad layout of N77-GL.

Figure 4-1 N77-GL pad layout (top view)



4.2 Pin Description

This chapter mainly introduces the N77-GL module pin types, interface power domains, and provide detailed explanations of the module pins.

Table 4-1 Pin type

Pin type	Pin description
AI	Analog input
AO	Analog output
AIO	Analog input/output
B	Digital Input/Output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output

Table 4-2 DC characteristics

Interface type	Power domain	Power domain description	Power domain features	Logic level characteristics	
USIM	P1	USIM interface	Either 1.85 V or 3.0 V SIM types are supported.	VIH = 0.7 x V_{DD_P1} ~ V_{DD_P1} V_{IL} = 0 V ~ 0.3 x V_{DD_P1}	V_{OH} = 0.9 x V_{DD_P1} ~ V_{DD_P1} V_{OL} = 0 V ~ 0.1 x V_{DD_P1}
SDIO	P2	SD card interface power domain	Either 1.85 V or 3.0 V SIM types are supported.	VIH = 0.7 x V_{DD_P1} ~ V_{DD_P1} V_{IL} = 0 V ~ 0.3 x V_{DD_P1}	V_{OH} = 0.9 x V_{DD_P1} ~ V_{DD_P1} V_{OL} = 0 V ~ 0.1 x V_{DD_P1}

GPIO	P3	Digital I/O power domain	1.85 V power output	VIH = 0.7 x V_{DD_P3} ~ V_{DD_P3} V_{IL} = 0 V ~ 0.3 x V_{DD_P3}	V_{OH} = 0.9 x V_{DD_P3} ~ V_{DD_P3} V_{OL} = 0 V ~ 0.1 x V_{DD_P3}

Table 4-3 Pin description

Signal	Pin SN	I/O	Function description	Level feature	Remarks
Power interfaces					
VBAT	57, 58, 59, 60	PI	Main power supply input	V_{min}=3.4 V V_{norm}=3.6 V V_{max}=4.2 V	The external power supply must ensure at least 2.5 A current.
VDD_EXT	7	PO	1.85 V power output	V_{norm}=1.85 V I_{max}=100 mA	Used only for pull-up or level shifting. Constantly on to supply power It is recommended to add ESD protection when using this pin.
VDDWIFIPA	141	PO	3.3 V power output	V_{norm}=3.3 V I_{max}=400 mA	Can be used to power an external WLAN module. If the 3.3 V power supply of the WLAN has a maximum load current greater than 400 mA, an external DC/DC or LDO is required. Leave this pin open if unused.
VDD2V8	116	PO	2.8 V power output	V_{norm}=2.8 V I_{max}=200 mA	Can be used to power an external SPI LCD. Leave this pin open if unused.
VDD_SDIO	34	PO	SDIO pull-up power supply	P2 I_{max}=50 mA	Only used for SDC2_CMD and SDC2_DATA pull-ups Leave this pin open if unused.
GND	8 - 10, 19, 22, 36, 46, 48, 50 - 54, 56, 72, 77, 85 - 112				Make sure all GND pins are grounded.
Control Interfaces					
RESET_N	20	DI	Module reset input	-	Pressing PWRKEY and RESET_N simultaneously for 2 seconds achieves a hard reset. This pin is internally pulled up to VBAT through a 20 kΩ resistor within the module.

PWRKEY	21	DI	Module on/off control	-	Effectively triggered by a low-level voltage or a low-level pulse, enabling control of the module's power on and off. This pin is internally pulled up to VBAT through a 20 kΩ resistor within the module.
USIM1 interface					
USIM1_VDD	14	PO	USIM1 power output	P1	I_{max}=50 mA
USIM1_DATA	15	B	USIM1 data	P1	Leave this pin open if unused.
USIM1_CLK	16	DO	USIM1 clock	P1	Leave this pin open if unused.
USIM1_RST	17	DO	USIM1 reset	P1	Leave this pin open if unused.
USIM1_PRESENCE	13	DI	USIM1 plug detection	P3	If the hot-swap function is not required, refer to Figure 5-19.
USIM2 interface					
USIM2_VDD	128	PO	USIM2 power output	P1	I_{max}=50 mA
USIM2_DATA	73	B	USIM2 data	P1	Leave this pin open if unused.
USIM2_CLK	74	DO	USIM2 clock	P1	Leave this pin open if unused.
USIM2_RST	75	DO	USIM2 reset	P1	Leave this pin open if unused.
USIM2_PRESENCE	76	DI	USIM2 plug detection	P3	If the hot-swap function is not required, refer to Figure 5-19.
USB interface					
USB_VBUS	71	AI	USB power supply detection input	V_{min}=4.5 V V_{norm}=5.0 V V_{max}=5.5 V	Also used as a charging voltage detection pin,
USB_DM	70	AIO	USB data -	-	USB 2.0 protocol standard for software downloading and data transfer; DM and DP differential routing, impedance control at
USB_DP	69	AIO	USB data +	-	

					90 Ω. Leave this open if unused.
UART2 interface *					
UART2_TXD	67	DO	UART data output	P3	Before use, please verify the configuration features corresponding to the software version. Leave this pin open if unused.
UART2_RXD	68	DI	UART data input	P3	
UART2_DTR	66	DI	Data terminal ready	P3	Leave this pin open if unused.
UART2_RTS	65	DO	UART request to send data	P3	
UART2_CTS	64	DI	UART clear to send data	P3	
UART2_DCD	63	DO	Data carrier detect	P3	
UART2_RI	62	DO	Ring indicator	P3	
Debug UART interface					
DBG_TXD	12	DO	UART data output	P3	During the module's normal startup, log information will be output from this pin; Before powering on, connect this pin with a 1kΩ resistor pulled down to GND to enter USB download mode.
DBG_RXD	11	DI	UART data input	P3	After the module has successfully booted up, this pin is exclusively used for debug purposes.
WLAN interface					
SDC1_CMD	134	B	SDIO command	P3	Leave this pin open if unused.
SDC1_CLK	133	DO	SDIO clock	P3	It is recommended to reserve an RC near the module to prevent EMI. Leave this pin open if unused.

SDC1_DATA0	132	B	SDIO bus data 0	P3	Leave this pin open if unused.
SDC1_DATA1	131	B	SDIO bus data 1	P3	Leave this pin open if unused.
SDC1_DATA2	130	B	SDIO bus data 2	P3	Leave this pin open if unused.
SDC1_DATA3	129	B	SDIO bus data 3	P3	Leave this pin open if unused.
WAKE_ON_WIRELESS	135	DI	Wake up the module by WLAN	P3	Leave this pin open if unused.
WLAN_SLP_CLK	118	DO	WLAN sleep clock	P3	The clock frequency is 32.768 kHz. Leave this pin open if unused.
WLAN_EN	136	DO	WLAN enable	P3	Active low. Leave this pin open if unused.
PM_ENABLE	127	DO	Control of the external power supply for WLAN	P3	Active low. Leave this pin open if unused.
BT interface					
BT_TXD	38	DO	Bluetooth serial interface data output	P3	BT_UART supports hardware flow control, used for connecting external Bluetooth chips or other external devices. Leave this pin open if unused.
BT_RXD	39	DI	Bluetooth serial interface data input	P3	
BT_CTS	40	DI	UART clear to send Data	P3	
BT_RTS	37	DO	UART request to send Data	P3	
BT_EN	139	DO	Bluetooth enable	P3	Leave this pin open if unused.

SD card interface*					
VDD_SDIO	34	PO	SDIO pull-up power supply	P2 I_{max}=50 mA	Only used for SDC2_CMD and SDC2_DATA pull-ups Leave this pin open if unused.
SDC2_DATA0	31	B	SD card data 0	P2	50 Ω single-terminal impedance control Leave this pin open if unused.
SDC2_DATA1	30	B	SD card data 1	P2	
SDC2_DATA2	29	B	SD card data 2	P2	
SDC2_DATA3	28	B	SD card data 3	P2	
SDC2_CLK	32	DO	SD card clock	P2	
SDC2_CMD	33	B	SD card command	P2	
SD_INS_DET	23	DI	SD card plug detection	P3	If the hot swap function is not used, please refer to the section 5.3.4 SD for handling method details of this pin.
PCM interface					
PCM_IN	24	DI	PCM data input	P3	Leave these pins open if unused.
PCM_OUT	25	DO	PCM data output	P3	
PCM_SYNC	26	B	PCM data frame synchronization	P3	
PCM_CLK	27	DO	PCM clock	P3	
I2C interface					
I2C1_SDA	42	B	I2C data	P3	Only used for external TP Leave these pins open if unused.
I2C1_SCL	41	DO	I2C clock	P3	
I2C2_SDA	124	B	I2C data	P3	Leave these pins open if unused.
I2C2_SCL	123	DO	I2C clock	P3	

SPI LCD interface					
SPI_CLK	81	DO	Clock signal	P3	Only used for external SPI LCD or other peripherals. Leave these pins open if unused.
SPI_MISO	79	DI	Output of slave device, input of master device	P3	
SPI_MOSI	80	DO	Input of slave device, output of master device	P3	
SPI_CS_N	78	DO	Chip selection signal of slave device	P3	
SPI_CD	82	DO	Data/command selection	P3	
LCD_RST_N	84	DO	Reset signal	P3	Leave these pins open if unused.
LCD_TE	83	DO	Frame sync	P3	
TP interface					
I2C1_SDA	42	B	I2C data	P3	Leave these pins open if unused.
I2C1_SCL	41	DO	I2C clock	P3	
TP_INT	140	DI	TP interrupt	P3	
TP_RST	18	DO	TP reset	P3	Active low Leave this pin open if unused.
RGB interface					
RGB_IB	55	AI	LED negative control	-	Connect it to LED negative With a current up to 218 mA

Audio interfaces*					
MIC_P	120	AI	MIC input (+)	-	Leave these pins open if unused.
MIC_N	119	AI	MIC input (-)	-	
MIC_BIAS	142	PO	MIC bias voltage	V_{min}=2.2 V V_{norm}=2.5 V V_{max}=3.0 V	
SPK_P	122	AO	Speaker output (+)	-	
SPK_N	121	AO	Speaker output (-)	-	
Battery charging and management interfaces*					
VBAT_THERM	3	AI	Battery temperature detection	-	10 k NTC thermistor is supported by default. Connect this pin to an external 10 kΩ resistor if not used.
SENSE_N	126	AI	Battery power detection negative	-	Ground the pin if not used.
SENSE_P	125	AI	Battery power detection positive	-	
VBAT_SENSE	113	AI	Battery voltage detection	-	Cannot be left floating, must connect to VBAT to power on. Maximum input voltage is 4.5V.
ISENSE	114	AI	Charging current detection	-	Leave this pin open if unused.
VDRV	117	AO	Charging drive control	-	Leave this pin open if unused.
USB_VBUS	71	AI	Charging voltage detection	V_{min}=4.5 V V_{norm}=5.0 V V_{max}=5.5 V	Also can be USB supply detection input.

ADC interface					
ADC0	45	AI	Generic analog-to-digital signal	-	11-bit resolution Detectable voltage range from 0.1 V to VBAT. Leave this pin open if unused.
ADC1	44	AI	Generic analog-to-digital signal	-	
Antenna interfaces					
ANT_MAIN	49	AIO	Main antenna	-	50 Ω impedance characteristic.
ANT_DIV	35	AIO	Diversity antenna	-	50 Ω impedance characteristic.
Other functional interfaces					
WAKEUP_IN*	1	DI	Sleep mode control	P3	It controls sleep mode of the module. Leave this pin open if unused.
W_DISABLE#	4	DI	Flight mode control	P3	Active low. Leave this pin open if unused.
AP_READY	2	DI	Sleep status detection	P3	Leave this pin open if unused.
STATUS	61	OD	Working status indication	-	Connecting an external pull-up resistor is required. Leave this pin open if unused.
NET_MODE	5	DO	Network registration mode indication	P3	Leave this pin open if unused.
NET_STATUS	6	DO	Network operation status indication	P3	
USB_BOOT	115	DI	Forcible download mode	P3	Before the module is powered on, pulling USB_BOOT down to ground will enable it to enter download mode.
RFCTL_9	143	DO	RF output control	P3	Antenna tuning control
RFCTL_10	144	DO	RF output control	P3	

Reserved		
RESERVED	43, 47, 137, 138	Reserved pins. Leave these pins open if unused.

5 Application Interfaces

N77-GL encompasses a versatile suite of interfaces, designed to cater to a wide spectrum of application scenarios. Ranging from control and communications, to peripherals and other functions, these interfaces offer comprehensive solutions tailored to specific needs.

This chapter describes how to design each interface and provides reference designs and guidelines. Please adhere to the guidelines detailed in this chapter, considering aspects such as trace width, component placement, and impedance control to implement best practices in circuit design to ensure optimal performance and reliability.

5.1 Power Interfaces

The power interfaces play a pivotal role in application design, with both the schematic design and PCB layout serving as critical components. Their configuration directly impacts the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

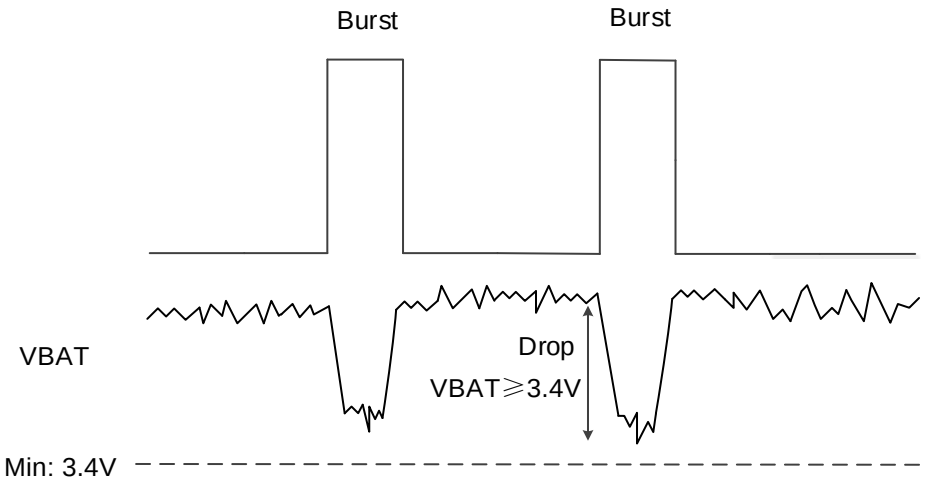
5.1.1 VBAT

The power supply design encompasses two key facets: schematic design and PCB layout. These are integral in sustaining the optimal functionality and safety of the module.

Schematic Design of Power Supply

In GSM/GPRS mode, RF data is transmitted in burst mode that generates voltage drops on the power supply. Furthermore, this results in a 217 Hz TDD noise through the power and the transient peak current is 2.5 A. Therefore, it is necessary to ensure that the power supply has adequate driving capacity to handle these peak currents, the power supply trace width is sufficient to reduce impedance, and there are capacitors with large capacitance to improve the ability to maintain current flow and to stabilize voltage during peak current demands.

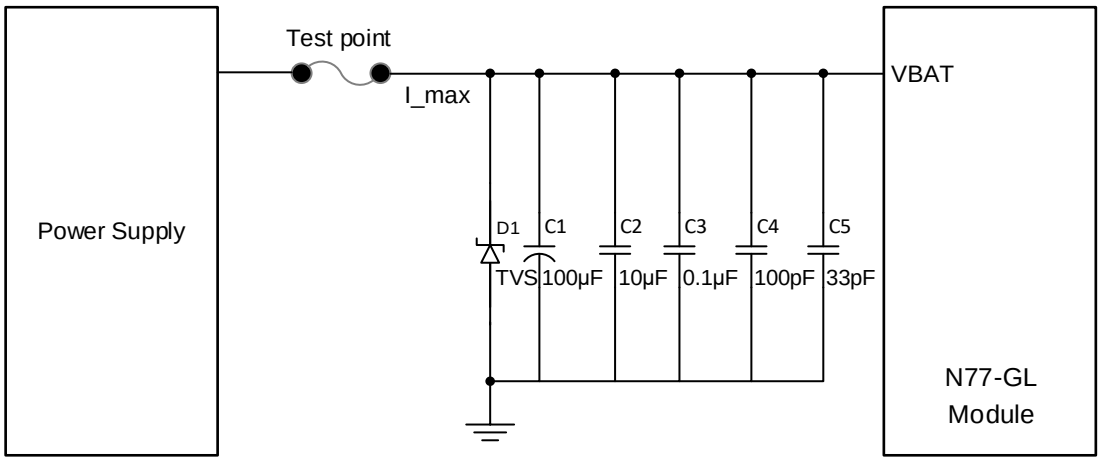
Figure 5-1 Voltage drop of the power supply.



Avoid Diode Voltage Drop: Never use a diode to bridge a voltage drop between a higher input and the module power supply, as its forward voltage drop characteristics can be leaded to instability or damage. The forward voltage drop Vf of diode has two characteristics: one is that it increases with the increase of the forward current. the other is that it increases significantly at a low temperature. The forward voltage drop V_f of the diode has two characteristics: one is that it increases with the increase of forward current; the other is that it increases significantly at a low temperature. Note that, if there is an instantaneous high current, the above characteristics will lead to unstable operating voltage of the module, and even damage the module.

Design Recommendations for 3.4 V - 4.2 V Power Input:

Figure 5-2 Recommended design of the power supply circuit 2



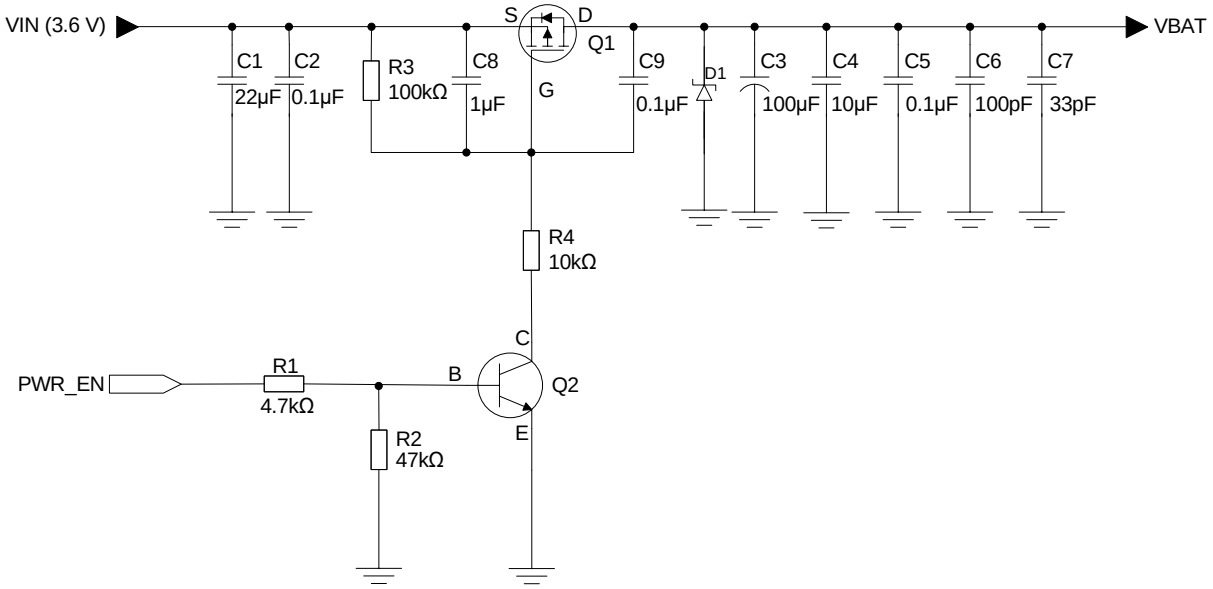
- The maximum input voltage of the module power supply is 4.2 V, and the typical value is 3.6 V. For VBAT, the recommended PCB trace width is 2.5 mm or above.
- In order to get a stable power source, it is recommended to select a TVS diode with suggested low reverse voltage (V_{RWM} = 4.5 V) and peak power (Ppp = 2800 W (tp = 8/20 us)) at D1. Keep

the TVS diode close to the power input interface to suppress the surge before it enters back-end circuits to prevent the back-end component and prevent damage.

- Use a large bypass tantalum capacitor (220 μF or 100 μF) or an aluminum capacitor (470 μF or 1000 μF) at C1 to decrease voltage drops during bursts. Its maximum safe operating voltage should be larger than 2 times the voltage of the power supply.
- Place low-ESR bypass capacitors (C2, C3, C4, C5) close to the module pins to filter out high-frequency jamming from the power supply.

If it is necessary to control the power supply, the following circuit design is recommended:

Figure 5-3 Recommended design of the power supply circuit 2



- Utilize an enhanced p-MOSFET at Q1, of which the safe operating voltage is at least 12 V (V_{dss}=-12 V) and drain current is at least 3.5 A ($I_{D(MAX)}$=-3.5 A) and Rds is low ($R_{ds(on)}$ =108 mΩ).
- Select a common NPN tripolar transistor at Q2. Reserve enough tolerances for R1 and R2, ensuring that R2 is at least 10 times greater than R1, as the break-over voltage on the transistor's base increases at low temperatures.
- C8 and C9 are two capacitors used to adjust the on and off times for the MOSFET. Please adjust their capacitance based on the testing results and the actual MOSFET specifications.

PCB Design Guidelines

A low ESR capacitor must be placed at the output side of the power supply to suppress the peak current. Add TVS diodes at the input of the power supply to suppress voltage spikes and protect back-end components.

Several key points in power supply design are summarized below:

- The TVS diode can absorb instantaneous high-power pulses and withstand instantaneous pulse current peaks up to tens or even hundreds of amperes. The clamp response time is extremely short. Keep the TVS diode as close as possible to the power input to ensure that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB wires.
- Place bypass capacitors as close as possible to the power supply interface of the module to filter out high-frequency noise signals in the power supply.
- For the main power circuit of the module, ensure that the PCB trace is wide enough that 2.5 A current can be safely passed, with no significant loop voltage drop. Keep PCB trace width be at least 2.5 mm and ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make power traces short and wide.

5.1.2 Power Output

The N77-GL module provides multiple power outputs, which can be used for I/O pin pull-up power, voltage level translation, and power supply for peripheral screens, WLAN, and other circuits. When applied, it is recommended to parallel 33 pF and 10 pF capacitors, which can effectively remove high-frequency interference.

Table 5-1 Power output description

Signal	Default voltage (V)	drive current (mA)	Standby	Remarks
VDD_EXT	1.85	100	Always on	Used only for pull-up or level shifting. Constantly on to supply power
VDD2V8	2.8	200	Always on	Power supply interface for SPI LCD or other peripherals. When used, an external bypass capacitor of 1.0 μF to 2.2 μF needs to be added. It is always powered on. Leave this pin open if unused.
VDDWIFIPA	3.3	400	-	Can be used to power an external WLAN module. If the 3.3V power supply of the WLAN has a maximum load current greater than 400mA, an external DC/DC or LDO is required. Add a bypass capacitor (1.0 μF- 2.2 μF) externally when using this pin. Leave this pin open if unused.
VDD_SDIO	3.0	50	-	Only used for SDC2_CMD and SDC2_DATA pull-ups. Leave this pin open if unused.

USIM1_VDD	1.8/3.0	50	-	USIM1 power output
USIM2_VDD	1.8/3.0	50	-	USIM2 power output

The VDD_EXT and VDD2V8 power sources are always on and cannot be turned off even in sleep mode. Connecting the module to an external circuit will increase its power consumption in sleep module. It is recommended to use VDD_EXT only for I/O pin pull-ups or interface level conversion, and not for other purposes. When using, it is advisable to reserve ESD protection. VDDWIFIPA needs software configuration to be activated. If needed, please verify the software version or consult with Neoway FAEs.

5.2 Control Interfaces

Signal	Pin SN	I/O	Function description	Remarks
RESET_N	20	DI	Module reset input	Pulling both PWRKEY and RESET_N low for 2 seconds can hard reset the module. This pin is internally pulled up to VBAT in the module through a 20 kΩ resistor.
PWRKEY	21	DI	Module on/off control	A low-level voltage or low-level pulse is effective for triggering the control of the module's power on and off. This pin is internally pulled up to VBAT in the module through a 20 kΩ resistor.

5.2.1 Module Power-on

Ensure that the VBAT voltage is stable before controlling PWRKEY. It is recommended to initiate the PWRKEY control operation 100 ms after the VBAT voltage has risen to the supply level, such as 3.6 V.

Table 5-2 Power-on description

Power-on trigger method	Supported or not	Power-off method	Notice
Button	Supported	Press the power-on key for no less than 3s and then release it.	**For Safety**: Do not disconnect the power supply when the module is on; flash memory

Pulse	Supported	Pulling the PWRKEY to a low-level voltage for ≥3s and then releasing it will power off the module.	may be damaged.
Auto power-on	Supported	Use the AT command to power off, followed by disconnecting power to the module.	If an automatic startup upon power-up is integrated into the design, the module will not be capable of being powered off using the PWRKEY. Additionally, if an AT command is employed to shut down the module while the system retains its power supply, the module will undergo a restart sequence following the shutdown.

Power-on Controlled by PWRKEY

In power-off state, applying a low-level pulse signal to the PWRKEY pin for a duration greater than 2.5s can power on the module.

Figure 5-4 Reference design for push-button startup

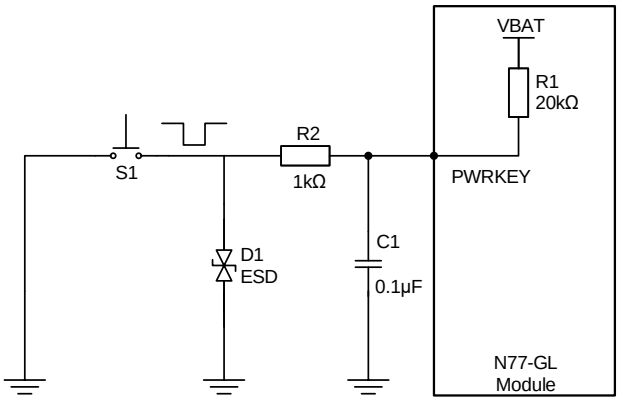
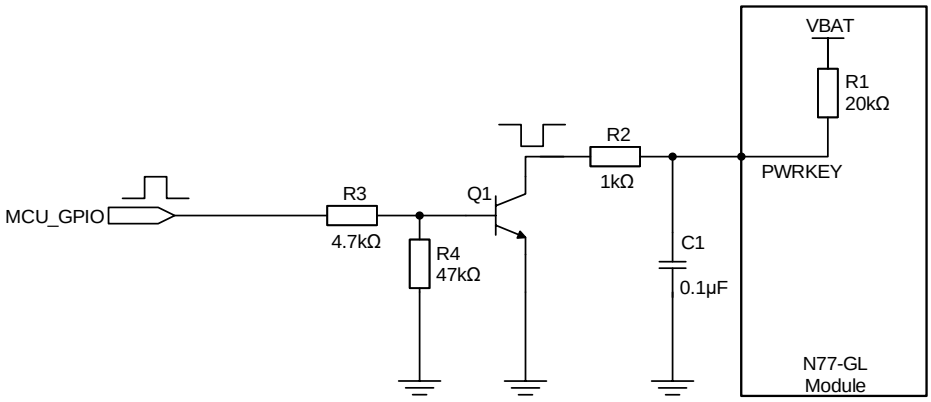


Figure 5-5 Reference design for MCU-controlled startup

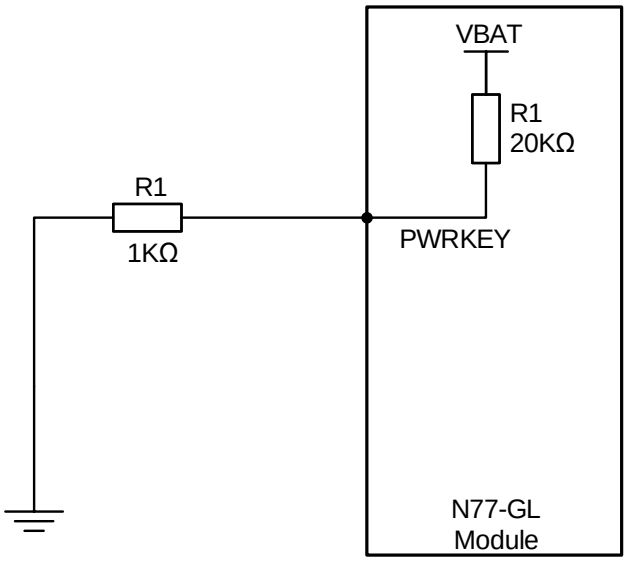


Automatic start once powered up

If you employ an automatic power-on method for the module, shutting down using the PWRKEY or AT commands will not be possible; the only option for shutting down will be to disconnect the power supply.

PWRKEY is a low-level power-on pin. By pulling the PWRKEY pin down to GND, the module powers on automatically. The following figure shows the reference design of startup controlled by the PWRKEY pin:

Figure 5-6 Reference design of automatic startup once powered up



Schematic Design Guidelines

- The PWRKEY pin is internally pulled up to VBAT through a 20 kΩ resistor. The external pull-down resistor should not be excessively high (a recommended resistance value is 1 kΩ), otherwise the PWRKEY will be continuously pulled high, preventing the module from powering on.

Power-on Process

After VBAT is powered on, inputting a low-level pulse to the PWRKEY pin for more than 2.5s and less than 3s can trigger the module to power on. It is recommended that the low-level duration is longer than 2.5s.

Do not perform other operations on the module until it is initialized completely. If the module is powered on but the initialization process has not been completed, the states of each pin are uncertain. For the power-on timing sequence of the module, see the diagram below.

Figure 5-7 Power-on timing

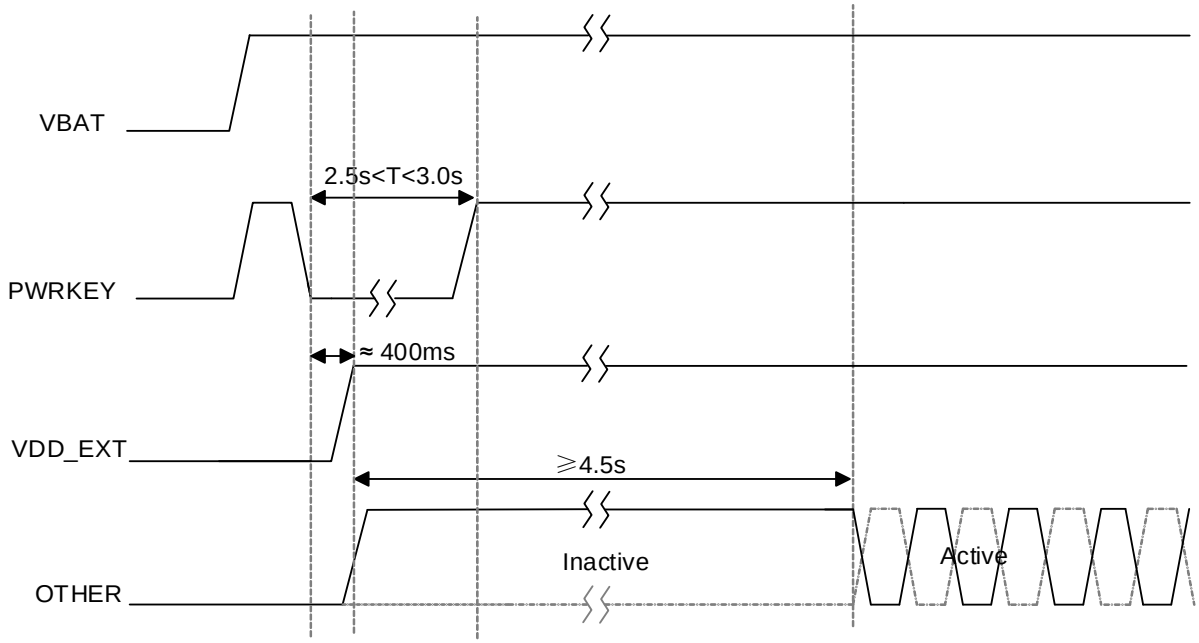
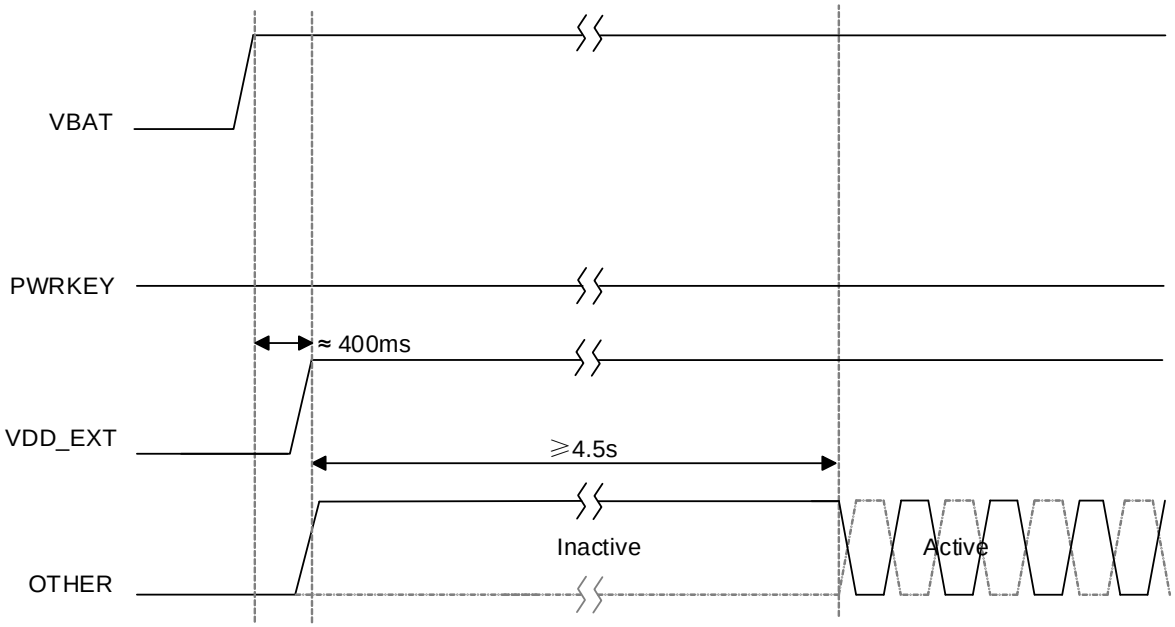


Figure 5-8 PWRKEY automatic power-on timing



5.2.2 Module Power-off

When the module is in normal startup state, inputting negative pulses for more than 3s to PWRKEY can shut down the module. Please refer to Figure 5-4 and Figure 5-5 for circuit design.

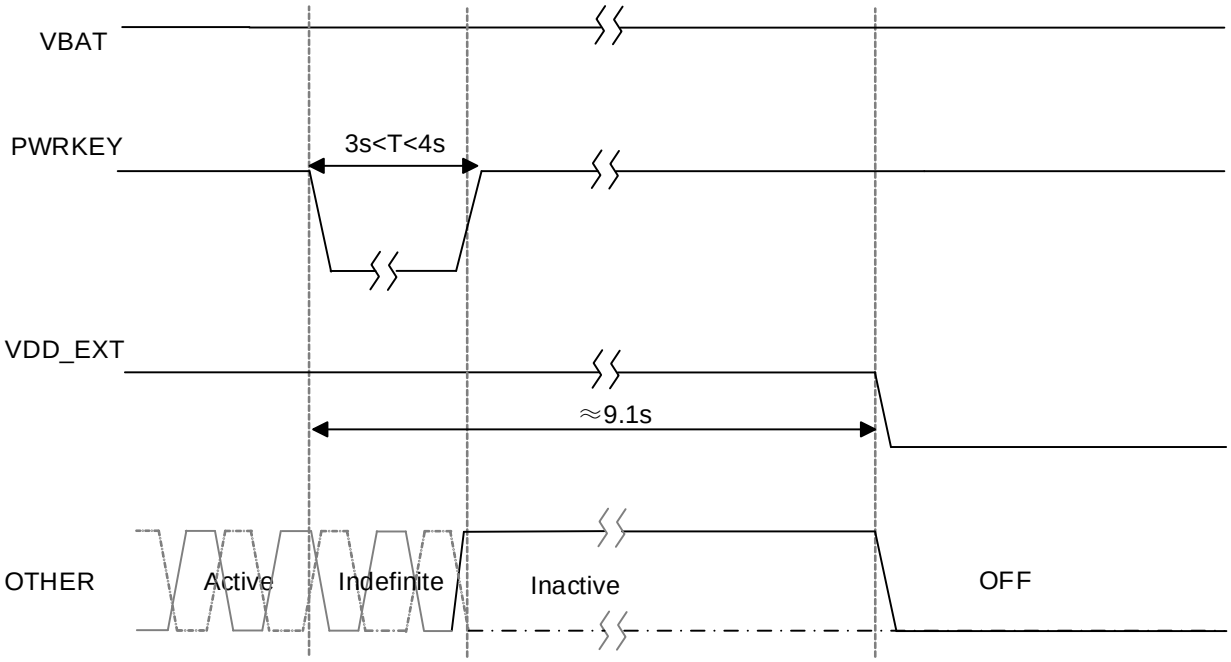
Power-off Process

Two methods are available to turn off the module: hardware shutdown using PWRKEY_N pin and software shutdown.

PWRKEY is used to hardware power off the module. Inputting negative pulses at PWRKEY for more than 3 seconds will switch off the module when it is in power-on mode. For details, see *Neoway_N77_AT_Commands_Manual*.

The following figure shows the hardware power-off process:

Figure 5-9 Module power-off timing

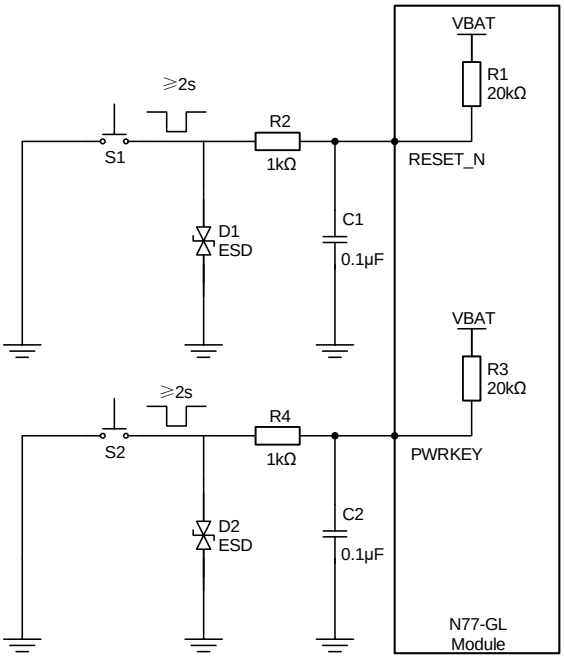


The module's shutdown time may vary depending on the firmware version; actual testing should be used for accurate assessment.

5.2.3 Resetting Methods

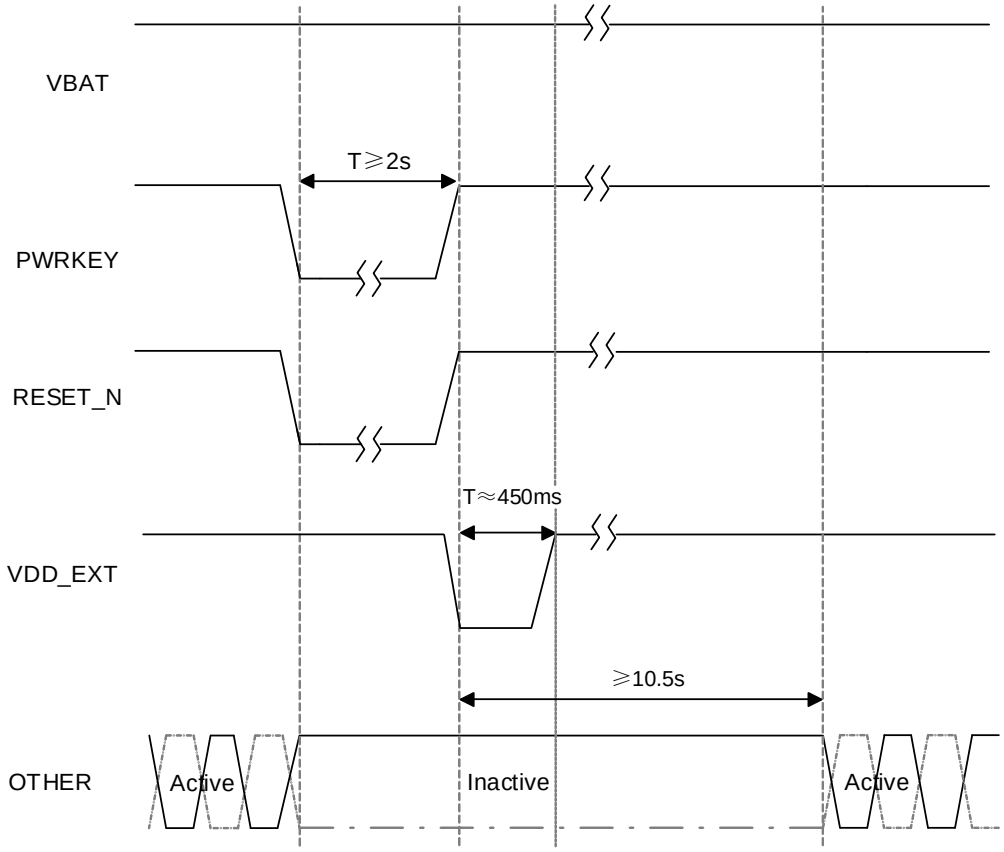
In the normal working state of the module, pulling both PWRKEY and RESET_N low for more than 2s can trigger a hard reset of the module.

Figure 5-10 Reference design for push-button reset



N77-GL module reset process is shown in the following figure.

Figure 5-11 N77-GL module reset process



The MiFi baseline version defaults to a 2-second dual-button hard reset. For reset methods of other baseline versions, please consult Neoway FAEs.

5.3 Peripheral Interfaces

This chapter mainly introduces the N77-GL module's peripheral interfaces.

The I/O direction, indicated by the module's peripheral interface pin, aligns with the module's orientation. Conversely, the I/O direction for the peripheral pin mirrors the characteristic of the associated peripheral component. For example, UART_TXD is the module's data send pin and MCU_RXD is the MCU's receive pin. These pins should be interconnected. During MCU selection and design, ensure that pin naming aligns with either the module or MCU.

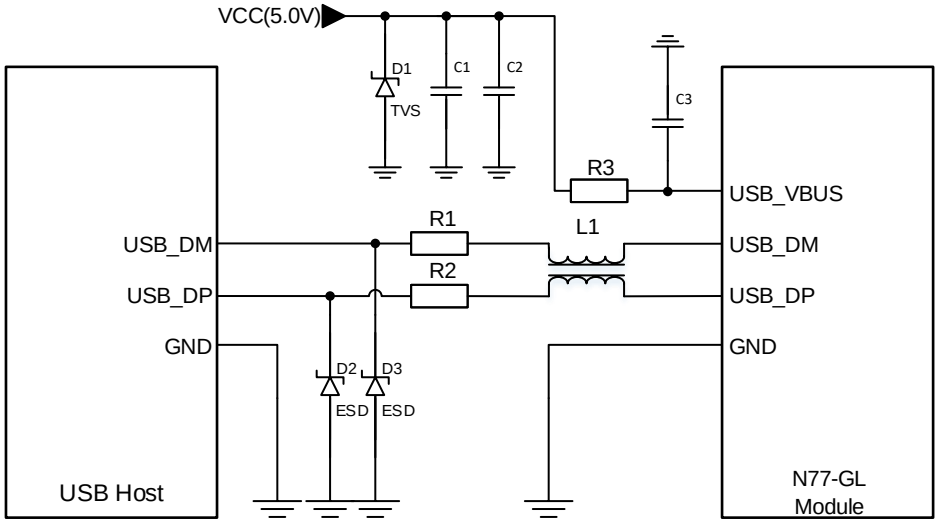
5.3.1 USB

Signal	Pin SN	I/O	Function description	Remarks
USB_VBUS	71	AI	USB power supply detection input	V_{min}=4.5 V V_{norm}=5.0 V V_{max}=5.5 V Also used as a charging voltage detection pin
USB_DM	70	AIO	USB data -	USB 2.0. This pin is used for software download and data transmission. Route the DM and DP traces as differential pairs, and the impedance of the differential pairs is 90 Ω.
USB_DP	69	AIO	USB data +	

When the USB_VBUS detects a USB insertion, the module will automatically power on. In the normal operating state of the module, if the USB_VBUS continuously detects an inserted state, the module will automatically power on again after executing the button shutdown, making it unable to achieve a button shutdown.

N77-GL can implement program download, data communications, and debugging through the USB interface. The module's USB interface defaults to "slave device mode", available for user selection based on specific requirements. The recommended USB connection circuit is shown in Figure 5-12.

Figure 5-12 Reference circuit design of USB connection



Schematic Design Guidelines

- Connect a 1 μF (C1) and a 33 pF (C2) filter capacitors in parallel to the USB_VBUS trace. A TVS device should be added to the power trace for protection.
- Ensure that the junction capacitance of the ESD components (D2 and D3) in parallel to the USB_DP and USB_DM traces be less than 0.5 pF.
- Series resistors or common-mode inductors are needed in series at the USB_DM and USB_DP pins (R1, R2) to enhance EMC performance. The selection of series resistor values and inductor types should be based on the actual USB signal quality.

PCB Design Guidelines:

- Place the filter capacitor on the USB_VBUS trace as close to the module pins as possible and place the ESD component as close to the USB connector as possible.
- Place the ESD diodes on the USB_DP and USB_DM traces as close to the USB connector as possible.
- It is important to route USB signal traces as differential pairs with ground surrounded. The impedance of the USB differential traces should be 90 Ω. The traces from the USB interface of your application PCB to the module must be isolated from other signal traces.

5.3.2 UART*

In environments with complex electromagnetic interference, the module's UART is susceptible to external electromagnetic interference, which can cause serious communication abnormalities. Therefore, please note the following when routing the UART signal trace on the PCB:

- Parallel a 5 to 10 pF capacitor near the module's UART_RXD and UART_TXD pins for filtering.
- Route UART traces far away from potential sources of interference.
- Route UART_RXD and UART_TXD traces on the inner layers of the PCB, maintain short trace lengths, avoid extensive routing on the top or bottom layers, and use a three-dimensional ground layout for these pins to enhance signal integrity.

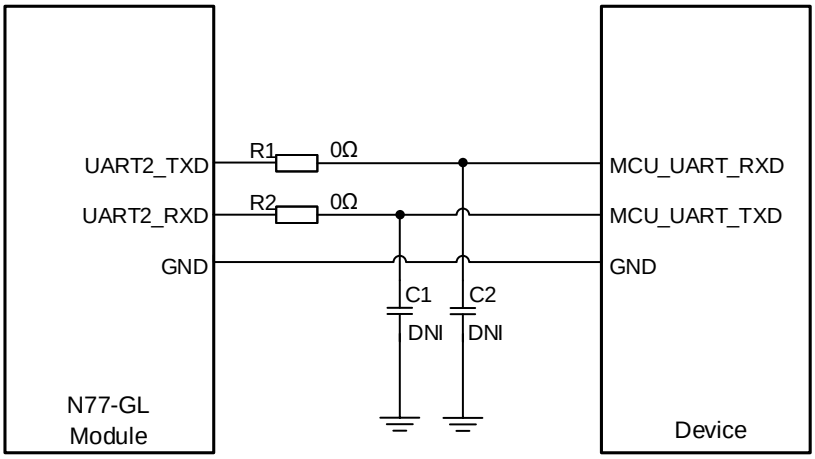
Signal	Pin SN	I/O	Function description	Remarks
UART2_TXD	67	DO	UART data output	Before use, please verify the configuration features corresponding to the software version. Leave this pin open if unused.
UART2_RXD	68	DI	UART data input	
UART2_DTR	66	DI	Data terminal ready	Leave this pin open if unused.
UART2_RTS	65	DO	UART request to send data	
UART2_CTS	64	DI	UART clear to send data	
UART2_DCD	63	DO	Data carrier detect	
UART2_RI	62	DO	Ring indicator	
DBG_TXD	12	DO	UART data output	During the normal startup of the module, log information will be output from this pin; before powering on, connect this pin to GND with a 1 kΩ resistor to enter USB download mode.
DBG_RXD	11	DI	UART data input	After the module has successfully booted up, this pin is exclusively used for debug purposes.

The N77-GL module by default offers three UART interfaces. BT_UART theoretically supports up to 3 Mbps speed. For BT_UART, refer to section 5.4.2 . UART2 supports up to 921600 bps speed. DBG is used as the default Debug UART and outputs Log information during startup. DBG_TXD is also compatible with USB forced download control functions.

All UART interfaces operate at a 1.8V level. For their reference design, please refer to Figure 5-13.

Only the connection relationship of UART2_TXD and UART2_RXD is listed here.

Figure 5-13 Reference design of the UART chip



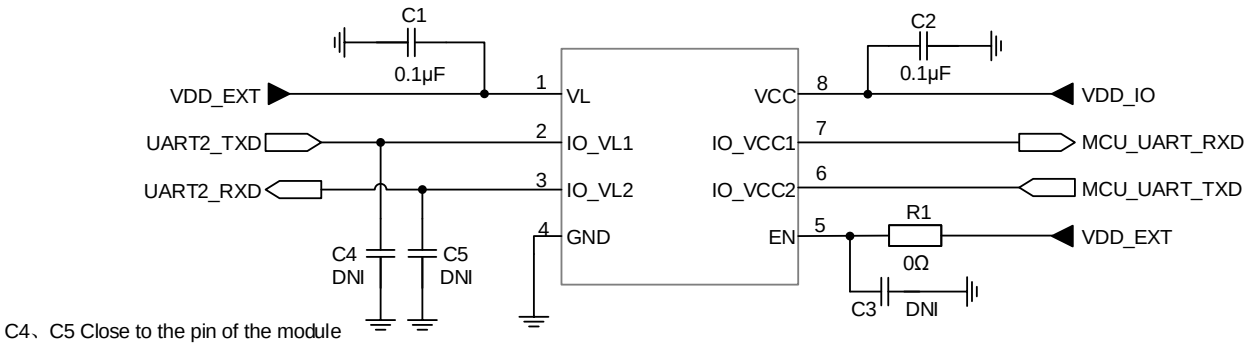
Schematic Design Guidelines

- Pay attention to the mapping relationship of signals.
- Figure 5-13 is only suitable for 1.8 V level systems and the use of diodes for level translation is prohibited.
- The resistance and capacitance values for R1, R2, C1, and C2 should be adjusted based on the waveform quality obtained through product testing.
- If an external connector is used for the signal, it is recommended to place an ESD protection device close to the connector.

If the the logic voltage of UART does not match that of the MCU, include an external voltage-level translation circuit. Three voltage-level translation circuits are recommended based on the differences in logic levels and rates.

If the UART baud rate is greater than 115200 bps, it is recommended to refer to the recommended voltage-level translation circuit 1.

Figure 5-14 Recommended voltage-level translation circuit 1



C4、C5 Close to the pin of the module

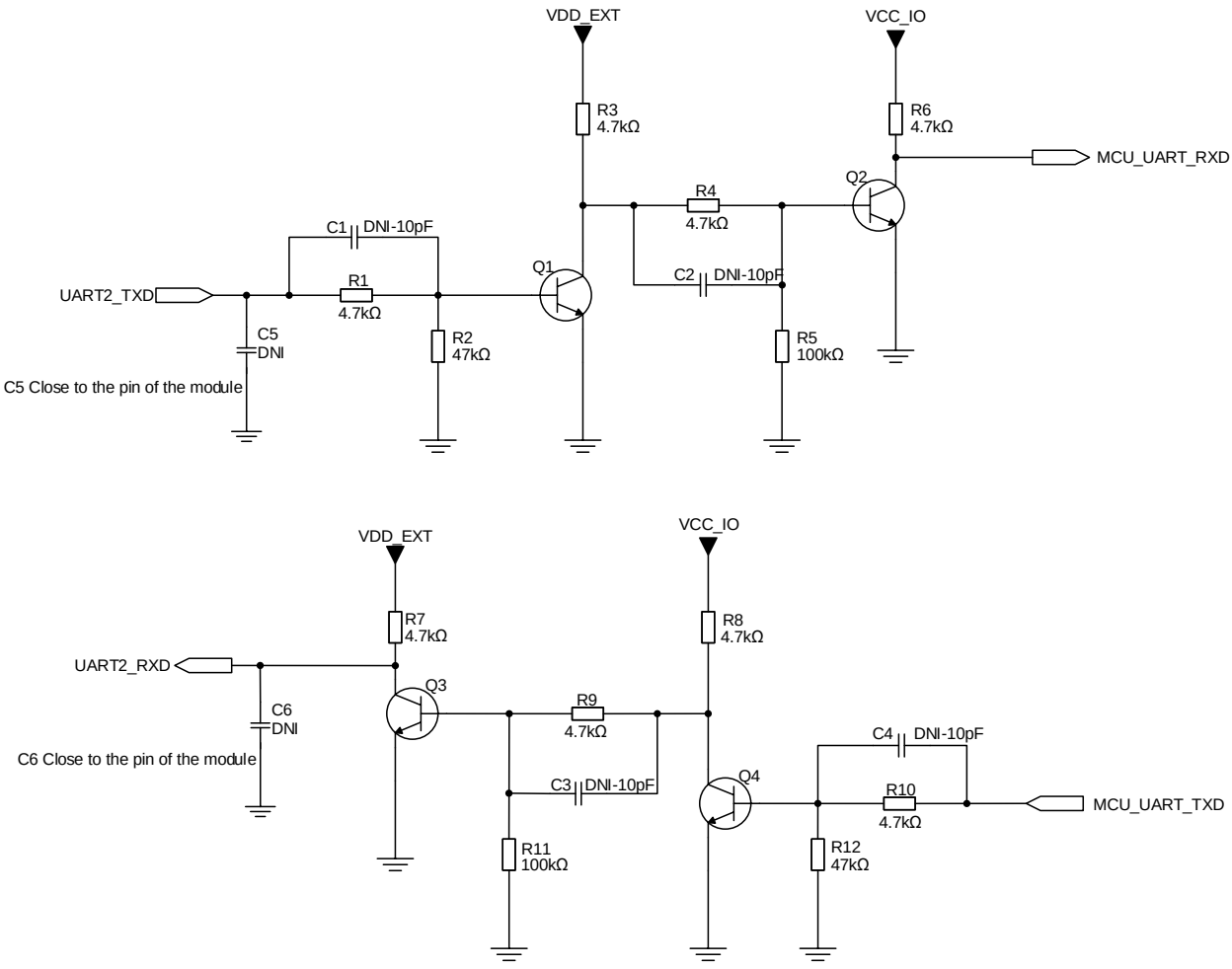
Schematic Design Guidelines

- It is recommended to select a bidirectional high-speed level translation chip.
- VL: reference voltage for IO_VL1 and IO_VL2.
- VCC: reference voltage for IO_VCC1 and IO_VCC2.
- EN is the enable pin, which works at a voltage of greater than VL-0.2 V. In the above circuit, the EN pin is connected to VDD_EXT and the voltage translator is always working.
- It is recommended to reserve positions for capacitors C4 and C5 (with suggested capacitance values of 5 ~10pF) and adjust them based on actual test results.

Dual-Triode Voltage-Level Translation Circuit (Baud Rate ≤ 115200 bps): Refer to the recommended voltage-level translation circuit 2.

If the serial port baud rate is less than or equal to 115200 bps, design the serial port TXD and RXD by referring to recommended voltage-level translation circuit 2, as shown in Figure 5-15

Figure 5-15 Recommended voltage-level translation circuit 2



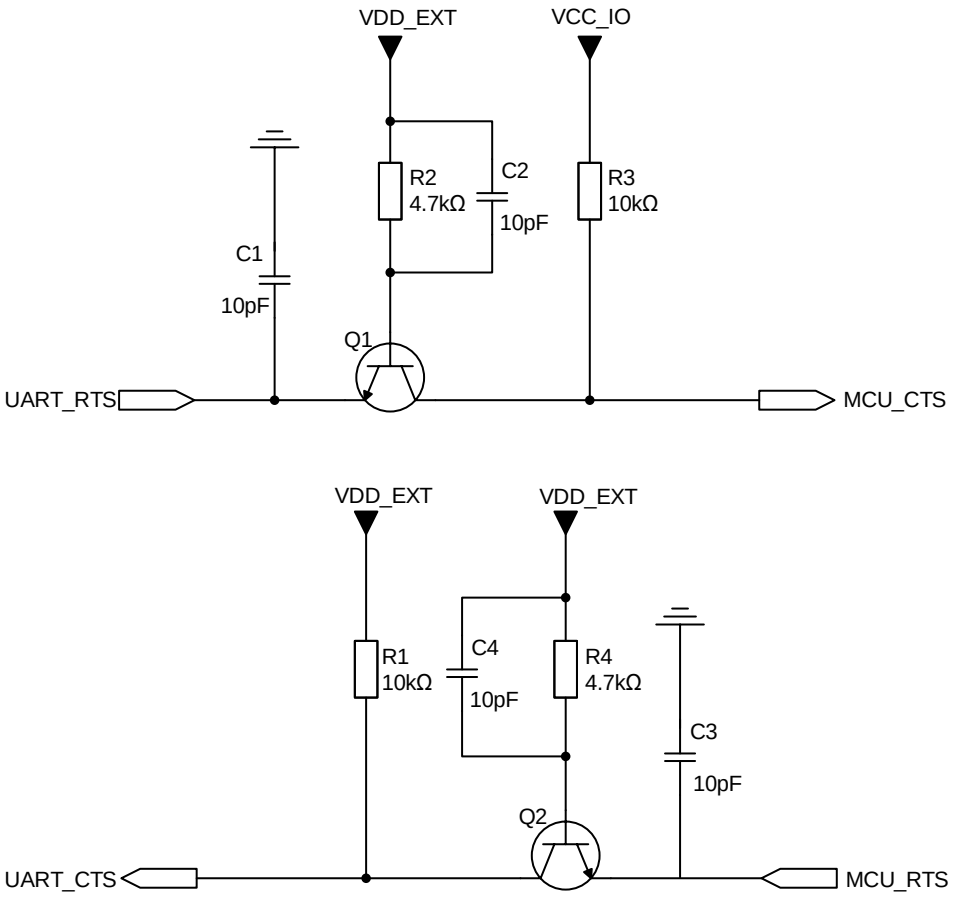
Schematic Design Guidelines

- MCU_UART_TXD and MCU_UART_RXD are the sending and receiving pins of MCU respectively, and UART2_TXD and UART2_RXD are the sending and receiving pins of module respectively. VCC_IO is the IO voltage of the MCU. VDD_EXT is the IO voltage of the module.
- The base voltage-dividing resistor of the triode need to be adjusted based on actual waveform measurements, ensuring complete conduction of the triode across the entire operational temperature range.
- The capacitance values for reserved capacitors C1~C6 should also be adjusted according to actual test results.

Single-Triode Voltage-Level Translation Circuit

Design the serial port pins CTS and RTS by reference to recommended voltage-level translation circuit 3, as shown in Figure 5-16.

Figure 5-16 Recommended voltage-level translation circuit 3



Schematic Design Guidelines

- R2/R4: 2 kΩ - 10 kΩ The higher the baud rate of the serial interface, the smaller the R2/R4 value.
- R1/R3: 4.7 kΩ - 10 kΩ The higher the working rate of the serial port, the smaller the value of R1/R3.

5.3.3 USIM

If using a single SIM, it is recommended to utilize USIM1.

Signal	Pin SN	I/O	Function description	Remarks
USIM1_VDD	14	PO	USIM1 power output	Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented.
USIM1_DATA	15	B	USIM1 data	Leave this pin open if unused.
USIM1_CLK	16	DO	USIM1 clock	Leave this pin open if unused.
USIM1_RST	17	DO	USIM1 reset	Leave this pin open if unused.
USIM1_PRESENCE	13	DI	USIM1 plug detection	If the hot-swap feature is not in use, this pin should still include a 47 kΩ pull-up resistor connected to VDD_EXT.
USIM2_VDD	128	PO	USIM2 power output	Both 1.8 V and 3.0 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented.
USIM2_DATA	73	B	USIM2 data	Leave this pin open if unused.
USIM2_CLK	74	DO	USIM2 clock	Leave this pin open if unused.
USIM2_RST	75	DO	USIM2 reset	Leave this pin open if unused.
USIM2_PRESENCE	76	DI	USIM2 plug detection	If the hot-swap feature is not in use, this pin should still include a 47 kΩ pull-up resistor connected to VDD_EXT.

The N77-GL module provides two USIM card interfaces that support either 1.8 V or 3.0 V USIM cards, with adaptive voltage compatibility. The following shows the reference design of the USIM card

connection.

Figure 5-17 Recommended design of the USIM interface (normally close connector)

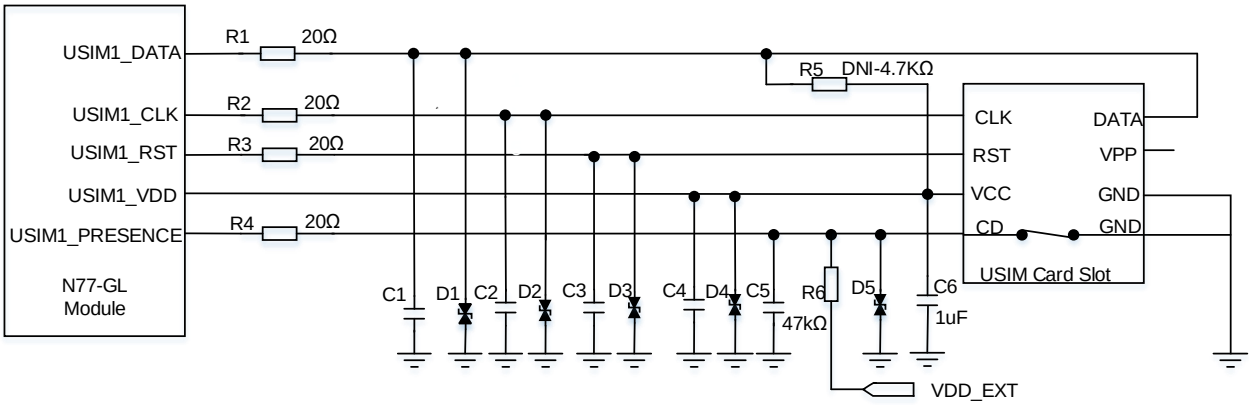
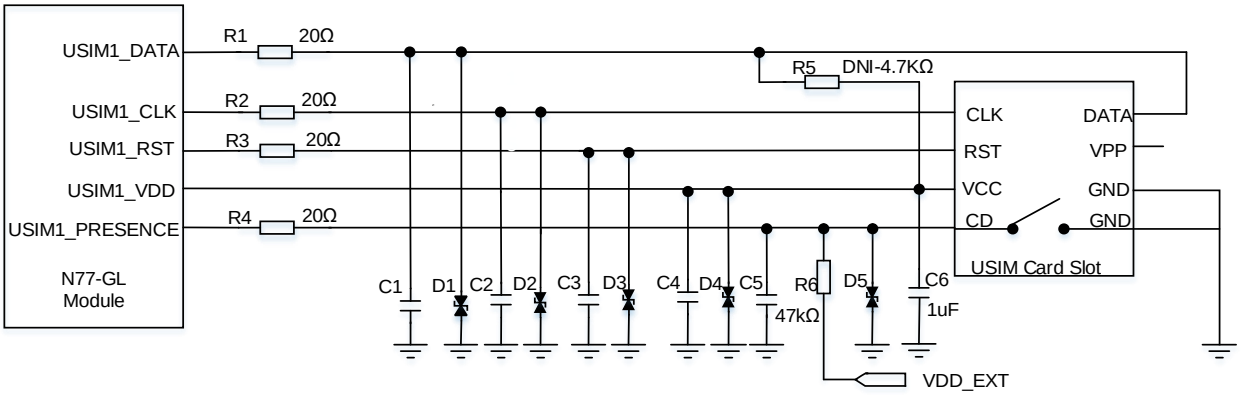


Figure 5-18 Recommended design of the USIM interface (normally open connector)



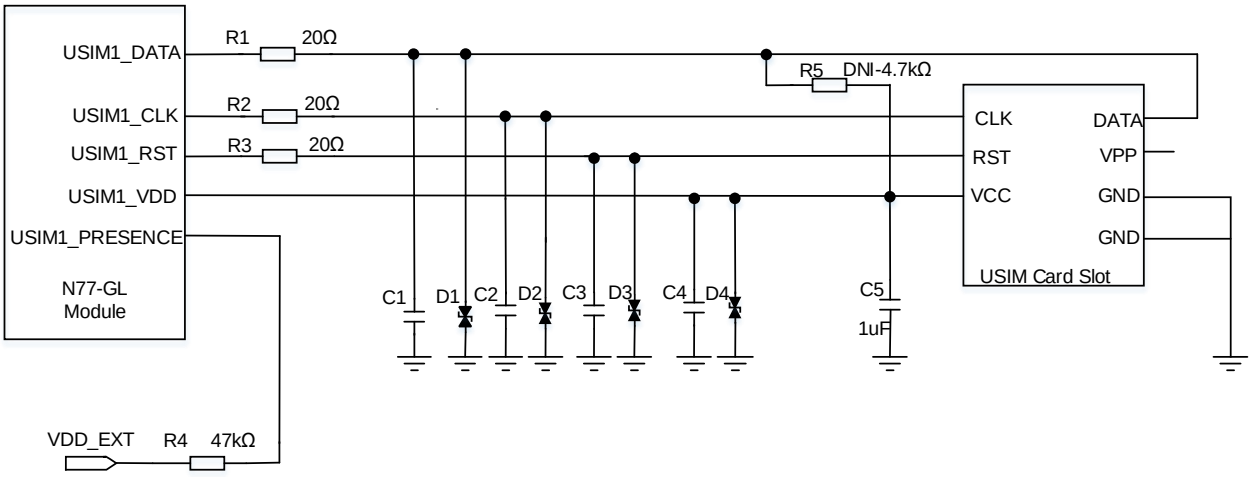
Schematic Design Guidelines

- USIM_VDD is the pin to supply power for USIM card and its maximum load is 50 mA. It is solely used for power supply for USIM card; do not power other loads.
- It is recommended to reserve a 4.7 kΩ pull-up resistor on the USIM_DATA pin connected to USIM_VDD.
- The applications in complex electromagnetic environment require ESD protection of high quality, so it is recommended to add ESD protection components (junction capacitance no more than 7 pF) on each signal traces.
- Connecting a resistor (not greater than 20 Ω) respectively to USIM_DATA, USIM_RST, USIM_CLK, USIM_ PRESENCE (close to the card connector) in series can enhance the ESD performance.
- C1 - C5 are in parallel to each USIM signal trace and are used to attach high-frequency filter capacitors, with capacitance ≤ 10 pF (adjust the value according to actual situations). They are unmounted by default.

- N77-GL supports USIM detection. USIM_PRESENCE is a 1.8 V interrupt pin. The USIM detection circuit works by checking the level of the voltage across the USIM_DET pin before and after a USIM card is inserted. In the reference circuit, SIM_DET is grounded before a USIM card is inserted and is connected to a 1.8 V voltage after a USIM card is inserted. The high voltage-level means USIM card detected while the low voltage-level means no USIM card detected. In the reference circuit, SIM_DET is at a high-level voltage before a USIM card is inserted and is grounded after a USIM card is inserted. The low voltage-level means USIM card detected while the high voltage-level means no USIM card detected. If the insertion detection function is not required, refer to Figure 5-19.

If the USIM card hot-swapping function is not used, the USIM_DET pin must be pulled up to VDD_EXT with a 47 kΩ resistor in series, and the USIM hot-swapping detection function must be disabled in software. Figure 5-19 shows the reference design of USIM card (without hot-swapping function) interface.

Figure 5-19 Reference design for USIM card interface (without hot-swap)



PCB Design Guidelines:

- USIM signals are like to be jammed by RF radiation, resulting in failure to detect the SIM card. Keep the USIM far from the antenna and RF circuit area to prevent jamming.
- Keep USIM card connectors close to the module and keep USIM traces as short as possible.
- On the USIM traces, connect the series resistor and ESD protection component close to the USIM card.
- In order to enhance EMC, surround USIM traces with ground.

5.3.4 SD*

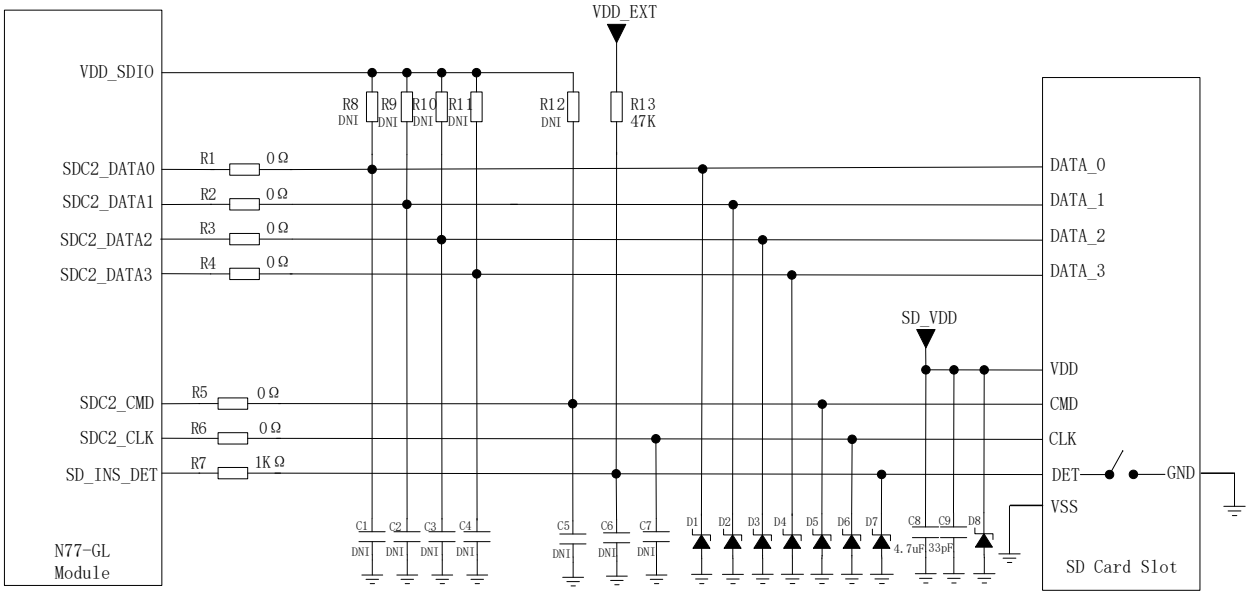
Signal	Pin SN	I/O	Function description	Remarks
VDD_SDIO	34	PO	SDIO pull-up power supply	Only used for SDC2_CMD and SDC2_DATA pull-ups
SDC2_DATA0	31	B	SD card data 0	50 Ω single-terminal impedance control
SDC2_DATA1	30	B	SD card data 1	
SDC2_DATA2	29	B	SD card data 2	
SDC2_DATA3	28	B	SD card data 3	
SDC2_CLK	32	DO	SD card clock	
SDC2_CMD	33	B	SD card command	
SD_INS_DET	23	DI	SD card plug detection	Leave this pin floating if the hot-swapping function is not used and the function should be disabled in software.

The SD operates as a dual-voltage SD 3.0 interface. It supports a maximum clock frequency of SDR 200 MHz or DDR 50 MHz. This interface is backward compatible with DS, HS, SDR12, SDR25, SDR50, and SDR104 modes, providing extensive compatibility with various operational modes.

- VDDSDIO is only used for SDC2_CMD and SDC2_DATA pull-ups. Do Not supply power for other peripherals.
- Leave this pin floating if the hot-swapping function is not used and the function should be disabled in software.

The following figure shows the connection of the SDC interface.

Figure 5-20 Reference design of the SD card (with hot-swap) interface



Schematic Design Guidelines

- SD_VDD is the driving power for the SD card peripheral, requiring an external LDO provided by the customer. If an externally connected SD card supports SDR104, it is recommended to choose an LDO with a 1A output capacity.
- VDD_SDIO is a dual voltage of 1.8 V/3.0 V, which can automatically adapt to the IO voltage of the SD card. It outputs a maximum current of 50 mA and is only used for SD pull-up. Do not use it for any other purpose.
- The module supports SD card detection. The SD_INS_DET pin is a 1.8V interrupt pin. The SD detection circuit works by checking the level of the voltage across the USIM_DET pin before and after a SD card is inserted. In the reference circuit, SD_INS_DET is at a high-level voltage (externally pulled up to VDD_EXT) before a SD card is inserted and is grounded after a SD card is inserted. The low voltage-level means SD card detected while the high voltage-level means no USIM card detected.

PCB Design Guidelines:

- CMD, CLK, and DATA are high-speed signal traces, which need to be controlled by 50 Ω single-terminal impedance. The traces should go as far as possible on the inner layer and control the equal length. The difference between the length of the CMD and DATA traces and the length of the CLK trace should not exceed 0.5 mm.
- SDC2_CLK needs to be grounded separately.
- Spacing between DATA traces should be larger than 2 times trace width.

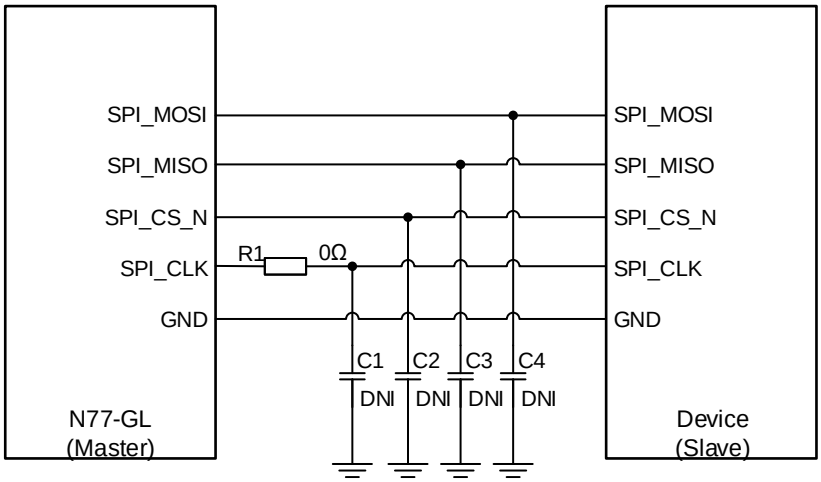
5.3.5 SPI

Generic SPI

Signal	Pin SN	I/O	Function description	Remarks
SPI_CLK	81	DO	Clock signal	48 MHz at most.
SPI_MISO	79	DI	Output of slave device, input of master device	Leave this pin open if unused.
SPI_MOSI	80	DO	Input of slave device, output of master device	Leave this pin open if unused.
SPI_CS_N	78	DO	Chip selection signal of slave device	Leave this pin open if unused.

The SPI interface uses a 1.8 V level, with clock frequencies up to 48 MHz. Please refer to Figure 5-21 for circuit design.

Figure 5-21 Reference design for the SPI interface



Schematic Design Guidelines

- Pay attention to the mapping relationship of signals.
- Figure 5-21 is only suitable for 1.8 V level systems and the use of diodes for level translation is prohibited.
- Please adjust or determine the need for R1, C1~C4 based on the waveform quality obtained through product testing.

- If an external connector is used for the signal, it is recommended to place an ESD protection device close to the connector.

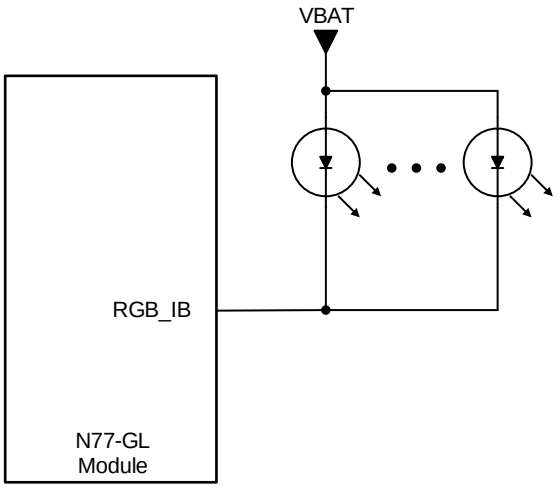
SPI LCD

Signal	Pin SN	I/O	Function description	Remarks
SPI_CLK	81	DO	Clock signal	48 MHz at most.
SPI_MISO	79	DI	Output of slave device, input of master device	Leave these pin open if unused.
SPI_MOSI	80	DO	Input of slave device, output of master device	
SPI_CS_N	78	DO	Chip selection signal of slave device	
SPI_CD	82	DO	Data/command selection	
LCD_RST_N	84	DO	Reset signal	
LCD_TE	83	DO	Frame sync	
VDD2V8	116	PO	2.8 V power output	Can be used to power an external SPI LCD.

The N77-GL module supports SPI LCD, with a maximum resolution of 320*240 pixels. It supports 3-wire 9-bit and 4-wire 8-bit configurations. The specific connection method is determined by the external LCD selection.

For the LCD backlight, the RGB_IB interface can be used. The cathode of the backlight LED connects to RGB_IB, with a maximum output current of 218 mA. The desired current can be adjusted through registers. The following shows the reference design:

Figure 5-22 Reference design of the RGB_IB interface

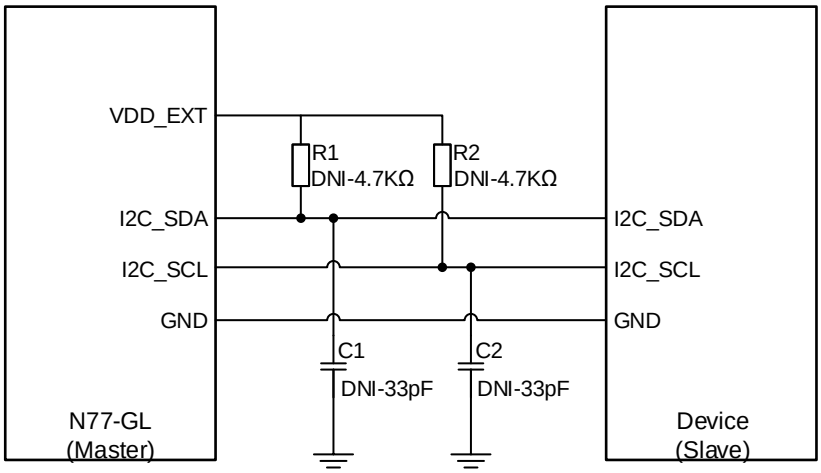


5.3.6 I2C

Signal	Pin SN	I/O	Function description	Remarks
I2C1_SDA	42	B	I2C data	The module can be configured via software for 1.8 kΩ/ 4.7 kΩ/ 20 kΩ pull-up resistors. It is recommended to reserve a pull-up resistor connected to VDD_EXT. Leave this pin open if unused.
I2C1_SCL	41	DO	I2C clock	
I2C2_SDA	124	B	I2C data	
I2C2_SCL	123	DO	I2C clock	

The N77-GL module offers two I2C interfaces, supporting only master mode. The interface accommodates both LS (100 Kbps) and FS (400 Kbps) modes and operates at a 1.8 V level. A pull-up resistor is recommended for reservation. Figure 5-23 shows the reference design of the I2C interface.

Figure 5-23 I2C reference design



Schematic Design Guidelines

- Figure 5-23 is only suitable for 1.8 V level systems and the use of diodes for level translation is prohibited.
- Please confirm the resistance values for pull-up resistors R1 and R2 based on the requirements of the external devices connected to the module.
- Please adjust or determine the need for C1 and C2 based on the waveform quality obtained through product testing.
- If external connectors are used for the I2C signals, it is advised to insert resistors in series with the I2C signal traces and to place ESD protective devices close to the connectors.

5.3.7 ADC

The N77-GL module provides two 11-bit ADC channels, with measurable voltage range 0.1 V - VBAT, which can be used for temperature measurement and other related measurement. For details, see *Neoway_N77_AT_Commands_Manual*.

Signal	Pin SN	I/O	Function description	Remarks
ADC0	45	AI	Generic analog-to-digital signal	Detectable voltage range: 0.1 V - VBAT.
ADC1	44	AI	Generic analog-to-digital signal	

5.4 Network and Connection

The N77-GL supports connectivity to external Bluetooth and Wi-Fi chips or modules.

5.4.1 SDIO/WLAN

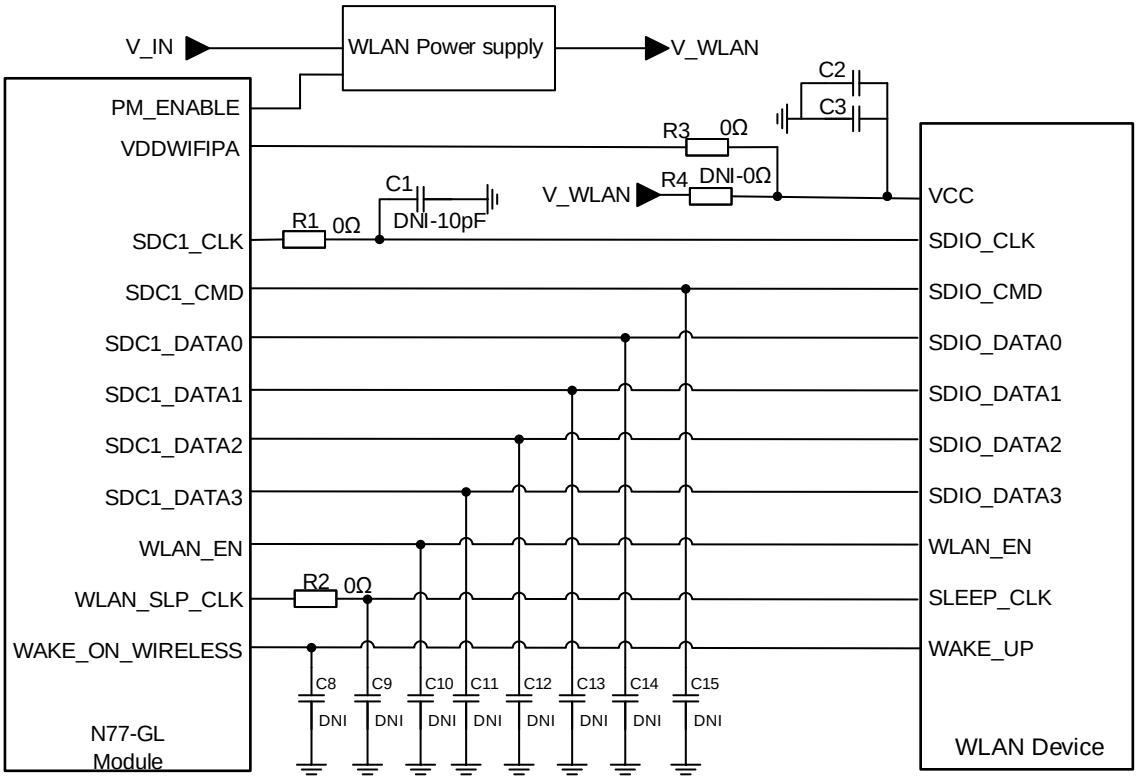
Signal	Pin SN	I/O	Function description	Remarks
VDDWIFIPA	141	PO	3.3 V power output	Can be used to power an external WLAN module. If the 3.3V power supply of the WLAN has a maximum load current greater than 400mA, an external DC/DC or LDO is required. Leave this pin open if unused.
SDC1_CMD	134	B	SDIO command	Leave this pin open if unused.
SDC1_CLK	133	DO	SDIO clock	It is recommended to reserve an RC near the module to prevent EMI. Leave this pin open if unused.

SDC1_DATA0	132	B	SDIO bus data 0	Leave this pin open if unused.
SDC1_DATA1	131	B	SDIO bus data 1	
SDC1_DATA2	130	B	SDIO bus data 2	
SDC1_DATA3	129	B	SDIO bus data 3	
WAKE_ON_WIRELESS	135	DI	Wake up the module by WLAN	
WLAN_SLP_CLK	118	DO	WLAN sleep clock	Clock frequency: 32.768 kHz Leave this pin open if unused.
WLAN_EN	136	DO	WLAN enable	Active low. Leave this pin open if unused.
PM_ENABLE	127	DO	WLAN external power enabling	Active low. Leave this pin open if unused.

The WLAN interface uses SDIO that supports SDIO 3.0 and operates solely at a 1.8 V voltage level. The SDIO interface maximumly supports SDR104-208 MHz or DDR50-50 MHz clock frequencies and is backward compatible with DS, HS, SDR12, SDR25, and SDR50 modes. The theoretical maximum data transfer rate of the bus is 104 MB/s. Due to variations in actual signal quality, please refer to empirical testing metrics.

Please refer to Figure 5-24 for circuit design.

Figure 5-24 Reference design for the WLAN interface



Schematic Design Guidelines

- The WLAN_SLP_CLK frequency is 32.768 KHz. If the trace length is too long, it is recommended to include an RC circuit close to the module.
- It is recommended to reserve an RC circuit on WLAN_SLP_CLK close to the module. The resistance and capacitance of the RC should be adjusted according to the actual signal quality.
- The use of WAKE_ON_WIRELESS, WLAN_SLP_CLK should be determined based on the specific WLAN chip chosen. For details, consult Neoway FAEs.

PCB Design Guidelines:

- Control the equal length for the SDIO interface. For the specific equal length requirements, see the requirements of the corresponding WLAN chip or module.
- Control the impedance for each SDIO trace to 50 Ω.

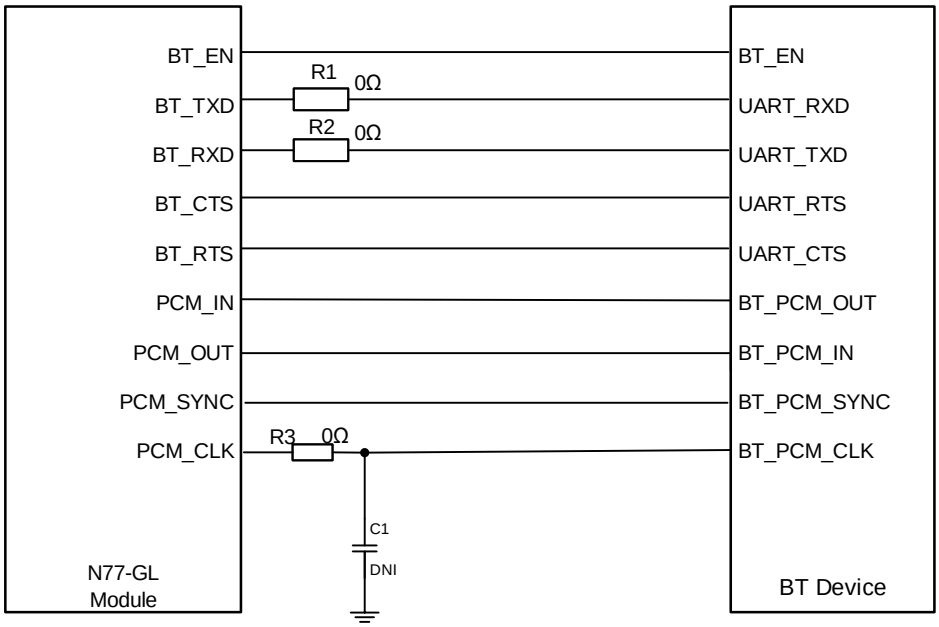
5.4.2 Bluetooth

Signal	Pin SN	I/O	Function description	Remarks
BT_TXD	38	DO	Bluetooth serial interface data output	It is used for Bluetooth data transmission. Leave this pin open if unused.
BT_RXD	39	DI	Bluetooth serial interface data input	
BT_CTS	40	DI	UART clear to send	It is used for Bluetooth data hardware flow control. Leave this pin open if unused.
BT_RTS	37	DO	UART request to send	
BT_EN	139	DO	Bluetooth enable	Leave this pin open if unused.
PCM_IN	24	DI	PCM data input	
PCM_OUT	25	DO	PCM data output	
PCM_SYNC	26	B	PCM data frame synchronization	
PCM_CLK	27	DO	PCM clock	

The BT_UART interface can also be connected to other devices that support UART communication. For inquiries about using the BT_UART interface, please contact Neoway FAEs.

The N77-GL module provides a 4-wire BT_UART serial port that supports hardware flow control. The theoretical maximum communication rate is 3 Mbps. For the reference design of connecting external Bluetooth chips, please refer to Figure 5-25.

Figure 5-25 Reference design for external Bluetooth chip interface



Schematic Design Guidelines

- Figure 5-25 is a 1.8 V voltage level system. Please pay attention to the level matching of each pin during design.
- Note the sequence of UART and PCM connection wires.

5.5 Other Functional Interfaces

Signal	Pin SN	I/O	Function description
WAKEUP_IN*	1	DI	Sleep mode control
W_DISABLE#	4	DI	Flight mode control
AP_READY	2	DI	Sleep status detection
STATUS	61	OD	Working status indicator, an external pull-up resistor is required.
NET_MODE	5	DO	Network registration mode indication
NET_STATUS	6	DO	Network operation status indication
USB_BOOT	115	DI	Forcible download mode

5.5.1 WAKEUP_IN*

WAKEUP_IN is used to set the module into sleep mode and needs to be used together with the AT command. For details of the AT command, see *Neoway_N77_AT_Commands_Manual*. In sleep mode, the module can still responds to voice calls, SMS, and processes data service normally.

The following figure shows the process of entering sleep mode:

Figure 5-26 Process of entering into sleep mode

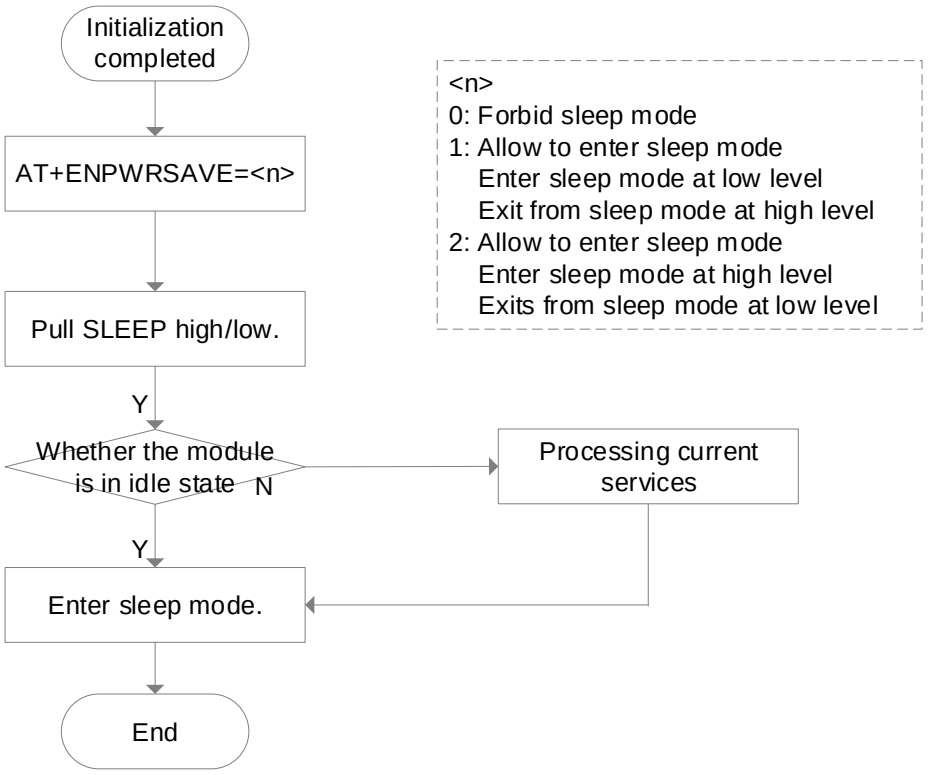


Figure 5-27 Process of processing data service in sleep mode

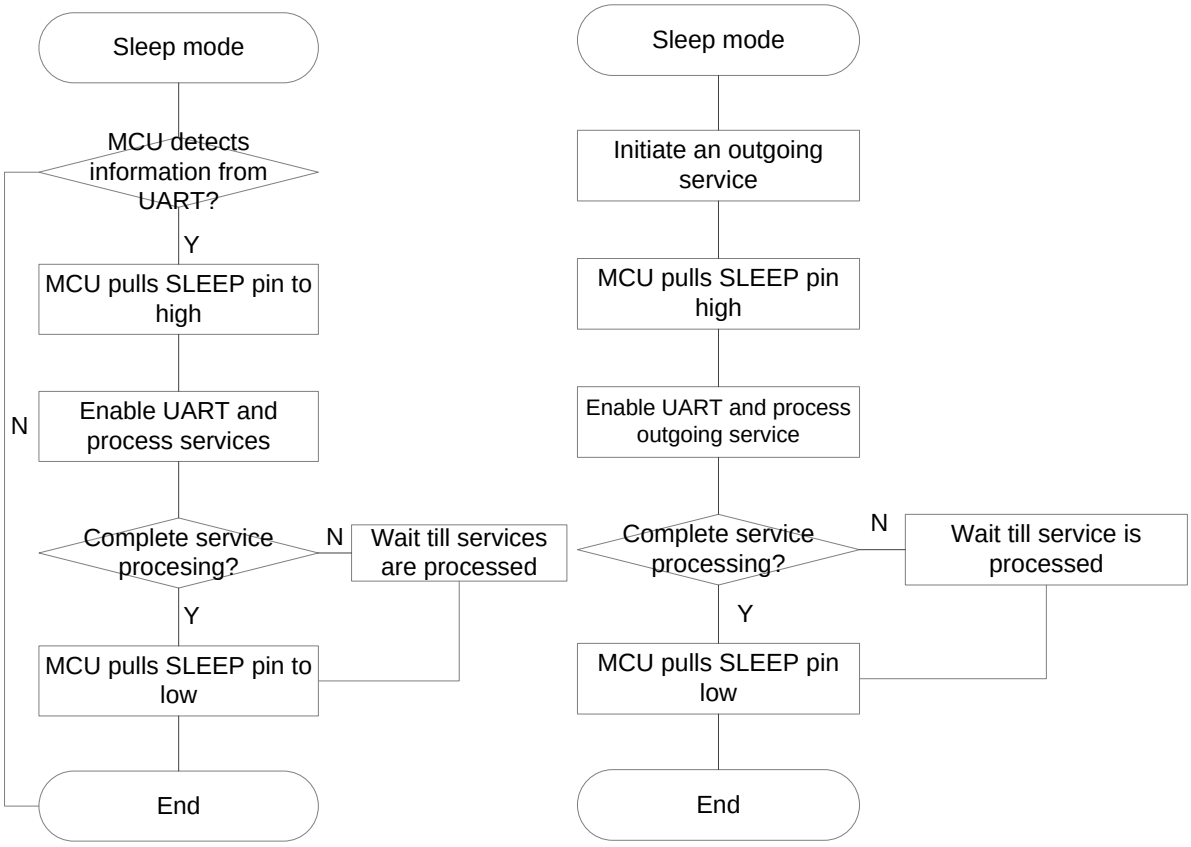
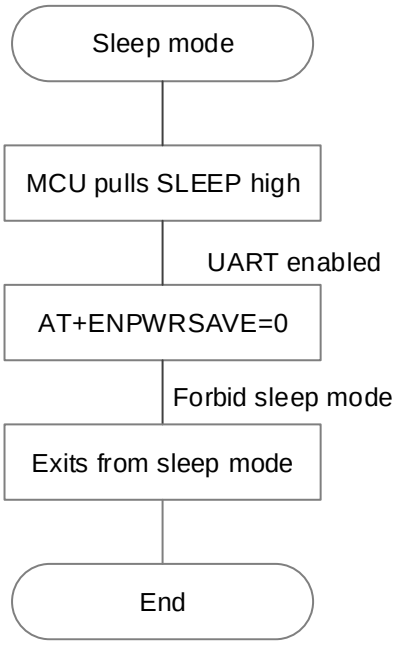


Figure 5-28 Process of existing from the sleep mode

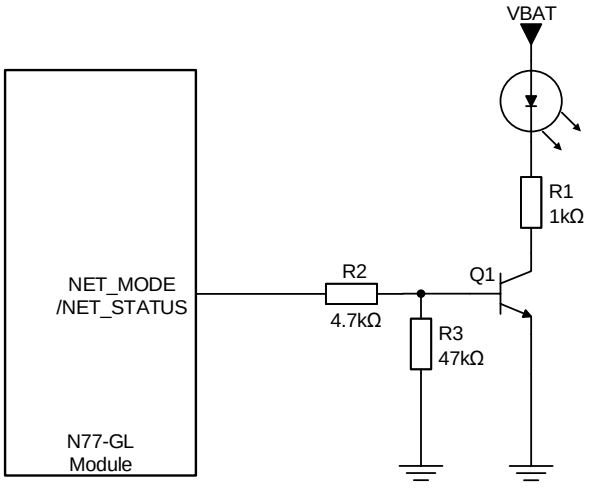


5.5.2 NET_MODE/ NET_STATUS

NET_MODE is the module's network registration mode indication pin, while NET_STATUS is the module's network operation status indication pin. During module operation, different duty cycle PWM waveforms can be output based on different working states, driving the LED indicator to flash at different frequencies. You can use the AT command to enable the LED indicator to blink in different states. For details, see *Neoway_N77_AT Command Manual.*

NET_MODE/ NET_STATUS pin outputs a high level of 1.85 V. It's prohibited to directly drive the LED indicator. It is recommended to control the LED through a transistor. Please refer to the specific reference design as shown in the diagram below.

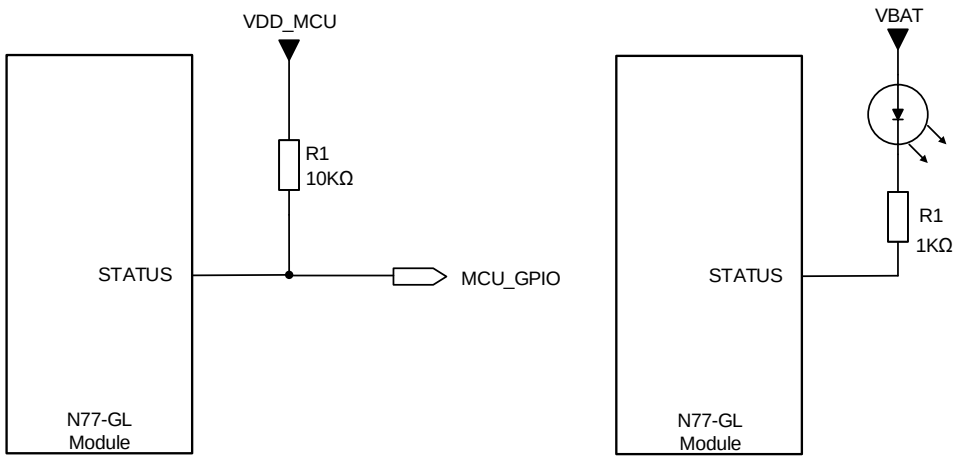
Figure 5-29 Driving LED with a triode



5.5.3 STATUS

STATUS is the module operation status indication pin with an open-drain output type. When in use, an external pull-up resistor is required. Two reference designs are shown in the diagram below.

Figure 5-30 Reference design of the STATUS chip

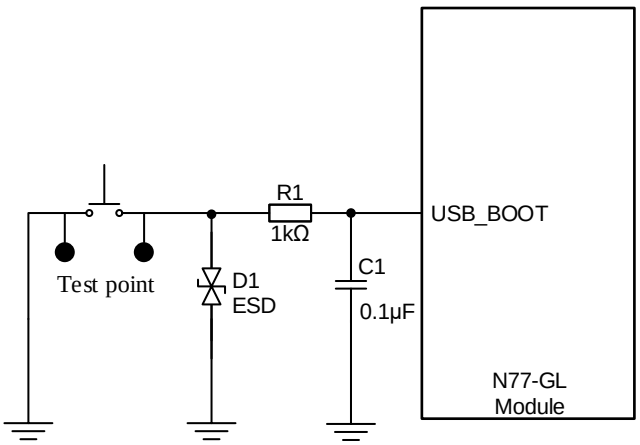


After VBAT power is lost, STATUS cannot be used to indicate the module's shutdown state.

5.5.4 USB_BOOT

The USB_BOOT pin is designed for enabling emergency download mode. Briefly pulling the USB_BOOT pin up to VDD_1P8 during the power-on sequence will activate the module into emergency download mode. This mode serves as a vital recovery method for product startup failure or malfunction. It is recommended to reserve the USB_BOOT pin within your design, allowing for potential emergency interventions when required. Adding an ESD component to protect USB_BOOT in the circuit is required.

Figure 5-31 Reference design for the emergency download pin



5.6 Signal Multiplexing

Table 5-3 Pin definitions

Function (default)	Pin SN	Multiplexing signal 1	Multiplexing signal 2	Remarks
NET_MODE	5	GPIO105	-	Low level by default
NET_STATUS	6	GPIO106	-	Low level by default
UART2_DTR	66	EXTINT5	GPIO113	Active low, with interrupt
UART2_RTS	65	GPIO17	PWMA	Active low
UART2_CTS	64	EXTINT3	GPIO19	Active low. with interrupt
UART2_DCD	63	GPIO18	PWMB	Active high
UART2_RI	62	GPIO104	-	Low level by default
WLAN_EN	136	GPIO100	-	Low level by default
PM_ENABLE	127	GPIO101	-	Low level by default
BT_CTS	40	GPIO82	PWMC	Low level by default
BT_RTS	37	EXTINT7	GPIO83	Active low, with interrupt
BT_EN	139	GPIO102	-	Low level by default
TP_INT	140	EXTINT2	GPIO15	Active low, with interrupt
TP_RST	18	GPIO115	-	Active high

If you need to multiplex the pin, ensure that the firmware supports the multiplexing; for details, contact Neoway FAEs.

5.7 RF Interfaces

Signal	Pin SN	I/O	Function description	Remarks
ANT_MAIN	49	AIO	Main antenna	50 Ω impedance

ANT_DIV	35	AIO	Diversity antenna	characteristic.

5.7.1 ANT_MAIN/ANT_DIV Antenna Interfaces

For the module to be applicable to your PCB, the characteristic impedance of the antenna interface should be controlled at 50 Ω and the impedance of the trace from the module's antenna interface to the antenna needs to be kept at 50 Ω to allow reception of radio frequency (RF) signals. In the circuit design, a matching network is essential for antenna matching in the circuit design. The matching network is generally divided into three types: L type, T type, and π type, which are shown in the following figure. The π-type matching circuitry is preferred.

Figure 5-32 L-type RF matching schematic

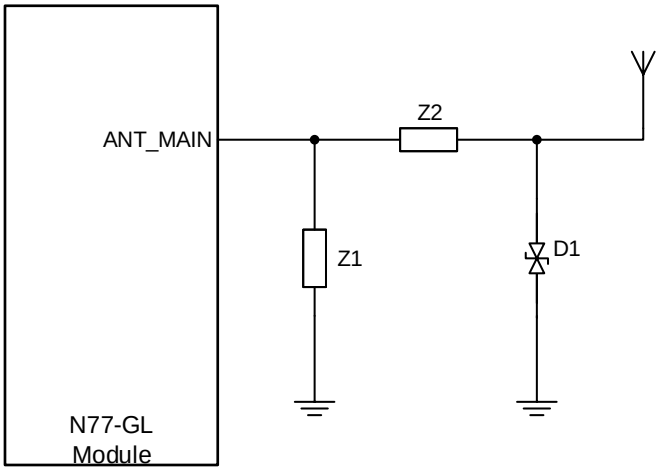


Figure 5-33 T-type RF matching schematic

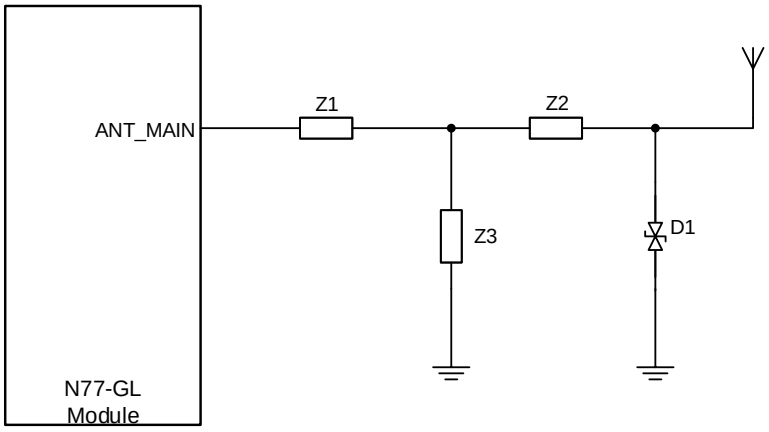
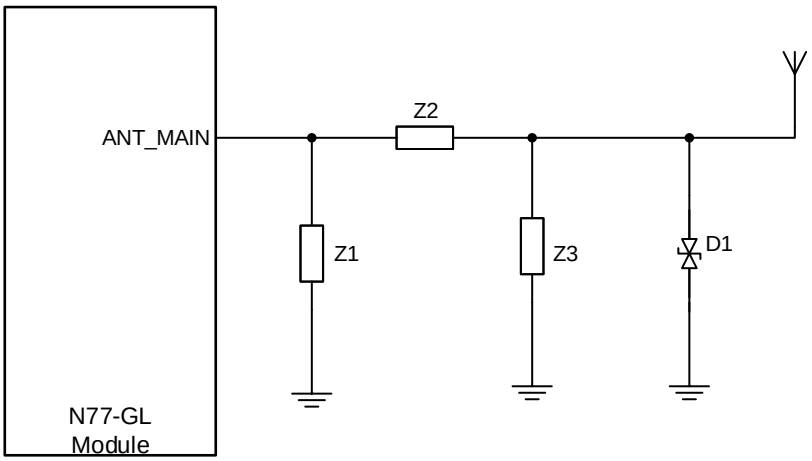


Figure 5-34 π-type RF matching schematic



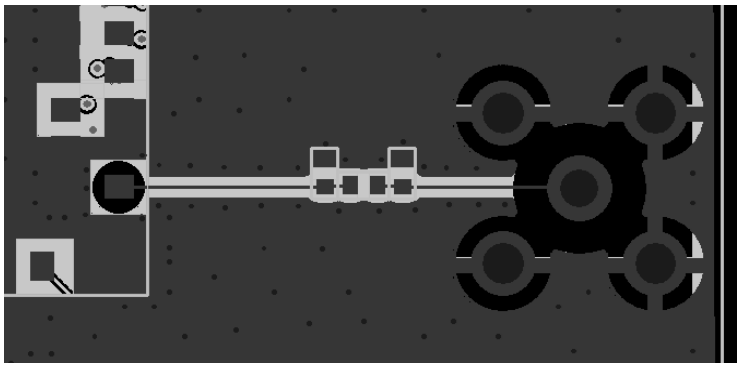
Schematic Design Guidelines

- The components in the RF matching circuit consist of capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- For situations involving electrostatic induction on the antenna, it is recommended to add electrostatic protection using ultra-low junction capacitance (less than 0.5 pF) ESD protection diodes. Besides, it is necessary to ensure that the reverse breakdown voltage of the ESD protection diodes is greater than 10 V, preferably 15 V or higher.

PCB Design Guidelines:

- Surround RF traces with grounded copper foil. Drill as many via holes as possible on the copper and control RF trace impedance to 50 Ω.
- Keep the PCB routing between the RF pin and the antenna interface under 50 Ω impedance control and make the trace length as short as possible.
- If using an SMA connector, hollow out the first and second layers below the RF solder pad or all layers of a multiple-layer PCB to minimize parasitic capacitance. The following is the recommended RF PCB design.

Figure 5-35 Recommended RF PCB design



- Position ANT_MAIN and other antennas at a reasonable distance to avoid mutual interference, affecting reception.
- On the PCB, keep the RF signals and components far away from digital circuits, switching power supplies, power transformers, power inductors, clock signals, etc.

5.7.2 Antenna Assembly

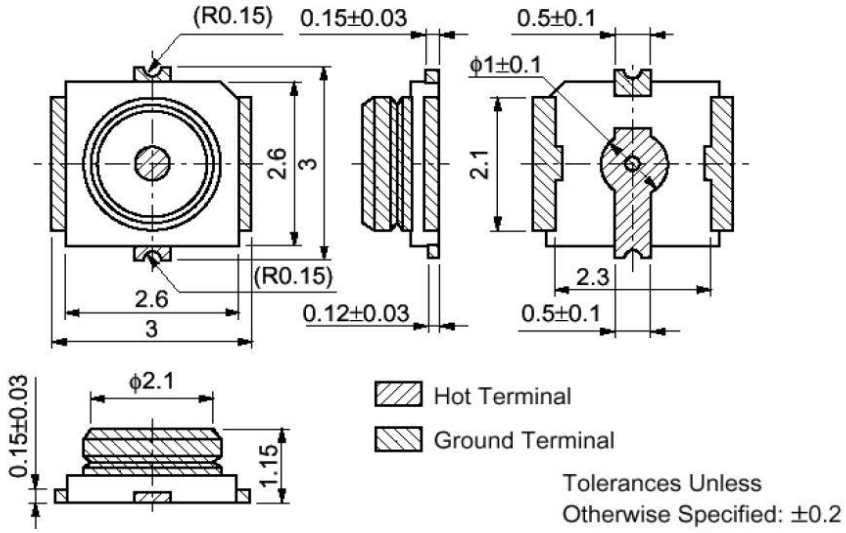
The antenna used by the module must comply with mobile device standards, with a standing wave ratio between 1.1 and 1.5, an input impedance of 50 Ω, and varying gain requirements based on the environment. You can choose an appropriate antenna according to specific application scenarios and environments.

The module antenna interface can be connected to rubber rod antenna, sucker antenna or internal PIFA antenna, with proper shielding between external antennas and RF pins. If using RF cable connections, keep the external RF cables away from all interference sources, especially digital signals and switching power supplies.

The following methods are commonly used to assemble antennas:

- Connecting to a GSC RF connector
  Recommended model MM9329-2700RA1. The following figure shows its encapsulation specifications. The connection to the external antenna can be made through RF lines.

Figure 5-36 Murata RF connector encapsulation specifications



- The RF cable is connected to the module by means of soldering. However, this method has the stability, consistency, and RF performance degradation issues, and therefore is not recommended.

The following figure shows the effect of the two connection methods.

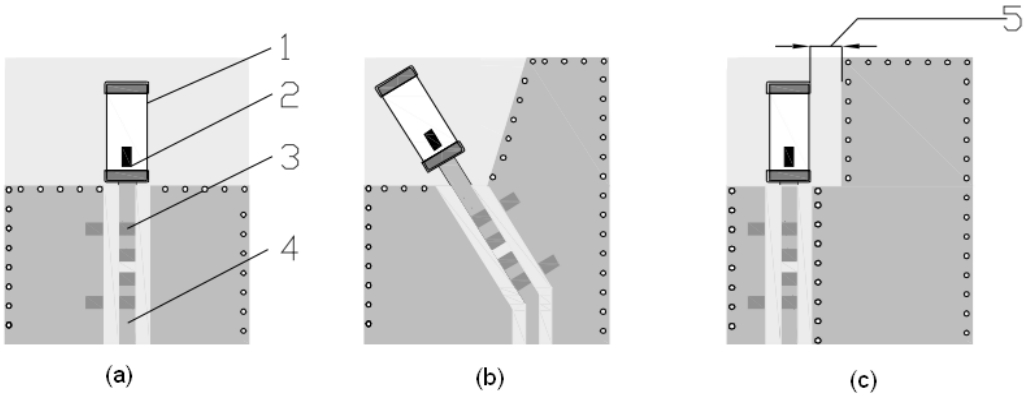
Figure 5-37 RF cable connections

- PCB antenna or chip antenna

  Due to the wide frequency range in which the module operates, PCB antennas or ceramic antennas find it difficult to cover such a broad frequency. Therefore, this type of connection is not recommended.

The following figure shows the layout of the 2.4G ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

Figure 5-38 Antenna layout

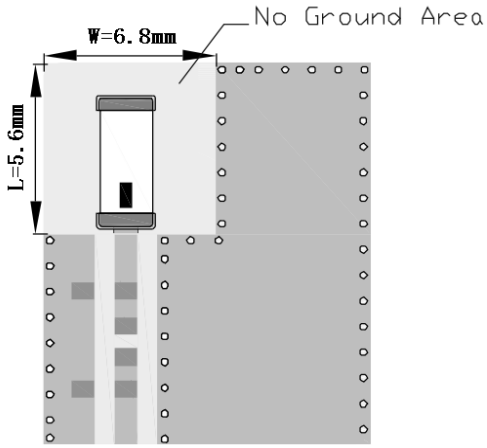


If there is enough space on the PCB, refer to Figure 5-38 (a).

- 1 Chip antenna
- 2 Antenna feed mark
- 3 Matching circuit pad
- 4 50 Ω impedance RF line

In Figure 5-38, the position marked as ”5“ depicts the area between the antenna and the ground. As shown in Figure 5-39, the "No Ground Area".

Figure 5-39 Clearance area (No Ground Area) around the antenna on the PCB board



For more details, refer to the antenna manuals and other documents.

6 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the N77-GL module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

6.1 Electrical Characteristics

If the voltage is lower than the threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.

When using LDO or DC-DC to power the module, ensure that it can output at least 2.5 A of instantaneous current. The 2.5 A current corresponds to the maximum power level of the module during GSM mode, and the peak current during burst transmission only lasts for a short time. Placing a large capacitor at the VBAT pin of the module can effectively enhance the freewheeling current of the power supply, preventing abnormalities like module shutdown caused by excessive voltage drop.

Table 6-1 N77-GL electrical characteristics

Pin SN	States	Min. value	Typical value	Max. value
VBAT	V_{in}	3.4 V	3.6 V	4.2 V
	I_{in}	-	-	2.5 A

Table 6-2 provides the power consumption data for the MiFi baseline version, which includes Wi-Fi functionality by default. This Wi-Fi consumes approximately 55 mA. Therefore, the actual maximum power consumption for each frequency band should be reduced by the power consumption of the Wi-Fi. For the actual baseline version in use, please consult with Neoway FAE.

Table 6-2 N77-GL current consumption (typical)

Status Network standard and band	Active (mA) @ max power
FDD-LTE: B1, B2, B3, B4, B5, B7, B8, B12 B13, B17, B18, B19, B20, B26, B28, B66	≤730 mA
TDD-LTE: B34, B38, B39, B40, B41	≤430 mA

WCDMA: B1, B2, B5, B8	≤640 mA
GSM/EDGE: 850/900/1800/1900 MHz	≤500 mA

6.2 Temperature Characteristics

The working temperature range for the MiFi baseline version is -20℃ to 75℃; for the module baseline version, it's -30℃ to 75℃. For the specific baseline version in use, please consult with Neoway FAE.

When the working environment temperature falls between -40℃ and -30℃ for low temperatures and between 75℃ and 85℃ for high temperatures, the RF performance of the module might deteriorate. However, this won't significantly impact the normal operation of the module, and the RF performance will recover once the temperature returns to the normal range.

Table 6-3 N77-GL temperature characteristics

Status	Min. value	Typical value	Max. value
Operating	-30℃	25℃	75℃
Extended	-40℃	25℃	85℃
Storage	-40℃	25℃	90℃

6.3 ESD Protection Characteristics

During the process of R&D, production testing, assembly, and transportation, electronic products may discharge the product through some means, which may cause damage to the module, so the ESD protection design of the product is very important. The following items are the electrostatic protection capabilities of the main pins of the module. When designing related products, you need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25 ℃

Table 6-4 N77-GL ESD protection characteristics

Contact point	Contact discharge	Air discharge
GND	±8 kV	±15 kV
ANT (outer shell)	±8 kV	±15 kV
Shielding cover	±8 kV	±15 kV

7 RF Characteristics

N77-GL provides connectivity on GSM, WCDMA, FDD-LTE (Cat4), TDD-LTE (Cat4) networks.

This chapter describes mechanical characteristics of the N77-GL module.

7.1 Operating Frequency Bands

Table 7-1 N77-GL operating frequency bands

Operating frequency band	Uplink	Downlink
GSM850	824 - 849 MHz	869 - 894 MHz
EGSM900	880 - 915 MHz	925 - 960 MHz
DCS1800	1710 - 1785 MHz	1805 - 1880 MHz
PCS1900	1850 - 1910 MHz	1930 - 1990 MHz
WCDMA B1	1920 - 1980 MHz	2110 - 2170 MHz
WCDMA B2	1850 - 1910 MHz	1930 - 1990 MHz
WCDMA B5	824 - 849 MHz	869 - 894 MHz
WCDMA B8	880 - 915 MHz	925 - 960 MHz
FDD-LTE B1	1920 - 1980 MHz	2110 - 2170 MHz
FDD-LTE B2	1850 - 1910 MHz	1930 - 1990 MHz
FDD-LTE B3	1710 - 1785 MHz	1805 - 1880 MHz
FDD-LTE B4	1710 - 1755 MHz	2110 - 2155 MHz
FDD-LTE B5	824 - 849 MHz	869 - 894 MHz
FDD-LTE B7	2500 - 2570 MHz	2620 - 2690 MHz
FDD-LTE B8	880 - 915 MHz	925 - 960 MHz
FDD-LTE B12	699 - 716 MHz	729 - 746 MHz
FDD-LTE B13	777 - 787 MHz	746 - 756 MHz
FDD-LTE B17	704 - 716 MHz	734 - 746 MHz
FDD-LTE B18	815 - 830 MHz	860 - 875 MHz
FDD-LTE B19	830 - 845 MHz	875 - 890 MHz
FDD-LTE B20	832 - 862 MHz	791 - 821 MHz

FDD-LTE B26	814 - 849 MHz	859 - 894 MHz
FDD-LTE B28	703 - 748 MHz	758 - 803 MHz
FDD-LTE B66	1710 - 1780 MHz	2110 - 2180 MHz
TDD-LTE B34	2010 - 2025 MHz	2010 - 2025 MHz
TDD-LTE B38	2570 - 2620 MHz	2570 - 2620 MHz
TDD-LTE B39	1880 - 1920 MHz	1880 - 1920 MHz
TDD-LTE B40	2300 - 2400 MHz	2300 - 2400 MHz
TDD-LTE B41	2496 - 2690 MHz	2496 - 2690 MHz

7.2 TX Power and RX Sensitivity

Table 7-2 N77-GL RF transmitting power

Band	Max Power	Min. Power
GSM850	33 dBm ± 2 dB	5 dBm±5 dB
EGSM900	33 dBm ± 2 dB	5 dBm±5 dB
DCS1800	30 dBm ± 2 dB	0 dBm±5 dB
PCS1900	30 dBm ± 2 dB	0 dBm±5 dB
WCDMA B1	24 dBm+1/-3 dB	< -50 dBm
WCDMA B2	24 dBm+1/-3 dB	< -50 dBm
WCDMA B5	24 dBm+1/-3 dB	< -50 dBm
WCDMA B8	24 dBm+1/-3 dB	< -50 dBm
FDD-LTE B1	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B2	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B3	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B4	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B5	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B7	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B8	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B12	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B13	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B17	23 dBm ± 2 dB	< -39 dBm

FDD-LTE B18	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B19	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B20	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B26	23 dBm ± 2 dB	< -39 dBm
FDD LTE B28	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B66	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B34	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B38	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B39	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B40	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B41	23 dBm ± 2 dB	< -39 dBm

Table 7-3 N77-GL RF RX sensitivity

Band	RX sensitivity
GSM850	≤ -107 dBm
EGSM900	≤ -107 dBm
DCS1800	≤ -107 dBm
PCS1900	≤ -107 dBm
WCDMA B1	≤ -107 dBm
WCDMA B2	≤ -107 dBm
WCDMA B5	≤ -107 dBm
WCDMA B8	≤ -107 dBm
FDD-LTE B1	≤ -97 dBm
FDD-LTE B2	≤ -95 dBm
FDD-LTE B3	≤ -94 dBm
FDD-LTE B4	≤ -97 dBm
FDD-LTE B5	≤ -95 dBm
FDD-LTE B7	≤ -95 dBm
FDD-LTE B8	≤ -94 dBm
FDD-LTE B12	≤ -94 dBm
FDD-LTE B13	≤ -94 dBm
FDD-LTE B17	≤ -94 dBm

FDD-LTE B18	≤ -97 dBm
FDD-LTE B19	≤ -97 dBm
FDD-LTE B20	≤ -94 dBm
FDD-LTE B26	≤ -94.5 dBm
FDD-LTE B28	≤ -95.5 dBm
FDD-LTE B66	≤ -96.5 dBm
TDD-LTE B34	≤ -97 dBm
TDD-LTE B38	≤ -97 dBm
TDD-LTE B39	≤ -97 dBm
TDD-LTE B40	≤ -97 dBm
TDD-LTE B41	≤ -95 dBm

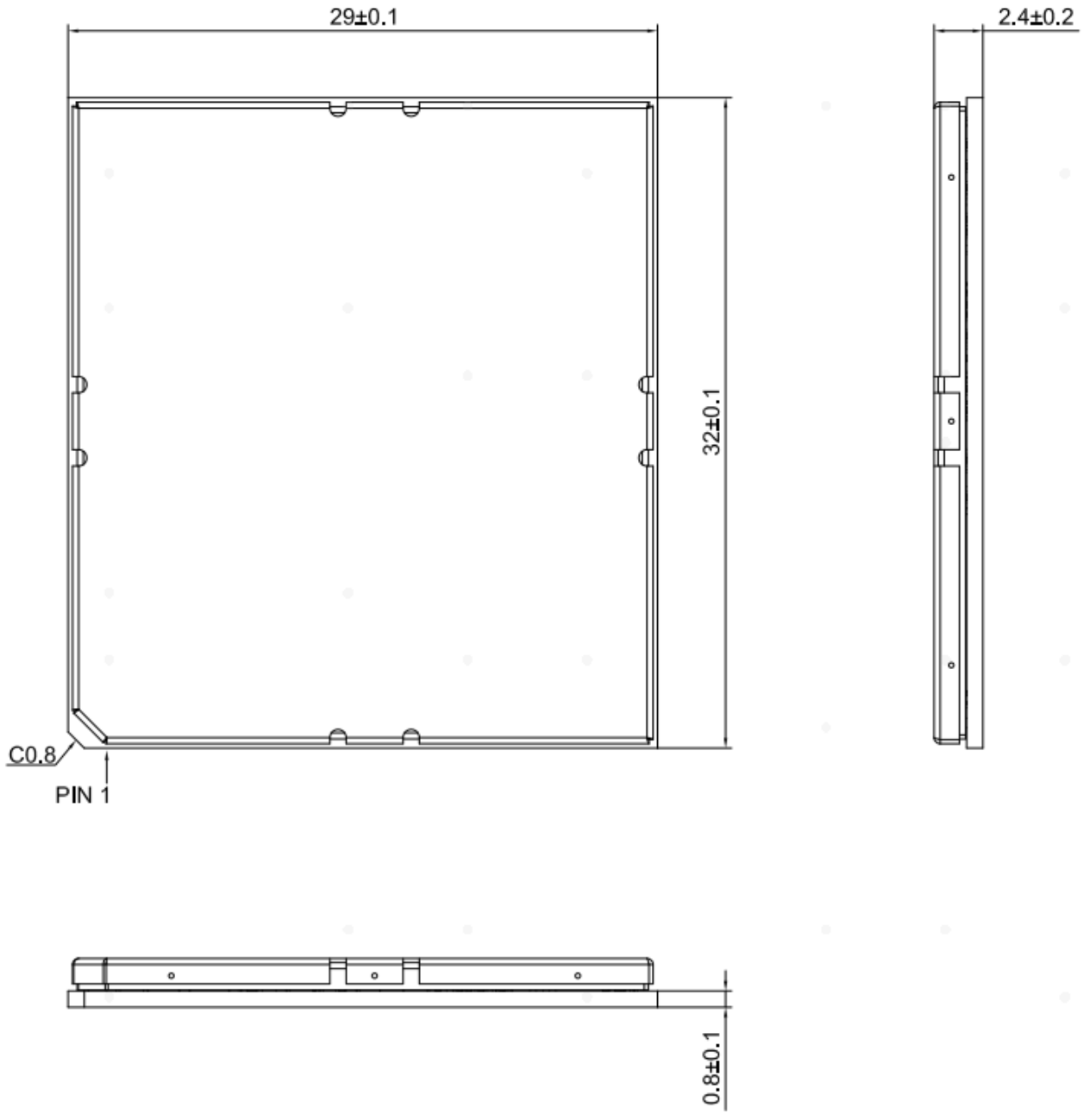
The values above are test data obtained in a lab environment. LTE results are tested under a 10 MHz bandwidth. Actual performance may vary due to network conditions.

8 Mechanical Characteristics

This chapter describes mechanical characteristics of the N77-GL module.

8.1 Dimensions

Figure 8-1 N77-GL Top and side view dimensions (unit: mm)



8.2 Labeling

The label information is laser carved on the cover. The following figure shows the label of N77-GL.

The preceding label is for reference only, the actual effect is subject to the actual product.

8.3 Packaging

The N77-GL module undergos reflow soldering through Surface Mount Technology (SMT) and is susceptible to moisture throughout its lifecycle, from manufacturing to end-user application. To mitigate moisture-related risks, the modules are delivered in trays and packaged in vacuum-sealed aluminum foil bags, complete with Silica gel desiccants and a humidity indicator card.

8.3.1 Tray

Neoway modules are packed in the following method, which enables efficient production.

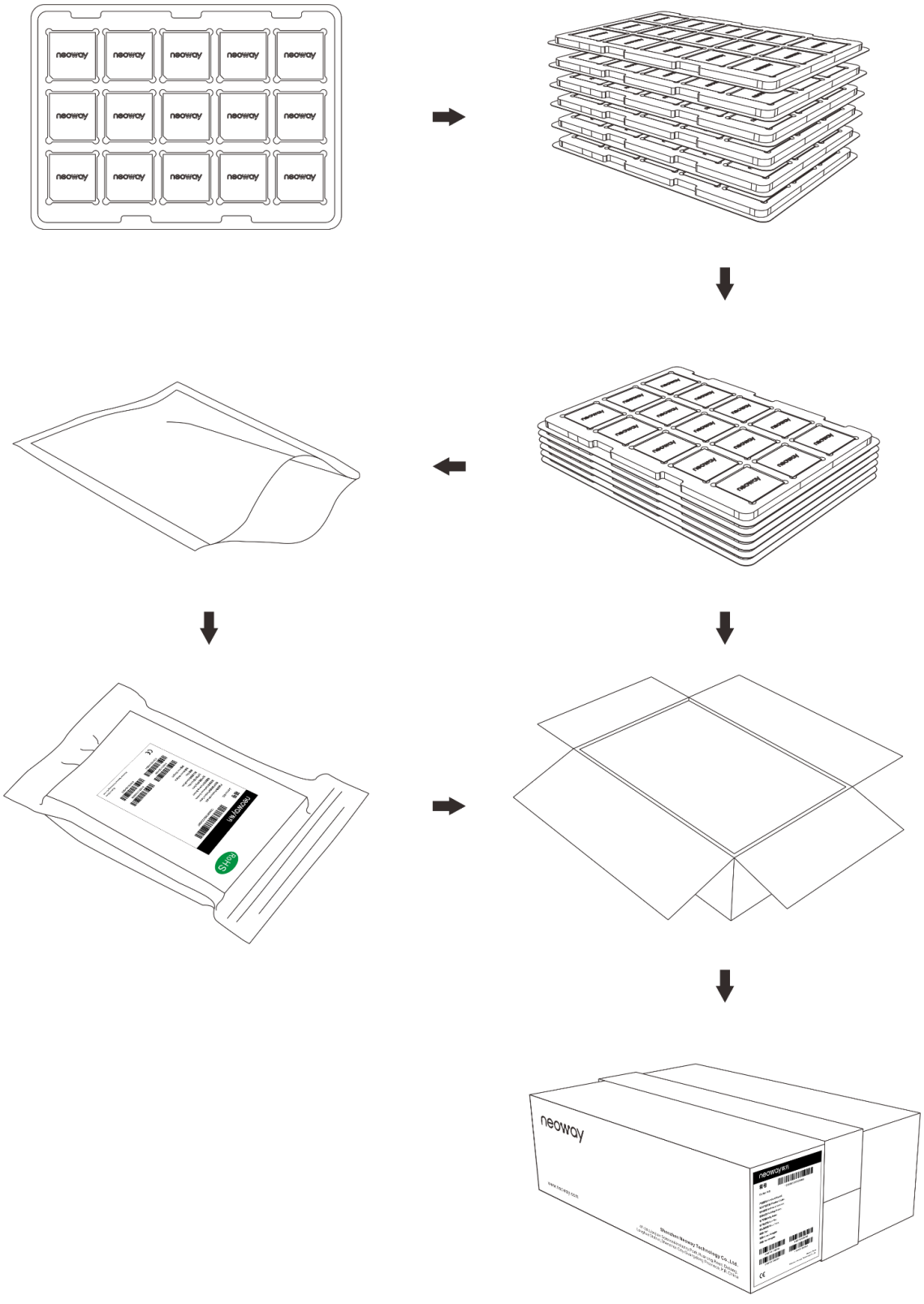
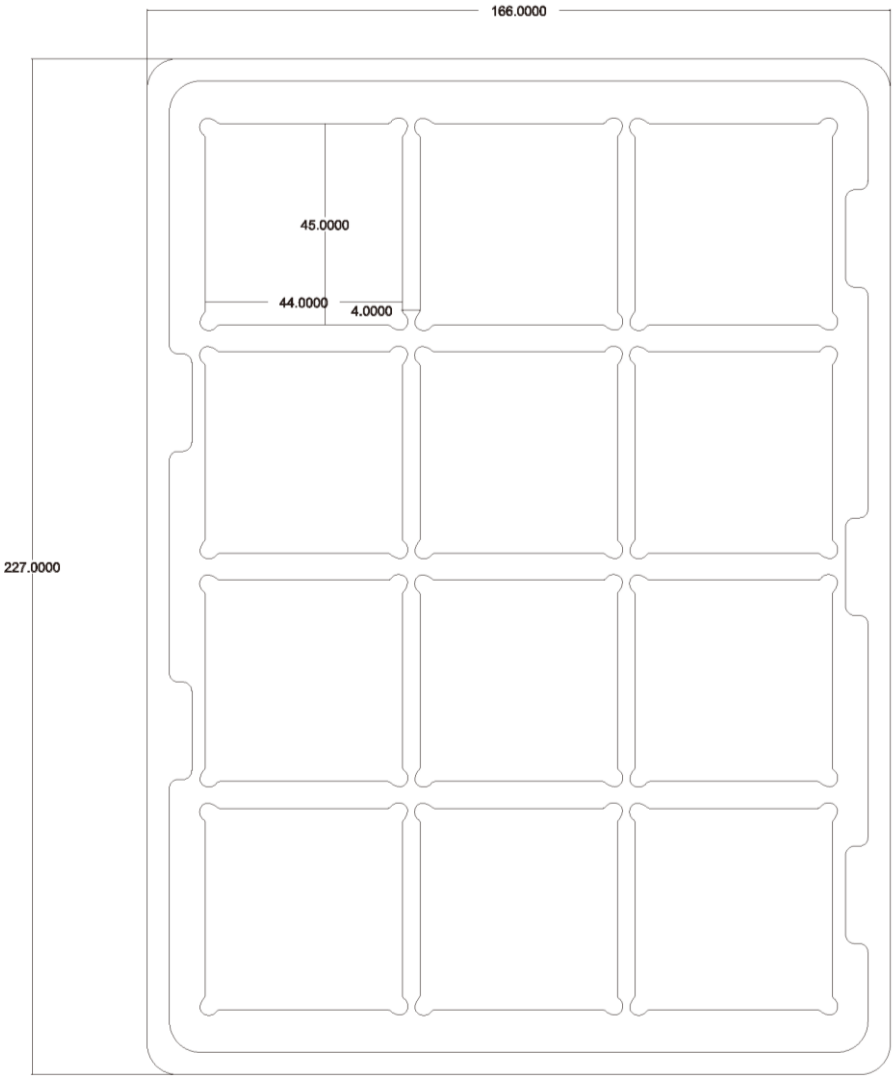
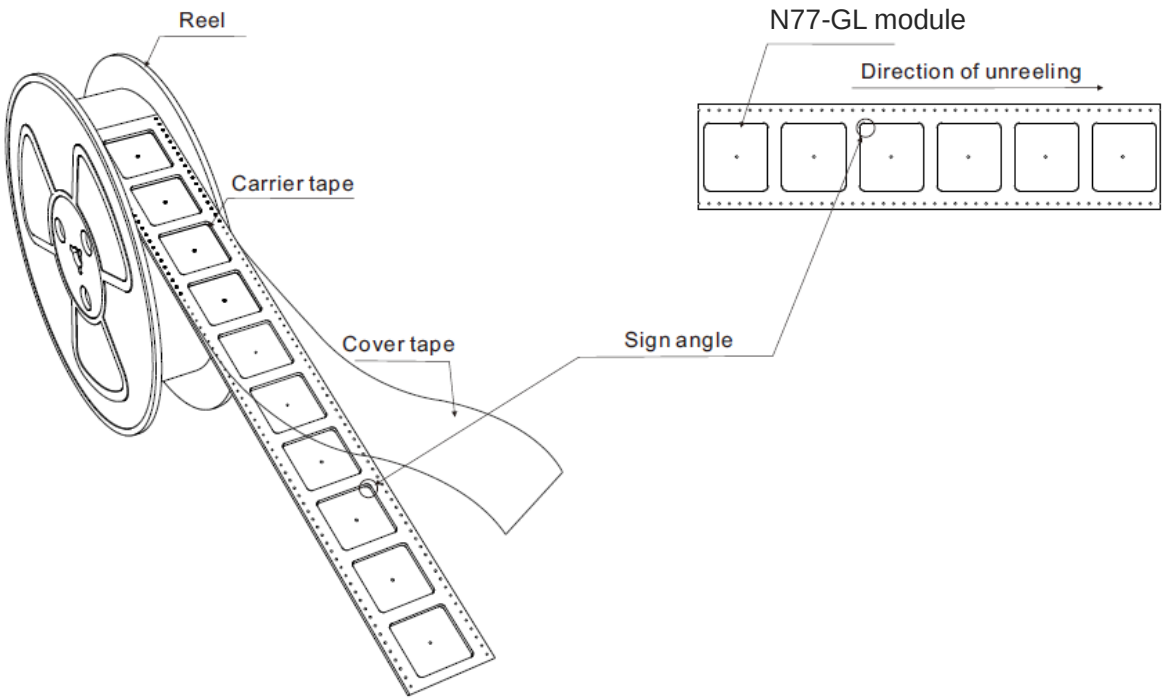

neoway
N77-GL
Shrink
neoway
www.neoway.com

Figure 8-2 Tray details

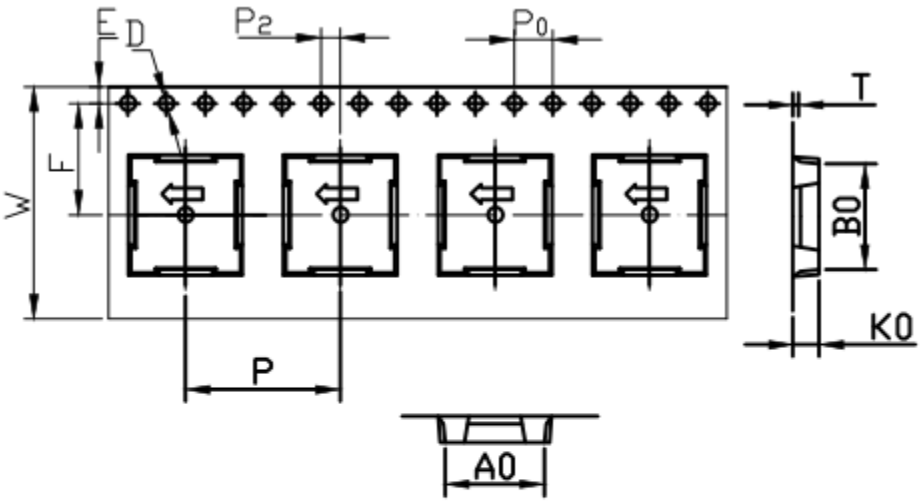


8.3.2 Tape&Reel

Neoway modules are delivered as reeled tapes as shown below:

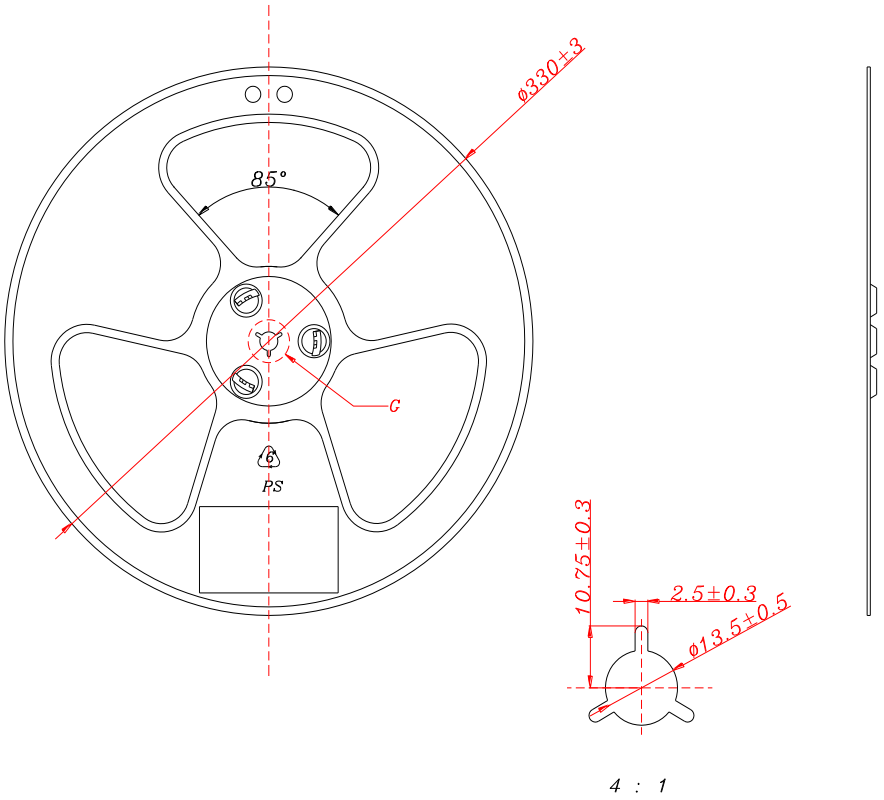


Tape Dimensions



ITEM	W	A0	B0	K0	K1	P	F	E	D	D1	P0	P2
DIM	24.0 +0.30 -0.10	10.1 +0.10 -0.10	11.0 +0.10 -0.10	2.7 +0.10 -0.10	0.00 +0.10 -0.10	16.0 +0.10 -0.10	11.5 +0.10 -0.10	1.75 +0.10 -0.10	1.50 +0.10 -0.00	0.00 +0.25 -0.00	4.00 +0.10 -0.10	2.00 +0.10 -0.10

Reel Dimensions



8.3.3 Moisture Sensitivity Level

N77-GL is a level 3 moisture-sensitive electronic element, in compliance IPC/ JEDEC J-STD-020 standard.

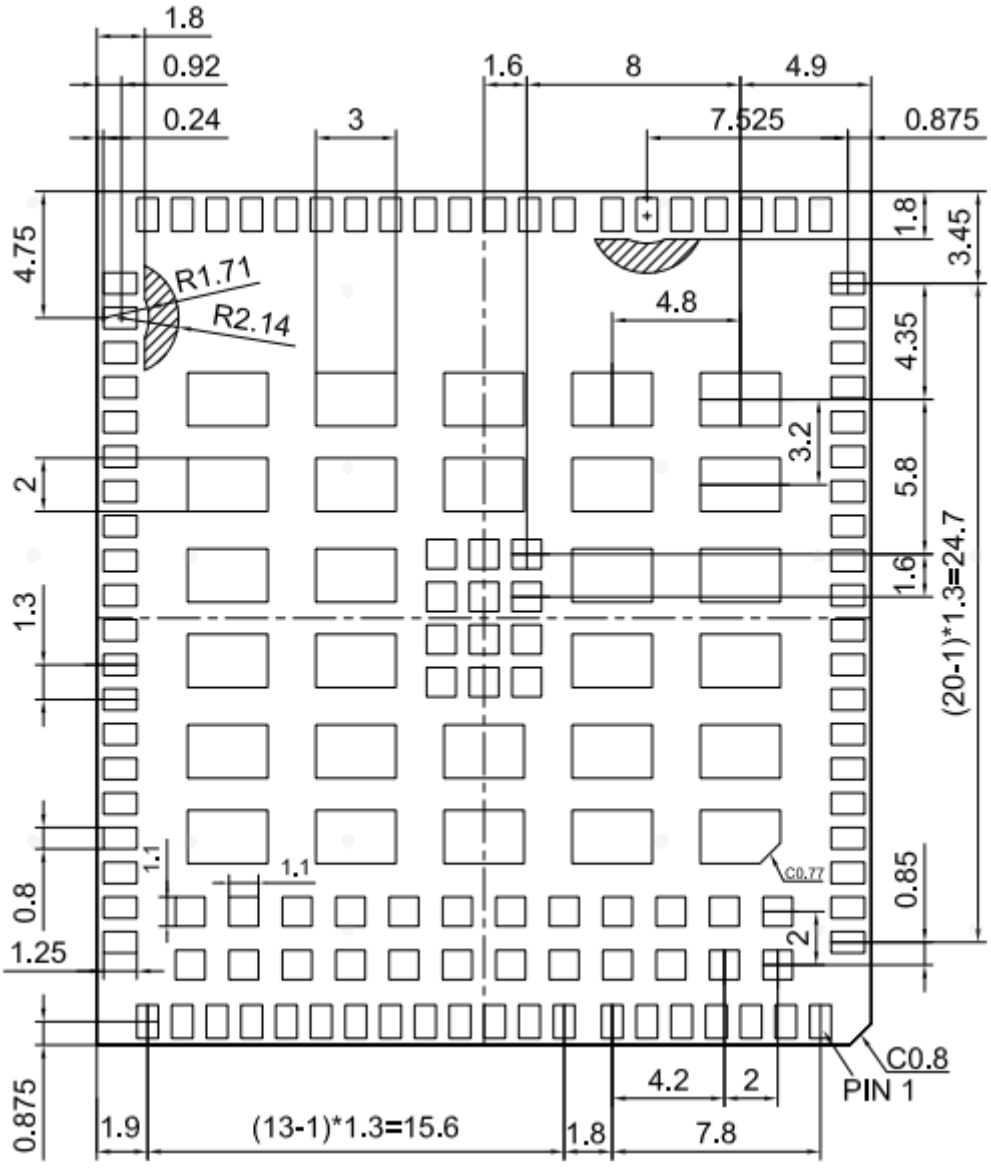
After unpacking, avoid leaving the module exposed to air for too long. If exposed to air for a prolonged period, the module could become damp, increasing the risk of damage during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at temperatures higher than 90 degrees for more than 12 hours. In addition, since the package tray is made of non-high temperature resistant material, do not bake modules with the package tray directly.

9 Mounting N77-GL onto Application Board

This chapter describes the module PCB package and application PCB package of N77-GL, as well as the key points of SMT related technology.

9.1 PCB Package

Figure 9-1 Bottom view of N77-GL PCB package (unit: mm)

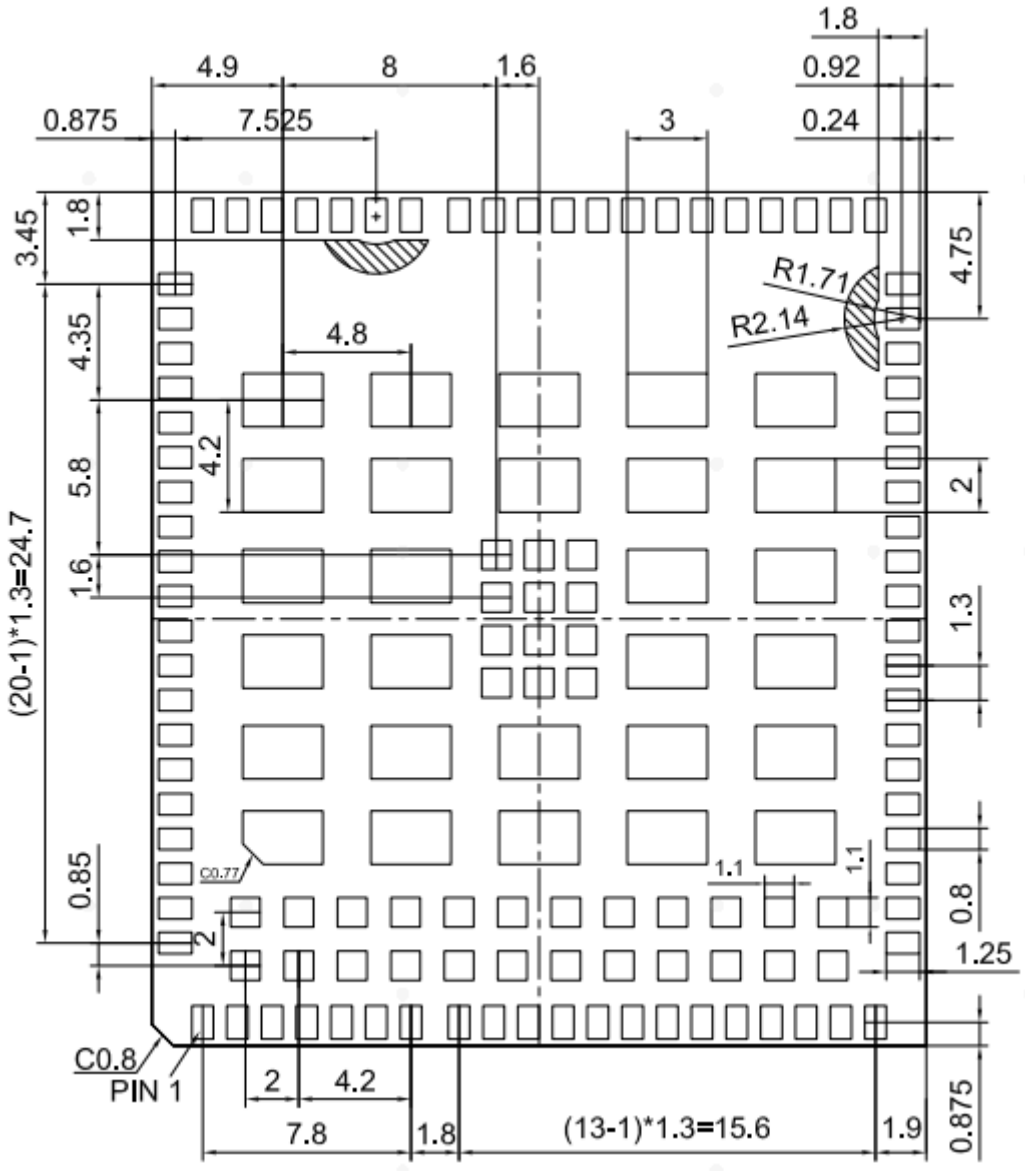


9.2 Application PCB Package

The N77-GL module has a total of 144 pins in LGA package, and the recommended application PCB package is as follows:

- To ensure proper operation of the module, only GND via-holes and copper pouring are allowed within the shaded area "▨" of the PCB package.
- To achieve higher yield during module production, it is recommended that the distance between other components on the PCB board and the module pads be at least 3 mm to avoid the risk of tin connection when using stepped stencil.

Figure 9-2 Top view of Application PCB package (unit: mm)



9.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

9.4 Solder Paste

The thickness of solder paste and the flatness of PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

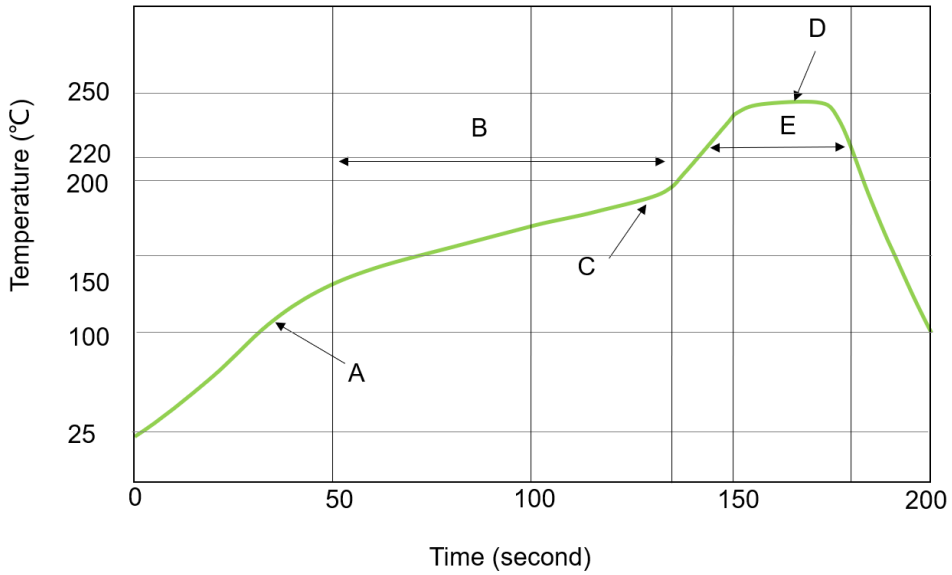
- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LCC/LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the time above 220°C (reflow temperature) exceeds 45 seconds and the peak temperature does not exceed 240°C.

9.5 Oven Temperature Profile

If the PCB is large, it is important to avoid bending of the printed circuit material during an SMT process. So a bending prevention tool must be placed on the bottom of the printed circuit board. It is recommended to use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Due to abnormal temperatures, thermal sensitive devices may fail and cause other adverse effects. Neoway assumes no responsibility for such consequences.

Figure 9-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4°C/sec
- Ramp down rate: -3 to -1°C/sec
- Soaking zone: 150 - 180°C, Time: 60 - 100s
- Reflow zone: >220°C, Time: 40 - 90s
- Peak temperature: 235 - 245°C

For information about cautions in storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When manually removing a module from your application's PCB board, it is important to use heat guns with large openings. Adjust the temperature to about 245°C (depending on the type of solder paste used) and heat the module until the solder paste melts. Use tweezers to remove the module, being careful not to shake it at high temperatures. Shaking the module may cause components inside to become misplaced.

A Abbreviations

Abbreviation	Full name
ADC	Analog-to-Digital Converter
AI	Analog Input
ARM	Advanced RISC Machine
bps	Bits per Second
CS	Chip Select
CTS	Clear to Send
DC	Direct Current
DCS	Digital Cellular System
DI	Digital Input
DL	Downlink
DO	Digital Output
DRX	Discontinuous Reception
DNI	Do Not Installed
EGSM	Enhanced GSM
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance
EVK	Evaluation Kit
FDD	Frequency Division Duplexing
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
3GPP	3rd Generation Partnership Project
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
IO	Input/Output
LED	Light Emitting Diode
LGA	Land Grid Array

LTE	Long Term Evolution
MCLK	Main Clock
MCU	Microcontroller Unit
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage
WiFi	Wireless Fidelity
WCDMA	Wide-band Code Division Multiple Access
WLAN	Wireless Local Area Network

