HID CORPORATION

# End Item Specification – 4041A Rev A
# EProx Lock Module (eProxL)

# Table Of Contents

# 1. eProxL - Product Description

## 1.1 Scope

This document describes the physical characteristics, functional requirements and software features contained in the eProxL. The eProxL was developed for the single door proximity reader system market. This document also contains the product specifications, which include performance, environmental, regulatory, and operational criteria.

## 1.2 Functional Summary

The eProxL reader is a low power RFID reader intended for use as an access-control component in battery-powered stand-alone electronic door lock systems. When installed into a door lock system, the user need only present an HID proximity card to the vicinity of the eProxL reader antenna in order to open the locked door.

The eProxL reader normally operates in a low-power sleep mode until a transponder (ProxCard) is brought near. The reader then activates for a brief time and reads the data from the transponder. The ID data is sent as a serial bit stream to the OEM's lock controlling board. The OEM board can then compare the card data to a database of ID's which are authorized to open the door lock.

## 1.3 Reference Documents

The following Standards have been achieved or applied for on previous HID RFID Readers and are for reference only:

> Security Industries Association 26-Bit Reader Interface Standard
> "UL 294 Underwriters Laboratories Recognized Component

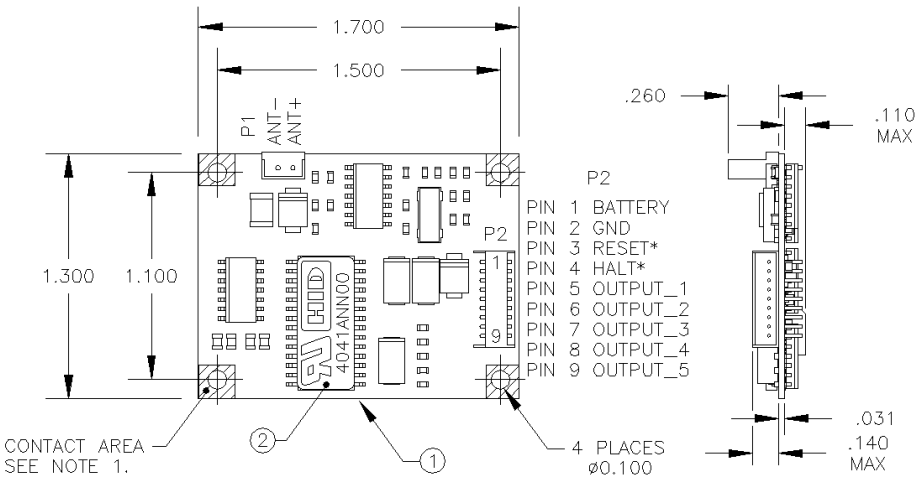
# 2. Physical Characteristics

## 2.1 Product Identification

The HID model number is 4041A - for the eProxL.

## 2.2 eProxL Dimensions

### 2.2.1 Final Assembly




TOLERANCES: .XXX= .020

NOTE:

1. CONTACT AREA AVAILABLE (BOTH SIDES OF PWB): .105 SQUARE FROM CENTER OF HOLE FOR METAL HARDWARE, .130 SQUARE FOR NON−METAL HARDWARE.

FIG. 1

This figure represents the EProxL standard configuration.

## 2.3 Product Packaging

Each unit shall be packaged in a static resistant bag, and marked with:

- Model number
- Date code
- Serial number

### 2.3.1 Packaging Notes

Unless otherwise specified:

1) Affix Item 2 (label) to Item 1 (final assembly).
2) Place Item 1 (final assembly) into Item 3 (anti-static bag).
3) Include Item 4 (installation manual) with bagged Item 1 (final assembly) prior to shipping.

## 2.4 eProxL Reader Connections

All outputs from the eProxL Reader are open-collector. Passive or active pullups are to be provided by the OEM host controller board.

The EProxL Reader provides a 1K Ohm pullup resistor for RESET* input, and a 10K Ohm pullup resistor for the HALT* input.

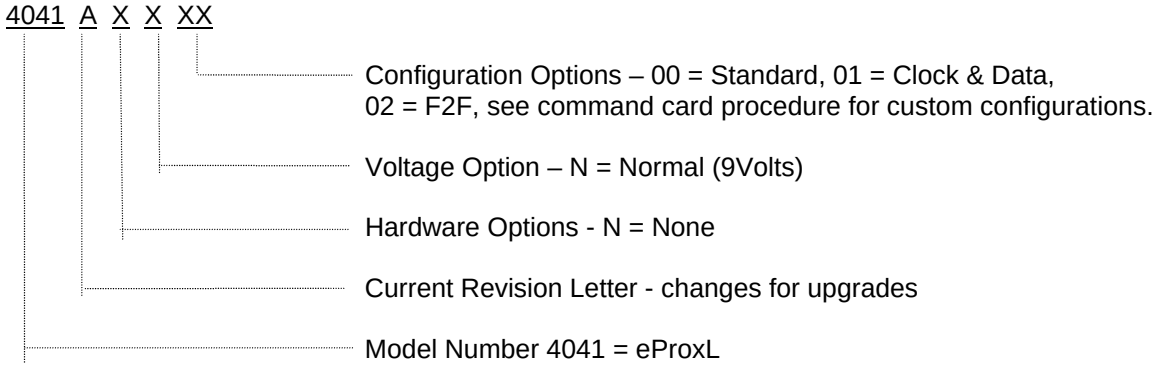
***P1***

| PIN | Signal Name | Signal Direction | Description |
|---|---|---|---|
| P1-1 | Antenna + | - | Antenna connection |
| P1-2 | Antenna - | - | Antenna connection |

***P2***

| PIN | Signal Name | Signal Direction | Description |
|---|---|---|---|
| P2-1 | V+ | Input to unit | DC power: (Battery or regulated by OEM host.) |
| P2-2 | GROUND | - | Signal and DC power common |
| P2-3 | RESET* | Input to Reader | Active Low, resets eProxL microprocessor |
| P2-4 | HALT* | Input to Reader | Active Low, inhibits eProxL read mode |
| P2-5 | OUTPUT 1 | Output from unit | Active Low, function depends on output protocol |
| P2-6 | OUTPUT 2 | Output from unit | Active Low, function depends on output protocol |
| P2-7 | OUTPUT 3 | Output from unit | Active Low, function depends on output protocol |
| P2-8 | OUTPUT 4 | Output from unit | Active Low, function depends on output protocol |
| P2-9 | OUTPUT 5 | Output from unit | Active Low, reset test signal, also active low in normal operation while unit is in active mode |

## 2.5 Product Configuration/Ordering Options




- Standard Part Number = 4041ANN00 is a eProxL with no (N)none hardware options, (N)9V normal operating voltage, and (00)standard wiegand, configuration options.

# 3. Product Specifications

## 3.1 Environmental Characteristics

- Operating Temperature Range ..... -30°C to 65°C (-22°F to 150°F)
- Storage Temperature Range ..... -40 C to 85 C (-40 F to 185 F)
- Operating Humidity Range ..... 5% to 95% non-condensing
- Operating Vibration Limit ..... 0.04 g2/Hz 20-2000Hz
- Operating Shock Limit ..... 30g, 11mSec, Half Sine

## 3.2 Power Requirements

- Supply Voltage ..... 4.0VDC – 10.0VDC
- Supply Current ..... 30uA max (wake up circuit, averaged over 1 second) – 50mA max (RF CardRead)

## 3.3 Operating Parameters

- Excitation Frequency ..... 125KHz
- Tag Read Time ..... 150mSec (typical)
- Report Time ..... format dependent
- Read Distance ..... 1.0" (antenna dependent)
- Wakeup Circuit Power Requirement ..... 30uA max
- Active Circuit Power Requirement ..... 50 mA max

## 3.4 Accuracy

The unit will not have more than 1 miss-read per 10 million.

# 4. eProxL Reader Functional Description

The RF reader shall acquire and output tag data from the FSK programmed RFID IC based tags. The firmware in the RF Reader will be programmed to interface with the Single Door Host in one of several selectable output formats (open collector signals).

## 4.1 Configuration Option chart

| Configuration option # | Description |
|---|---|
| 00 | Wiegand Output, Default timing, Long Range Search, All Customer Codes |
| 01 | Clock & Data Output, Default timing, Long Range Search, All Customer Codes |
| 02 | F2F Output, Default timing, All Customer Codes |

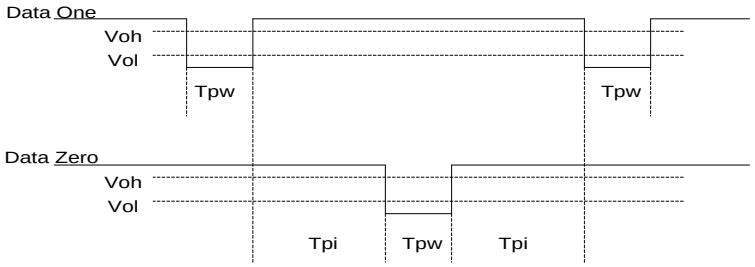
*Contact HID sales for Custom Configuration Options.
**EEPROM configuration options available. Contact Technical Support for more information.

## 4.2 Wiegand Output

| Outputs | Description |
|---|---|
| Output 1 – Card -Valid | Active low signal indicates successful transponder read. |
| Output 2 – Data 0 | Active low signal carries transponder data information. |
| Output 3 – Data1 | Active low signal carries transponder data information. |

### 4.2.1 Data Pulses - Wiegand

The Data One and Data Zero signals are normally held at a logic high level until the reader is ready to send a data stream. The reader places asynchronous low pulses on the appropriate data lines to transmit the data stream to the panel. The following timing parameters shall be observed:



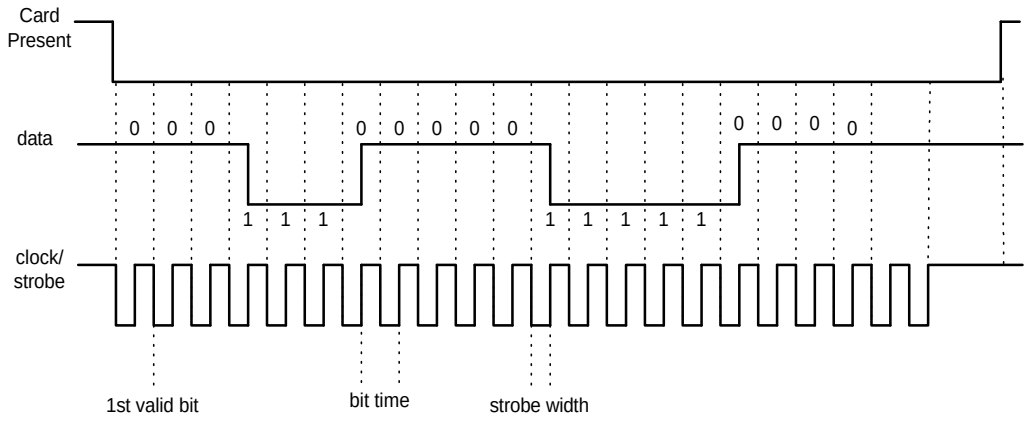

- Tpw Pulse Width Time - 35µSec (minimum) to 80µSec (maximum), 50µSec (typical)
- Tpi Pulse Interval Time – .750mSec (minimum) to 1.30mSec (maximum), 1mSec (typical)

## 4.3 Clock and Data Output

| Output | Description |
|---|---|
| Output 1 = Card Present | Active low signal indicates successful transponder read. |
| Output 2 = Data | Active low signal carries transponder data information |
| Output 3 = Clock | Active low signal, data is valid on falling edge of this signal. |

### 4.3.1 Data Pulse – Clock and Data

- bit time = 1.5 mSec (default)
- **Clock** strobe width = bit time/3 (33% of bit time), default = 500 uSec
- **Clock** is valid 1.5 mSec (one clock cycle, min) after **Card Present** is asserted
- **Data** is valid 10 uSec (min) before the negative edge of **Clock**
- **Card Present** returns to the high level a configurable delay after the last clock/strobe.



### 4.3.2 Clock & Data Output – message content

The content of the of ABA clock and data message is:

<Preamble><Start Sentinel><data digit 1>..<data digit n><End sentinel><LRC><Postamble>

where

<Preamble> = 10 zero bits (minimum) + configurable number of additional zero bits
<Start Sentinel> = 4 bit character, hexadecimal 'B', LSB first, followed by ODD parity bit
= $<S_0><S_1><S_2><S_3><S^c>$
= 11010 (transmitted left to right)

<data digit> = 4 bit BCD character, LSB first, followed by Odd parity bit
= $<d^k_0><d^k_1><d^k_2><d^k_3><p^k>$ for $k^{th}$ data digit

where $<p^k> = <d^k_0> + <d^k_1> + <d^k_2> + <d^k_3> + 1$

<End Sentinel> = 4 bit character, hexadecimal 'F', LSB first, followed by ODD parity bit
= $<F_0><F_1><F_2><F_3><F^c>$
= 11111

<LRC> = longitudinal checkword
= 4 bit word of even parity check over corresponding bits, followed by Odd parity bit over preceding LRC bits only.
= $<c_0><c_1><c_2><c_3><p^c>$

where $<c_0> = <d^1_0> + <d^2_0> + <d^3_0> + ... <d^n_0> + <S_0> + <F_0>$
$<c_1> = <d^1_1> + <d^2_1> + <d^3_1> + ... <d^n_0> + <S_1> + <F_1>$
$<c_2> = <d^1_2> + <d^2_2> + <d^3_2> + ... <d^n_0> + <S_2> + <F_2>$
$<c_3> = <d^1_3> + <d^2_3> + <d^3_3> + ... <d^n_0> + <S_0> + <F_3>$
$<p^c> = <c_0> + <c_1> + <c_2> + <c_3> + 1$

where all sums above are modulo 2 sums (EXCLUSIVE OR)

<Postamble> = 10 zero bits (minimum) + configurable number of additional zero bits

The data digit bits are determined from the card data bits in a manner dependent on the card's customer codes. There are two cases:

1) Customer code 74 is a 36 bit format consisting of 9 BCD digits. The first 8 digits are data digits, with the last digit being the LRC. The Reader inserts the preamble leading zeroes, then inserts the start sentinel. The eight data digits are sent, then the reader inserts the end sentinel. The LRC is then transmitted, and the postamble trailing zero bits are appended by the Reader firmware

2) For all other formats, the card bitstream is taken 3-bits at a time. The 37 data bits are broken into octal digits as follows: The first data bit becomes the LSB of the first digit. The other bits of the first digit are cleared to zero. All succeeding bits are taken 3 at a time, with the first bit of each group of three becoming the MSB of an octal digit, and the last of each group of three becoming the LSB of that octal digit. The bits are then transmitted as 13 equivalent BCD digits with parity appended.

For reasons of backward compatibility the bitstream has 3 leading BCD "zero" digits transmitted, for a total of 16 BCD data digits.

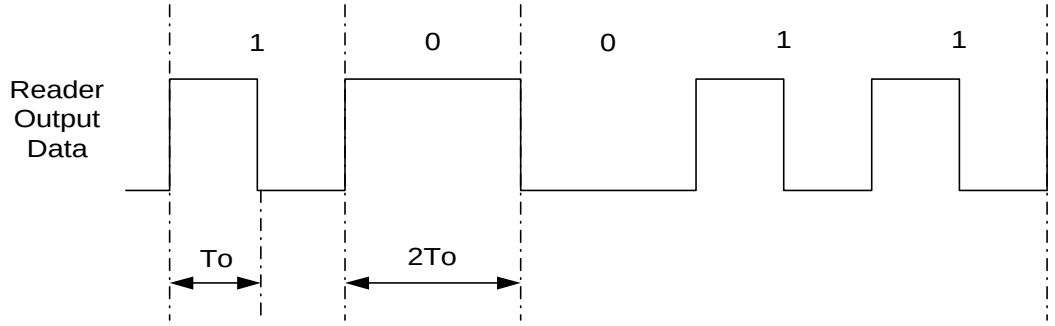
The preamble leading zeroes, start sentinel, end sentinel, LRC, and postamble trailing zeroes are all inserted by the Reader firmware and are not part of the programmed bits on the card.

## 4.4 F2F Output

| Output | Description |
|---|---|
| Output 1 = Card Present | Active low signal indicates successful transponder read. |
| Output 2 = Data | Active low signal carries transponder data information |

### 4.4.1 Data Pulse - F2F

- **Card Present** goes low a configurable time before first data edge
- bit period = 1.0 mSec (default)
- phase toggles at beginning of every bit period
- data 0 is represented by 1/2 cycle of 500 Hz
- data 1 is represented by 1 cycle of 1 KHz
- **Card Present** returns to quiescent high condition a configurable delay after last data edge




### 4.4.2 F2F Output – message content

The message content is identical to that to that described in section 4.3.2.