Circuit Explanations

2 Technical description

2.1 Block diagram

The LMX4268 transceivers require only a few external circuits. The block diagram in figure 1 represents the RTX RF module. The baseband controller (NSC SC14408) controls the LMX by a Microwire interface and by other baseband signals. The interface is described in detail in section 2.7.

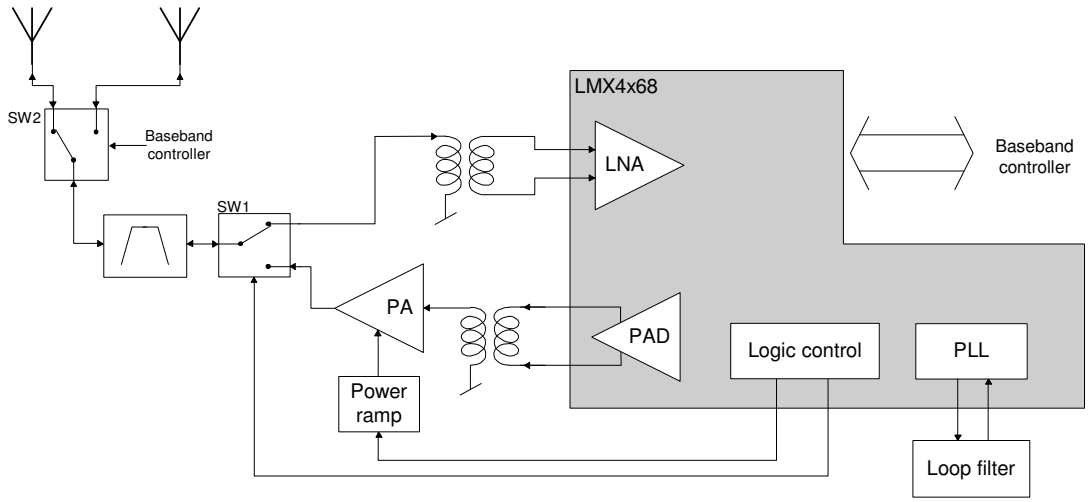

Figure 1. Block diagram of RF module employing the LMX4268. Only two logic ports are used in the Reference Design Kit.

The four logic ports are capable of controlling auxiliary circuits, such as activating the power amplifier (PA) and controlling the RX/TX switch. If preamble antenna diversity is to be employed, the baseband processor should control the antenna switches. Both the PA-driver and the LNA require balanced signals. Baluns must be placed at the LNA input and the PA driver output.
It is recommended to have the schematics of the RTX module at hand before proceeding.

2.2 Front-end

The RTX RF module has two antenna ports. Two PIN diodes controlled by the baseband processor are used for routing the desired antenna to the RX/TX path. Preamble antenna diversity, also known as fast antenna diversity, is supported by this solution. The LMX4268 also features built-in preamble antenna diversity, and has two output ports for driving the antenna switches. Using the bidirectional microwire interface, it can be read-back which antenna was chosen for a receive slot. That same antenna is usually selected for the following transmit slot. Mounting options determine the diversity function of the Kit.

RX/TX switching is accomplished using two PIN diodes, one in the signal line from the power amplifier, and a shunt diode placed a quarter of a wavelength towards the LNA. Logic ports on the transceiver control the diodes. When the two diodes are forward biased, the PA signal is routed towards the antennas, and the shunt diode shorts the signal to ground. However, the quarter-wave microstrip transforms this short into a high-impedance load. This construction has the advantage of very low loss and low power consumption in receive mode.

A band pass filter is used to protect the receiver from blocking signals and to attenuate certain spurious emissions, such as the 3rd and 4th harmonic of the VCO. For 2.4GHz ISM systems there are no formal requirements for receiver immunity to other systems. The LMX4268 receivers have some frequencies that are subject to blocking, namely the fundamental as well as the first harmonics of the VCO. Using band pass filters generally increases immunity to other systems, and gives a better product.

To control the power envelope in transmit mode, the power amplifier supply voltage is switched. A logic port on the transceiver activates the supply power to the power amplifier. The used power amplifier has integrated switching. Ramping up or down the PA is prone to cause transient emissions or even frequency offsets of the VCO. By proper ramping of the supply voltage transients can be avoided, and shielding the transceiver circuit isolates the VCO from the field surrounding the module.

2.3 PLL synthesizer

The integrated integer-N PLL uses the 10.368MHz clock signal supplied by the baseband chip as reference frequency. The phase detector operates at 432kHz, which gives a channel spacing of 864kHz, because the prescaler is connected to the VCO output at half the transmit frequency. Please refer to the data sheet for specific A- and B counter settings.

The synthesizer requires an external loop filter between the charge pump output and the VCO tune input. The lock-in time of the PLL and open-loop drift depends on this filter. The LMX4268 uses open-loop modulation, where the gaussian shaped transmit signal is applied directly to the VCO modulation input. This implies tri-stating the charge pump when transmitting a burst of data. This also conveniently prohibits the front-end from transmitting any spurious emissions generated by the synthesizer.

During the lock-in phase of the synthesizer, it is critical that the modulation input to the VCO is kept at the mean voltage of the modulation that will be applied during the actual transmission. If this is not the case, a frequency offset will be present. If the modulation input

of the VCO is not linear, it may be beneficial to modulate the VCO in the lock-in period with a pattern similar to the preamble (alternating zeroes and ones).

The 10.368MHz reference frequency is used by the digital circuitry as well as reference for the synthesizer. This means that the reference frequency cannot be switched off, even when the PLL is not active.

2.4 Power up, calibration and initialization

After power up or reset, the chip must be calibrated and initialized. Calibrating IF filter response and DC-offset at the ADC input compensates for manufacturing tolerances. The calibration is fully automatic in LMX4268.

2.5 Burst operation

Practically all timing during a transmit or receive burst is managed by “Switch instants” and the Dynamic Control Function (DCF) featured by the transceiver. All the different parts of the chip have their own programmable power controller. The logic ports are equivalent to these power controllers, with the exception that the polarity can be reversed on the logic ports. A burst is initiated by a start Burst-Mode Control Word (BMCW), and optionally ended by a stop BMCW. All timers are reset when issuing the start BMCW.

The DCFs have the following options:

- Power-up either when BMCW is issued, or after a programmable delay.
- Power-down either when stop BMCW is issued, or after a programmable delay.
- Any DCF can be activated for RX- or TX bursts only, or for both types of burst.

2.5.1 Preparing the LMX for a RX/TX burst

The only timing requirement for the baseband processor is the waiting for initialization and locking of the PLL, and then transmitting the TX-data or receiving RX-data at the right synchronization. If preamble diversity switching is to be implemented, the baseband processor must decide which antenna to use by monitoring RSSI levels.
The initialization sequence is as follows.

1. The BMCW is issued. All timers are reset. The following items are controlled by DCFs:
2. The bias, PLL and VCO is powered up.
3. The VCO is coarse tuned
4. The frequency doubler is powered up.

5. If an RX BMCW was issued, the LNA, mixer, IF, ADC, RSSI and demodulator is turned on. If a TX BMCW was issued, the PA driver is turned on.
6. The PLL loop is opened.
7. The RX/TX switch is activated, and the front-end PA is ramped up if in TX mode.

The transceiver is now ready for receiving or transmitting a burst.

2.5.2 Coarse tuning the VCO

The coarse tuning automatically determines the value of a capacitor bank such that the VCO runs at the programmed frequency, with a tune voltage close to the nominal tune voltage. This scheme also allows a lower k_{vco} because the tune voltage does not have to cover the entire band. This is an advantage especially for the LMX4268 operating in the 80MHz wide ISM band. The coarse tuning must be done before each burst.

2.5.3 Automatic frequency compensation (AFC)

The demodulator features an automatic frequency compensation that can extract the optimum slicing frequency from the preamble. The feature is referred to as 'active slice'. There are two methods for activating the AFC, either after a fixed delay from activating the demodulator or using the RSSI level as a trigger. The two methods are depicted in figure 2 below.

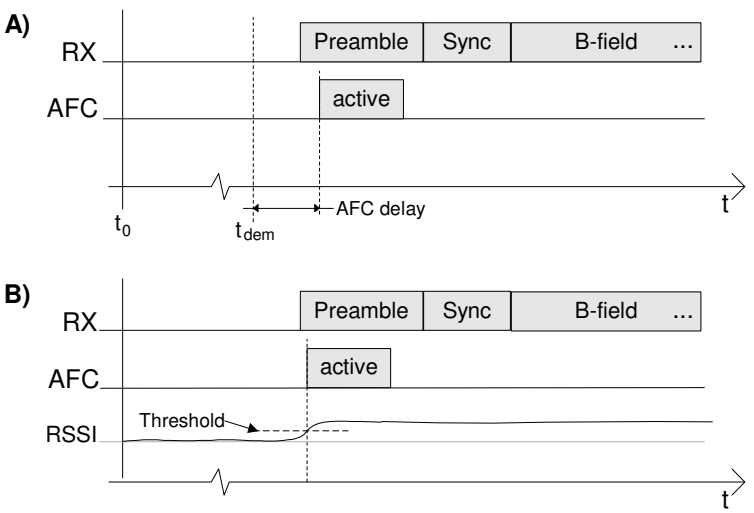

*Figure 2. **A**) Activating the AFC a fixed delay after activating the demodulator. **B**) Activating the AFC by triggering on the RSSI level.*

Method A in figure 2 is normally used, because the handset and fixed part are synchronized. The fixed *AFC delay* is chosen so that the AFC is active inside the preamble. If the handset

and fixed part are not synchronized, the AFC can be set up to activate on a trigger signal from the RSSI level. This method can however also be used when synchronized.

2.5.4 Alternative timing in 'search mode'

When a handset is not synchronized to a fixed part, it starts to search for a dummy bearer. In this search mode, it may be desirable to receive for a prolonged time, e.g. up to several milliseconds. To be able to do this, the chip must either be configured to keep receiving until as stop BMCW is issued, or the DCFs must be reprogrammed. The LMX4168/4268 can receive with the PLL locked, which enables infinite reception. This however requires reprogramming of several register banks, but it can shorten the search time significantly.

2.6 Power supply

All power supply lines should be decoupled close to the chip. The power amplifier draws up to 330mA or more in bursts, setting a demand for a stable supply.

2.7 Interfacing the LMX4268

The interface towards baseband consists of only a few connections. The only analog signals are the RSSI voltage and the transmit modulation signal. The connections are as follows:

- Power supply. The nominal supply voltage is 2.5V.
- Reset (active low). The chips must be reset after power-up.
- Reference clock. The clock reference used is 10.368MHz.
- Microwire bus. All the digital functions are programmed using this bus.
- TX modulation signal (Gaussian shaped FSK modulation)
- RX data
- RSSI voltage
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2.7.1 The Microwire bus

All setup and control of the transceiver is done via the Microwire bus. This three wire serial bus accepts 8 and 24 bit words, with the MSB transmitted first. Bits are clocked at rising edge, and the word is latched at rising edge. The clock is furthermore gated by the latch enable signal, so this signal must be kept low during transmission of a word.

2.7.2 DIP code example

An example of the DIP sub program for programming any of the registers in the LMX4268 is shown below (The registers are programmed by sending 3 bytes RAM contents through the Microwire bus.):

Antenna Switch, Bandpass-filter and RX/TX Switch

The antenna-diversity switch is constructed using two PIN diodes in one casing D301. DC biasing is achieved using quarter-wave transformers, which transform the short provided by capacitors C367, C368 and C369 into high-impedance loads. The antenna-diversity switch is controlled by the BMC (ANTSEL 0 and ANTSEL 1). A simple bandpass filter is implemented using capacitors C358, C359 and C361. The filter provides notches at the third and fourth harmonic of the VCO.

The RX/TX switch is implemented using two PIN diodes in one casing D300. DC biasing is achieved using quarter-wave transformers, which transform the short provided by capacitors C318 and C363. Isolation is improved in the RX-diode by making a notch-filter with C1 and L1. This is done to reduce frequency-offset of the transmitter.

PA supply and ramping.

The PA is supplied directly from the battery connector and is enabled by PA_ON from the LMX4268 (Port 0). The ramping is determined by the components C311 and R301.

Power Amplifier

The power amplifier needs external in- and output matching as well as DC feed at the output pins.

LNA balun

The coupler structure tuned with C319 transforms the single-ended signal from the front-end into a balanced signal for the LNA input.

PA driver balun (and supply)

The balanced PA drive signal is power-matched and transformed to a single-ended signal by the coupler structure tuned with C332. DC bias is provided to the outputs of the PA driver by the coupler as well, limited by R306.

10.368MHz reference clock filter

This filter can be used to reduce the voltage swing and the harmonics of the reference clock.

Loop filter

The loop filter is designed to achieve frequency lock in the time period after coarse tuning and before the burst starts.