Chipcon SmartRF® CC1000

# CC1000
# Single Chip Very Low Power RF Transceiver

## Applications

- *Very low power UHF wireless data transmitters and receivers*
- *315 / 433 / 868 and 915 MHz ISM/SRD band systems*
- *RKE – Two-way Remote Keyless Entry*
- *Home automation*
- *Wireless alarm and security systems*
- *AMR – Automatic Meter Reading*
- *Low power telemetry*
- *Toys*

## Product Description

**CC1000** is a true single-chip UHF transceiver designed for very low power and very low voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 315, 433, 868 and 915 MHz, but can easily be programmed for operation at other frequencies in the 300-1000 MHz range.

The main operating parameters of **CC1000** can be programmed via an easy-to-interface serial bus, thus making **CC1000** a very flexible and easy to use transceiver. In a typical system **CC1000** will be used together with a microcontroller and a few external passive components.

**CC1000** is based on Chipcon's SmartRF® technology in 0.35 µm CMOS.


## Features

- True single chip UHF RF transceiver
- Very low current consumption
- Frequency range 300 – 1000 MHz
- Integrated bit synchroniser
- High sensitivity (typical -110 dBm at 2.4 kBaud)
- Programmable output power –20 to 10 dBm
- Small size (TSSOP-28 package)
- Low supply voltage (2.1 V to 3.6 V)
- Very few external components required
- No external RF switch / IF filter required
- RSSI output
- Single port antenna connection
- FSK data rate up to 76.8 kBaud
- Complies with EN 300 220 and FCC CFR47 part 15
- FSK modulation spectrum shaping
- Programmable frequency in 250 Hz steps makes crystal temperature drift compensation possible without TCXO
- Suitable for frequency hopping protocols
- Development kit available
- Easy-to-use software for generating the **CC1000** configuration data

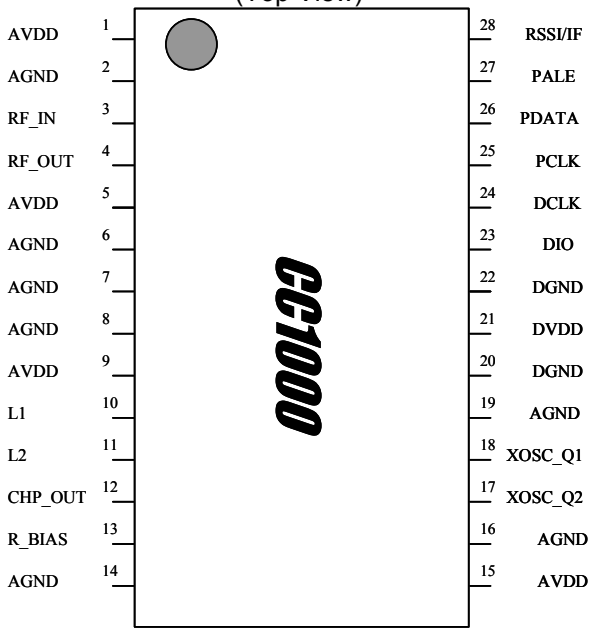
This document contains information on a pre-production product. Specifications and information herein are subject to change without notice.

## Pin Assignment

| Pin no. | Pin name | Pin type | Description |
|---|---|---|---|
| 1 | AVDD | Power (A) | Power supply (3 V) for analog modules (mixer and IF) |
| 2 | AGND | Ground (A) | Ground connection (0 V) for analog modules (mixer and IF) |
| 3 | RF_IN | RF Input | RF signal input from antenna |
| 4 | RF_OUT | RF output | RF signal output to antenna |
| 5 | AVDD | Power (A) | Power supply (3 V) for analog modules (LNA and PA) |
| 6 | AGND | Ground (A) | Ground connection (0 V) for analog modules (LNA and PA) |
| 7 | AGND | Ground (A) | Ground connection (0 V) for analog modules (PA) |
| 8 | AGND | Ground (A) | Ground connection (0 V) for analog modules (VCO and prescaler) |
| 9 | AVDD | Power (A) | Power supply (3 V) for analog modules (VCO and prescaler) |
| 10 | L1 | Analog input | Connection no 1 for external VCO tank inductor |
| 11 | L2 | Analog input | Connection no 2 for external VCO tank inductor |
| 12 | CHP_OUT (LOCK) | Analog output | Charge pump current output<br>The pin can also be used as PLL Lock indicator. Output is high when PLL is in lock. |
| 13 | R_BIAS | Analog output | Connection for external precision bias resistor (82 kΩ, ± 1%) |
| 14 | AGND | Ground (A) | Ground connection (0 V) for analog modules (backplane) |
| 15 | AVDD | Power (A) | Power supply (3 V) for analog modules (general) |
| 16 | AGND | Ground (A) | Ground connection (0 V) for analog modules (general) |
| 17 | XOSC_Q2 | Analog output | Crystal, pin 2 |
| 18 | XOSC_Q1 | Analog input | Crystal, pin 1, or external clock input |
| 19 | AGND | Ground (A) | Ground connection (0 V) for analog modules (guard) |
| 20 | DGND | Ground (D) | Ground connection (0 V) for digital modules (substrate) |
| 21 | DVDD | Power (D) | Power supply (3 V) for digital modules |
| 22 | DGND | Ground (D) | Ground connection (0 V) for digital modules |
| 23 | DIO | Digital input/output | Data input/output. Data input in transmit mode. Data output in receive mode |
| 24 | DCLK | Digital output | Data clock for data in both receive and transmit mode |
| 25 | PCLK | Digital input | Programming clock for 3-wire bus |
| 26 | PDATA | Digital input/output | Programming data for 3-wire bus. Programming data input for write operation, programming data output for read operation |
| 27 | PALE | Digital input | Programming address latch enable for 3-wire bus. Internal pull-up. |
| 28 | RSSI/IF | Analog output | The pin can be used as RSSI or 10.7 MHz IF output to optional external IF and demodulator. If not used, the pin should be left open (not connected). |

A=Analog, D=Digital

(Top View)



## Absolute Maximum Ratings

| Parameter | Min. | Max. | Units | Condition |
|---|---|---|---|---|
| Supply voltage, VDD | -0.3 | 5.0 | V | |
| Voltage on any pin | -0.3 | VDD+0.3, max 5.0 | V | |
| Input RF level | | 10 | dBm | |
| Storage temperature range | -50 | 150 | °C | |
| Operating ambient temperature range | -40 | 85 | °C | |
| Lead temperature | | 260 | °C | T = 10 s |

Under no circumstances the absolute maximum ratings given above should be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

***Caution!*** *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

## Electrical Specifications

Tc = 25°C, VDD = 3.0 V if nothing else stated

| Parameter | Min. | Typ. | Max. | Unit | Condition / Note |
|---|---|---|---|---|---|
| **Overall** | | | | | |
| RF Frequency Range | 300 | | 1000 | MHz | Programmable in steps of 250 Hz |
| **Transmit Section** | | | | | |
| Transmit data rate | 0.6 | | 76.8 | kBaud | NRZ or Manchester encoding. 76.8 kBaud equals 76.8 kbit/s using NRZ coding. See page 14. |
| Binary FSK frequency separation | 0 | | 65 | kHz | The frequency corresponding to the digital "0" is denoted $f_0$, while $f_1$ corresponds to a digital "1". The frequency separation is $f_1$-$f_0$. The RF carrier frequency, $f_c$, is then given by $f_c=(f_0+f_1)/2$. (The frequency deviation is given by $f_d$=+/-($f_1$-$f_0$)/2 ) The frequency separation is programmable in 250 Hz steps. 65 kHz is the minimum guaranteed separation at 1 MHz reference frequency. Larger separations can be achieved at higher reference frequencies. |
| Output power<br>433 MHz<br>868 MHz | <br>-20<br>-20 | | <br>10<br>5 | <br>dBm | Delivered to 50 Ω load.<br>The output power is programmable. |
| RF output impedance<br>433/868 MHz | | 140 / 80 | | Ω | Transmit mode. For matching details see “Input/ output matching” p.28. |
| Harmonics | | -20 | | dBc | An external LC or SAW filter should be used to reduce harmonics emission to comply with SRD requirements. See p.34. |

| Parameter | Min. | Typ. | Max. | Unit | Condition / Note |
|---|---|---|---|---|---|
| **Receive Section** | | | | | |
| Receiver Sensitivity, 433 MHz<br>Optimum sensitivity (9.3 mA)<br>Low current consumption (7.4 mA) | | <br>-110<br>-109 | | <br>dBm | 2.4 kBaud, Manchester coded data, 64 kHz frequency separation, BER = $10^{-3}$ |
| Receiver Sensitivity, 868 MHz<br>Optimum sensitivity (11.8 mA)<br>Low current consumption (9.6 mA) | | <br>-107<br>-105 | | <br>dBm | See Table 5 and Table 6 page 19 for typical sensitivity figures at other data rates. |
| System noise bandwidth | | 30 | | kHz | 2.4 kBaud, Manchester coded data |
| Cascaded noise figure 433/868 MHz | | 12/13 | | dB | |
| Saturation | 10 | | | dBm | 2.4 kBaud, Manchester coded data, BER = $10^{-3}$ |
| Input IP3 | | -18 | | dBm | From LNA to IF output |
| Blocking | | 40 | | dBc | At +/- 1 MHz |
| LO leakage | | | -57 | dBm | |
| Input impedance | | <br>88-j26<br>70-j26<br>52-j7<br>52-j4 | | <br>Ω<br>Ω<br>Ω<br>Ω | Receive mode, series equivalent<br>at 315 MHz<br>at 433 MHz<br>at 868 MHz.<br>at 915 MHz<br>For matching details see “Input/ output matching” p. 28. |
| Turn on time | 11 | | 128 | Baud | The turn-on time is determined by the demodulator settling time, which is programmable. See p. 17 |
| **IF Section** | | | | | |
| Intermediate frequency (IF) | | 150 | <br>10.7 | kHz<br>MHz | Internal IF filter<br>External IF filter |
| IF bandwidth | | 175 | | kHz | |
| RSSI dynamic range | -105 | | -50 | dBm | |
| RSSI accuracy | | ± 6 | | dB | See p.30 for details |
| RSSI linearity | | ± 2 | | dB | |
| **Frequency Synthesiser Section** | | | | | |
| Crystal Oscillator Frequency | 3 | | 16 | MHz | Crystal frequency can be 3-4, 6-8 or 9-16 MHz. Recommended frequencies are 3.6864, 7.3728, 11.0592 and 14.7456. See page 32 for details. |

| Parameter | Min. | Typ. | Max. | Unit | Condition / Note |
|---|---|---|---|---|---|
| Crystal frequency accuracy requirement | | ± 50<br>± 25 | | ppm | 433 MHz<br>868 MHz<br>The crystal frequency accuracy and drift (ageing and temperature dependency) will determine the frequency accuracy of the transmitted signal. |
| Crystal operation | | Parallel | | | C171 and C181 are loading capacitors, see page 32 |
| Crystal load capacitance | 12<br>12<br>12 | 22<br>16<br>16 | 30<br>30<br>16 | pF<br>pF<br>pF | 3-8 MHz, 22 pF recommended<br>6-8 MHz, 16 pF recommended<br>9-16 MHz, 16 pF recommended |
| Crystal oscillator start-up time | | 5<br>1.5<br>2 | | ms<br>ms<br>ms | 3.6864 MHz, 16 pF load<br>7.3728 MHz, 16 pF load<br>16 MHz, 16 pF load |
| Output signal phase noise | | -85 | | dBc/Hz | At 100 kHz offset from carrier |
| PLL lock time (RX / TX turn time) | | 200 | | µs | Up to 1 MHz frequency step |
| PLL turn-on time, crystal oscillator on in power down mode | | 250 | | µs | Crystal oscillator running |
| **Digital Inputs/Outputs** | | | | | |
| Logic "0" input voltage | 0 | | 0.3*VDD | V | |
| Logic "1" input voltage | 0.7*VDD | | VDD | V | |
| Logic "0" output voltage | 0 | | 0.4 | V | Output current -2.5 mA, 3.0 V supply voltage |
| Logic "1" output voltage | 2.5 | | VDD | V | Output current 2.5 mA, 3.0 V supply voltage |
| Logic "0" input current | NA | | -1 | µA | Input signal equals GND |
| Logic "1" input current | NA | | 1 | µA | Input signal equals VDD |
| DIO setup time | 20 | | | ns | TX mode, minimum time DIO must be ready before the positive edge of DCLK |
| DIO hold time | 10 | | | ns | TX mode, minimum time DIO must be held after the positive edge of DCLK |
| Serial interface (PCLK, PDATA and PALE) timing specification | | | | | See Table 2 page 12 |
| **Power Supply** | | | | | |
| Supply voltage | | 3.0 | | V | Recommended operation voltage |
| | 2.1 | | 3.6 | V | Operating limits |
| Power Down mode | | 0.2 | 1 | µA | Oscillator core off |
| Current Consumption, receive mode 433/868 MHz | | 7.4/9.6 | | mA | Current is programmable and can be increased for improved sensitivity |
| Current Consumption, average in receive mode using polling 433/868 MHz | | 74/96 | | µA | Polling controlled by micro-controller using 1:100 receive to power down ratio |

| Parameter | Min. | Typ. | Max. | Unit | Condition / Note |
|---|---|---|---|---|---|
| Current Consumption, transmit mode 433/868 MHz: | | | | | |
| P=0.01mW (-20dBm) | | 5.3/8.6 | | mA | The ouput power is delivered to a 50Ω load, see also p. 29 |
| P=0.3mW (-5dBm) | | 8.9/13.8 | | mA | |
| P=1mW (0dBm) | | 10.4/16.5 | | mA | |
| P=3mW (5dBm) | | 14.8/25.4 | | mA | |
| P=10mW (10dBm) | | 26.7/NA | | mA | |
| Current Consumption, crystal osc. | | 30<br>80<br>105 | | µA | 3-8 MHz, 16 pF load<br>9-14 MHz, 12 pF load<br>14-16 MHz, 16 pF load |
| Current Consumption, crystal osc. and bias | | 860 | | µA | |
| Current Consumption, crystal osc., bias and synthesiser, RX/TX | | 4/5<br>5/6 | | mA<br>mA | < 500 MHz<br>> 500 MHz |

## Circuit Description

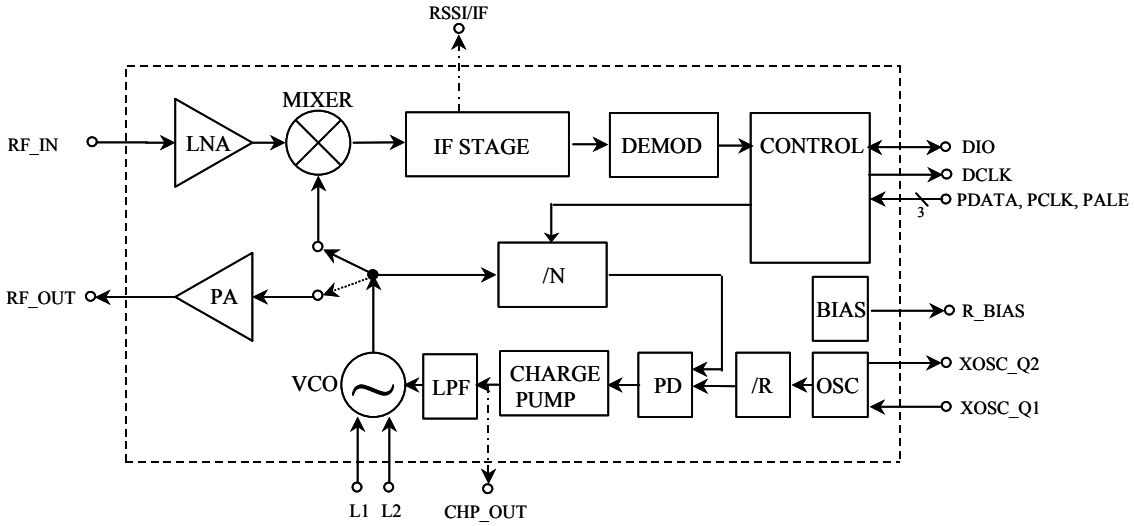



**Figure 1. Simplified block diagram of the *CC1000***

A simplified block diagram of ***CC1000*** is shown in Figure 1. Only signal pins are shown.

In receive mode ***CC1000*** is configured as a traditional superheterodyne receiver. The RF input signal is amplified by the low-noise amplifier (LNA) and converted down to the intermediate frequency (IF) by the mixer (MIXER). In the intermediate frequency stage (IF STAGE) this downconverted signal is amplified and filtered before being fed to the demodulator (DEMOD). As an option a RSSI signal, or the IF signal after the mixer is available at the RSSI/IF pin. After demodulation ***CC1000*** outputs the digital demodulated data on the pin DIO. Synchronisation is done on-chip providing data clock at DCLK.

In transmit mode the voltage controlled oscillator (VCO) output signal is fed directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream fed to the pin DIO. The internal T/R switch circuitry makes the antenna interface and matching very easy.

The frequency synthesiser generates the local oscillator signal which is fed to the MIXER in receive mode and to the PA in transmit mode. The frequency synthesiser consists of a crystal oscillator (XOSC), phase detector (PD), charge pump (CHARGE PUMP), VCO, and frequency dividers (/R and /N). An external crystal must be connected to XOSC, and only an external inductor is required for the VCO.

The 3-wire digital serial interface (CONTROL) is used for configuration.

## Application Circuit

Very few external components are required for the operation of ***CC1000***. A typical application circuit is shown in Figure 2. Component values are shown in Table 1.

**Input / output matching**
C31/L32 is the input match for the receiver, and L32 is also a DC choke for biasing. C41, L41 and C42 are used to match the transmitter to 50 Ohm. An internal T/R switch circuit makes it possible to connect the input and output together and match the ***CC1000*** to 50 Ω in both RX and TX mode. See "Input/output matching" p.28 for details.

**VCO inductor**
The VCO is completely integrated except for the inductor L101.

Component values for the matching network and VCO inductor are easily calculated using the SmartRF Studio software.

**Additional filtering**
Additional external components (e.g. RF LC or SAW-filter) may be used in order to improve the performance in specific applications. See also "Optional LC filter" p.34 for further information.

**Voltage supply decoupling**
C10-C16 are voltage supply de-coupling capacitors. These capacitors should be placed as close as possible to the voltage supply pins of ***CC1000***.

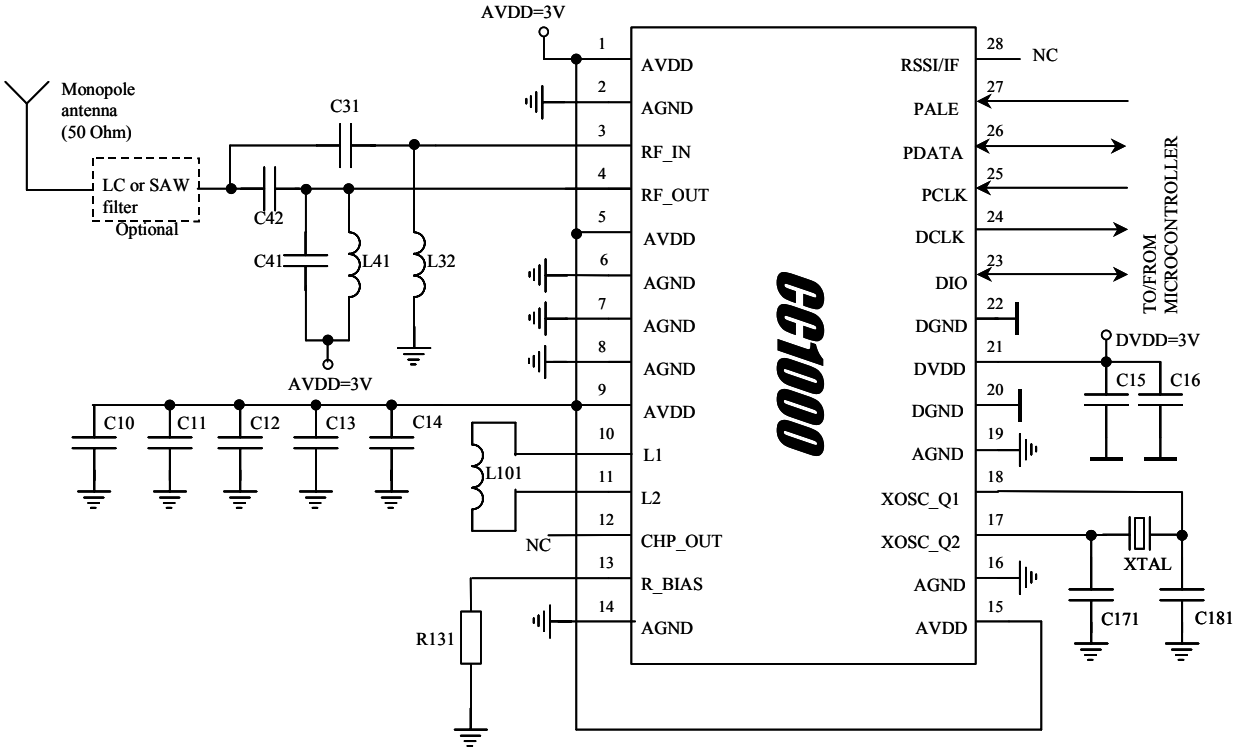



**Figure 2. Typical *CC1000* application circuit**

## IF output

***CC1000*** has a built-in 10.7 MHz IF output buffer. This buffer could be applied in narrow-band applications with requirements on mirror image filtering. The system is then built with ***CC1000***, a 10.7 MHz ceramic filter and an external 10.7 MHz demodulator. The external network for IF output operation is shown in Figure 21. R281 = 470 Ω, C281 = 3.3nF.

The external network provides 330 Ω source impedance for the 10.7 MHz ceramic filter.

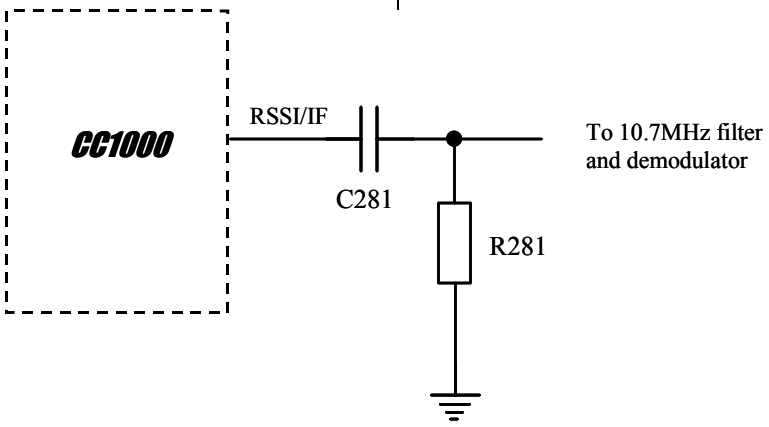



**Figure 21. IF output circuit**