GOC-MD-630

USER MANUAL

(This module is limited to OEM Installation only)

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1. Introduction

GOC-MD-630 , be of Bluetooth v2.1 system , combines radio frequency, Bluetooth Baseband controller and Bluetooth antenna together into a small close box to make cost down and worryless, and save space as well .

GOC-MD-630 is intended for Bluetooth applications where a host processor is capable of running the Bluetooth sortware stack . With the on-chip CSR Bluetooth software stack , it provides a fully comliant Bluetooth v2.1 specification system for data and voice communications .

In addition , GOC-MD-630 can help users customize soft well based on abundance in extra soft well design .

2. Fields for application

A、 Cellular handsets

B、 PDAs and PNDs

C、 Automotive

D、 Embedded systems

3. Main Specification instruction

Table 1: main Specifications

Production	Bluetooth Heart Module
type	GOC-MD-630
Standard	Bluetooth v2.1
Frequency Range	2.4~2.48GHz
Modulation Method	GFSK, 1Mbps, 0.5BT Gaussian
Max speed for transfer	Asynchronous: 723.2kbps/57.6kbps Synchronous: 433.9kbps/433.9kbps
Hop	1600hops/sec, 1MHz channel space
Output impedance	50 ohms
Crystal Frequency	26MHz
Outer interface	UART，PCM，PIO, SPI CSPI，SDIO
Apply to Bluetooth instructions	OPP,OBEX,SPP, A2DP, AVRCP, FTP ,HS/HF,PBAB ， DUN Profiles
Range for working distance	10 meters (33 feet)
Receiving Sensitivity	-90dBm@0.1%BER
Emissive power	<4dBm
Connect Method	Point to Multi-Point
Audio Function	
Audio Coding	
SNC	
Accounting Audio coding	
Size	11.60mm X 17.09mm X 0.8mm
POWER	
POWER Voltage	2.7V~4.9V
working Current	≤70mA Typical
Standby Current	<0.1mA
Working condition	
Storage Temperature Range	-40° C to +85° C
Operating Temperature Range	-30° C to +85° C
Humidity Range	10%~90% Non-Condensing
Certificates	BQB,CE,FCC

4. Microcontroller, Memory and Baseband Logic

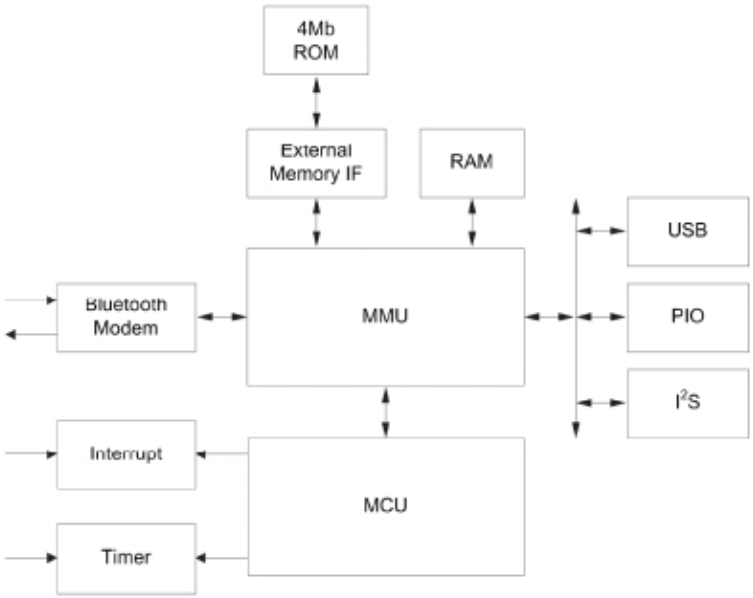


Figure 1 : Baseband Digits Block Diagram

4.1 AuriStream CODEC

The AuriStream CODEC works on the principle of transmitting the delta between the actual value of the signal and a prediction rather than the signal itself. Hence, the information transmitted is reduced along with the power requirement. The quality of the output depends on the number of bits used to represent the sample.

The inclusion of AuriStream results in reduced power consumption compared to a CVSD implementation when used at both ends of the system.

4.1.1 AuriStream CODEC Requirements

AuriStream supports the following modes of operation :

	fs	Bit Rate (kbps)							
		16	20	24	32	40	48	64	80
G726	8 kHz	(✓)		✓	✓	✓			
	10 kHz				(✓)		(✓)	(✓)	(✓)
G722	8 kHz		(✓)	(✓)	(✓)				
	16 kHz					(✓)	✓	✓	

Table 2 : AuriStream Supported Bitrates

4.2 Memory Managements Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory(RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

4.3 Burst Mode Controller

During transmission the Burst Mode Controller(BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.4 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error correction
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/ -law/linear voice data (from host)
- A-law/ -law/Continuously variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.1 including AFH and eSCO.

4.5 WLAN Coexistence

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. For more information contact Buegiga technical support.

4.6 Configurable I/O Parallel Ports

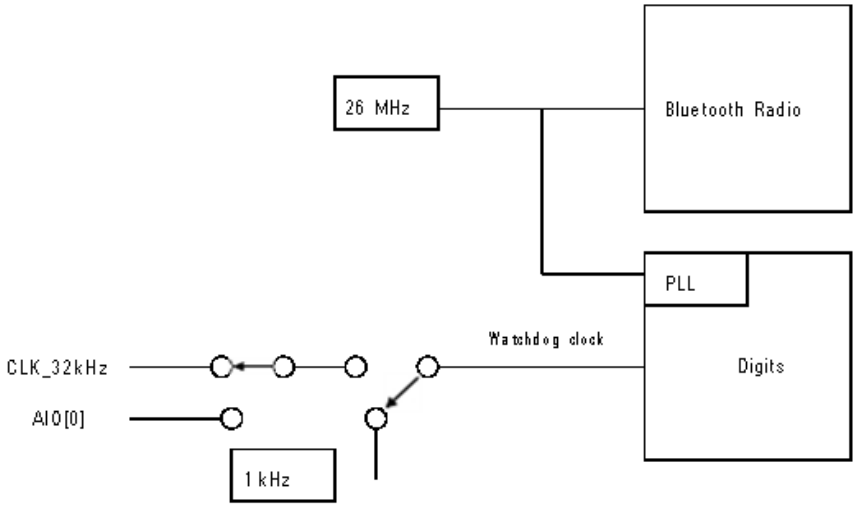
7 lines of programmable bi-directional input/outputs (I/O) are provided. PIO[1: 5, 7, 9] are powered from VDD_PADS .

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset .

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.PIO[2] can be configured as a request line for an external clock source .

4 . 7 Clock Generation

GOC-MD-630 uses an internal 26 MHz crystal as a Bluetooth reference clock. All GOC-MD-630 internal digital clocks are generated using a phase locked loop, which is locked to the 26 MHz reference clock.
Also supplied to the digits is a watchdog clock, for use in low power modes. This uses a frequency of 32.768kHz from CLK_32K, or an internally generated reference clock frequency of 1kHz, determined by PSKEY_DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE.
The use of the watchdog clock is determined with respect to Bluetooth operation in low power modes.



4.7.1 32kHz External Reference Clock

A 32kHz clock can be applied to CLK_32K, using PSKEY_DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE. The CLK_32K pad is in the VDD_PADS domain with all the other digital I/O pads and is driven between levels specified in Section 7.3.4.

5. Host Interfaces

5.1 Host Information

This module was defined to be used for specific host only. The designated host for this module was:

Company: Mobile Devices Ingénierie
Address: 100 avenue de Stalingrad 94800 VILLEJUIF – France
Host Model Name: C4MAX/C4MAX+
Host brand name: Mobile Devices

The MCU selects the UART/SDIO interfaces by reading PIO[4] at boot-time. When PIO[4] is high, the SDIO interface is enabled; when PIO[4] is low, the UART is enabled.

If in UART mode, the MCU selects the UART transfer protocol automatically using the unused SDIO pins shown in Table 2 .

SDIO_CLK	SDIO_CMD	Protocol
0	0	bcsp
0	1	h4
1	0	h4ds
1	1	h5

Table 3 : SDIO_CLK and SDIO_CMD transfer Protocols

5.2 UART Interface

This is a standard UART interface for communicating with other serial devices .

GOC-MD-630 UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

Note:

WT21 uses RS232 protocol, but voltage levels are 0V to VDD_PADS (requires external RS232 transceiver chip.

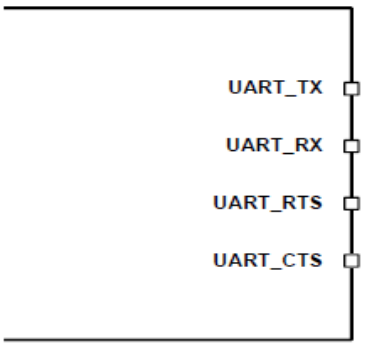


Figure 2 : Universal Asynchronous Receiver

Four signals implement the UART function, as shown in Figure 2 . When GOC-MD-630 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.
UART configuration parameters, such as baud rate and packet format, are set using GOC-MD-630 firmware.

Note:

An accelerated serial port adapter is required to communicate with the UART at maximum baud rate using a standard PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Figure 3 : Possible UART Settings

Note:

Baud rate is the measure of symbol rate i.e. , the number of distinct symbol changes (signaling events) made to transmission medium per second in a digitally modulated Signal.

The UART interface is capable of resetting GOC-MD-630 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 4. If tBRKis longer than the value, defined by the PSKEY_HOSTIO_UART_RESET_TIMEOUT, (0x1a4), a reset occurs. This feature allows a host to initialise the system to a known state. Also, WT21 can emit a break character that may be used to wake the host. By default this feature is disabled and it is recommended to enable it by setting PSKEY_HOSTIO_UART_RESET_TIMEOUT.

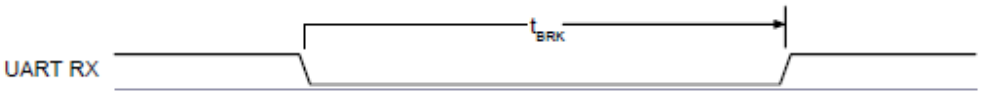


Figure 4 : Break Signal

Table 3 shows a list of commonly used baud rates and their associated values for the PSKEY_UART_BAUDRATE (0x1be). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula .

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 4 : Baud rate

5.2.1 UART Configuration While Reset is Active

The UART interface for WT21 is tri-state while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when WT21 reset is de-asserted and the firmware begins to run .

5.3 SDIO Interface

This is a host interface which allows a Secure Digital Input Output(SDIO) host to gain access to the internals of the chip. It provides all defined slave modes (SPI, SD 1bit, SD 4bit), but not SD host function.

The function provided includes generating responses to each command in hardware and implementing the state machines defined in the SDIO specification. Within the various modes of operation, it provides initialisation functions (cmds 0, 3, 5, 7, 15, 59) and two other functions:

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

- Function 1 provides Bluetooth type A support, and follows that specification

- Function 2 provides generic register access(cmd52 (byte read/write))

For more information, see the following specifications:

- SD Specifications Part 1 Physical Layer Specification v.1.10
- SD Specification Part E1 SDIO Specification v.1.10
- SDIO Card Part E2 Type-A Specification for Bluetooth v.1.00

5.3.1 SDIO/CSPI Deep-Sleep Control Schemes

This is the lowest power mode, where the processor, the internal reference (fast) clock, and much of the digital and analogue hardware are shut down. To support this power consumption reduction solution and to prevent any errors arising on the SDIO host interface there are two Deep-Sleep control schemes.

- Scheme 1: The host retransmits any packets that Bluecore was unable to receive as a result of being in Deep-Sleep
- Scheme 2: Introduces additional signaling to prevent the need for retransmissions

During Deep-Sleep the internal reference clock is turned off. However, the host transport protocols (SD/UART/CSPI) are driven from the SDIO clock and so continue to function during Deep-Sleep, enabling access to the function 0 interface, but not the function 1 interface.

5.3.2 Retransmission

Bluecore enters Deep-Sleep whenever it becomes idle after which time, when the host transmits a message on function 1 an illegal command error will be signaled. The activity that this initiates on the SDIO Interface provokes Bluecore into wakeup after which the host re-transmits the original message.

Bluecore will wait for a configurable period of time before re-entering Deep-Sleep, thus ensuring that the original packet is sent/received on retransmission. This control scheme is the default mode of operation.

5.3.3 Signaling

Signalling between the host and Bluecore enables host control over Bluecore Deep-Sleep mode. Consequently the host is aware of when it is appropriate to send Bluecore HCI traffic over function 1.

The signals used by this scheme are Host wakeup and Ready status interrupt select, implemented as register bit in the vendor unique area of function 0.

5.4 Serial Peripheral Interface (SPI)

5.4.1 GOC-MD-630 Serial Peripheral Interface (SPI)

SPI is used for debuging primarily. This section details the considerations required when interfacing to GOC-MD-630 via the SPI.
Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

5.4.2 Instruction Cycle

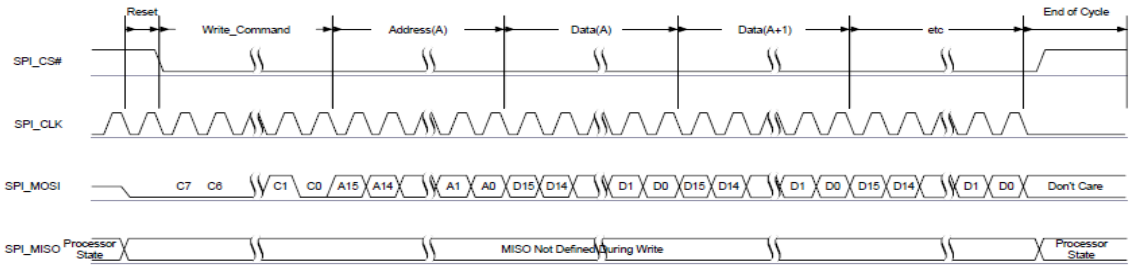
GOC-MD-630 is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8 shows the instruction cycle for an SPI transaction.

Table 5 : Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the WT21 on the rising edge of the clock line SPI_CLK. When reading, WT21 replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this WT21 offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

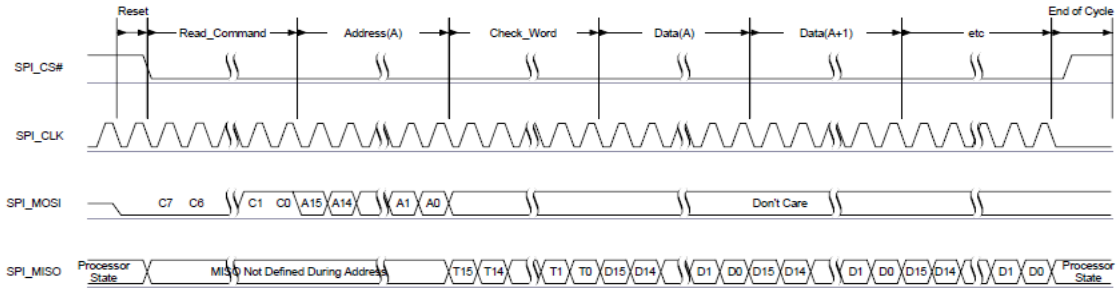
5.4.3 Writing to the Device



To write to GOC-MD-630, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

Figure 5 : SPI Write Operation

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high



5.4.4 Reading from the Device

Reading from GOC-MD-630 is similar to writing to it. An 8-bit read command (00000011) is sent first (C [7:0]), followed by the address of the location to be read (A[15:0]). WT21 then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

Figure 6 : SPI Read Operation

5.4.5 Multi-Slave Operation

GOC-MD-630 should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When WT21 is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, WT21 outputs 0 if

the processor is running or 1 if it is stopped .

6. Size and Pin definition

6.1 SIZE

THE SIZE OF GOC-MD-630 IS : 11.60mm X 17.09mm X 1.2mm .

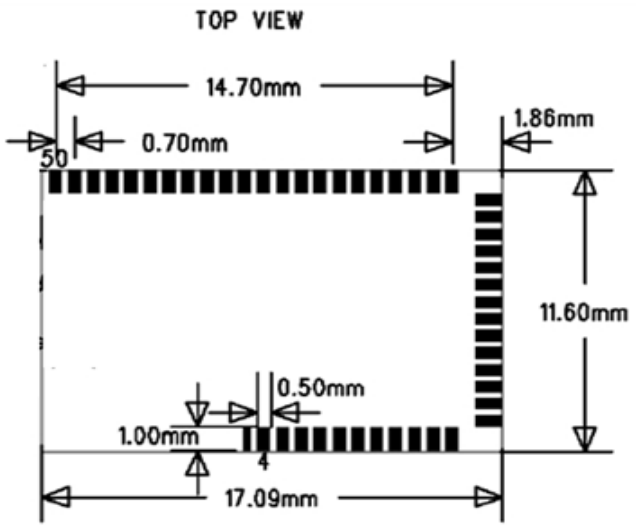


Figure 7 : GOC-MD-630 size and pin

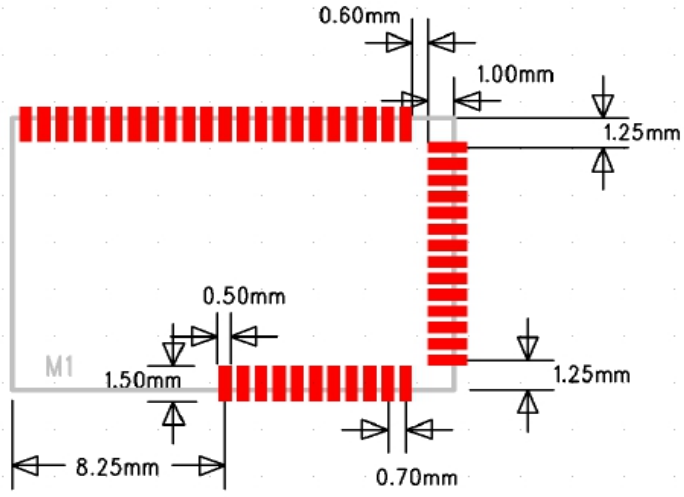


Figure 8 : GOC-MD-630 recommended land pattern

6.2 PIN definition and Terminal Description

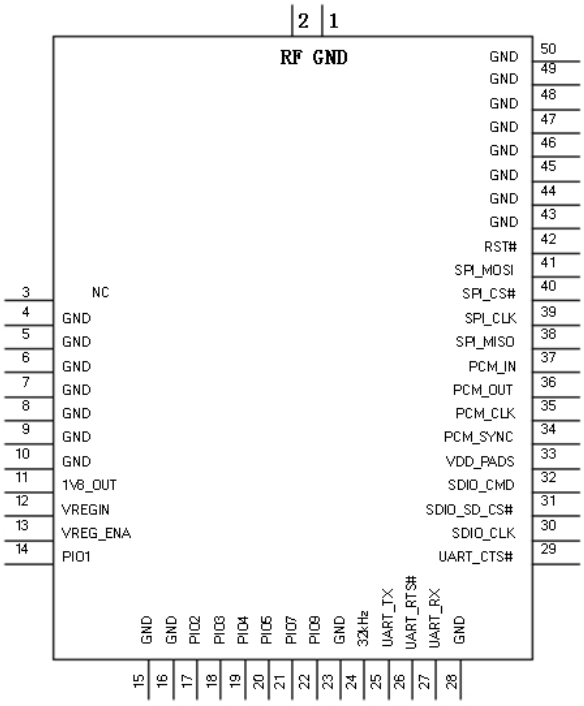


Figure 9 : GOC-MD-630 pin out

Table 6 : Pin out Definition

Pin	Symbol	I/O	Description
1	GND	GND	Ground
2	RF	ANT	RF Interface
3	NC	Not in use	Leave floating or connect to GND
4	GND	GND	Ground
5	GND	GND	Ground
6	GND	GND	Ground
7	GND	GND	Ground
8	GND	GND	Ground
9	GND	GND	Ground
10	GND	GND	Ground

11	1V8_OUT	Power output	1.8V regulator output
12	VREGIN	Power input	Input for the internal 1,8V regulator
13	VREG_ENA	input	Take high to enable internal voltage regulators
14	PIO1	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
15	GND	GND	Ground
16	GND	GND	Ground
17	PIO2	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
18	PIO3	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
19	PIO4	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
20	PIO5	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
21	PIO7	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
22	PIO9	Bi-directional, programmamble strength internal pull-down/pull-up	Programmamble input/output line
23	GND	GND	Ground
24	32KHz	Clock input	32KHz clk input
25	SDIO_DATA[0] CSPI_MISO	Bi-directional, tri-	Synchronous data input/output CSPI data output

	UART_TX	state, weak internal pull-down	UART data output, active high
26	SDIO_DATA[1] CSPI_INT UART_RTS	Bi-directional,weak internal pull-down	Synchronous data input/output CSPI data input UART request to send, active low
27	SDIO_DATA[2] UART_RX	Bi-directional, weak internal pull-down	Synchronous data input/output UART data input, active high
28	GND	GND	Ground
29	SDIO_DATA[3] CSPI_CS# UART_CTS#	Bi-directional, weak internal pull-down	Synchronous data input/output Chip select for CSR Serial Peripheral Interface, active low UART clear to send, active low
30	SDIO_CLK CSPI_CLK	Bi-directional, weak internal pull-	SDIO clock CSPI clock
31	SDIO_SD_CS#	Bi-directional, weak internal pull-down	SDIO chip select to allow SDIO accessess
32	SDIO_CMD SDIO_CMD	Bi-directional, weak internal pull-down	SDIO data input SDIO data input
33	VDD_PADS	Power input	Positive supply for the digital interfaces
34	PCM_SYNC	Bi-directional, weak internal pull-down	Synchronous data sync
35	PCM_CLK	Bi-directional, weak internal pull-down	Synchronous data clock
36	PCM_OUT	Output, tri-state, weak internal pull-down	Synchronous data output
37	PCM_IN	Input, weak internal pull- down	Synchronous data input
38	SPI_MISO	Output, tri-state, weak internal pull-down	SPI data output
39	SPI_CLK	Bi-directional, weak internal pull-down	SPI clock
40	SPI_CS#	Bi-directional, weak internal pull-down	Chip select for Serial Peripheral Interface, active low
41	SPI_MOSI	Weak internal pull-down	SPI data input
42	RST#	Input, weak internal pull- up	Active low reset. Keep low for >5 ms to cause a reset

43	GND	GND	Ground
44	GND	GND	Ground
45	GND	GND	Ground
46	GND	GND	Ground
47	GND	GND	Ground
48	GND	GND	Ground
49	GND	GND	Ground
50	GND	GND	Ground

7. Electric Feature

7.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	85	°C
IO Voltage	VDD_PADS	-0.4	3.7	V
Supply Voltage	VREG_IN, VREG_ENA	-0.4	4.9	V
Other Terminal Voltages		VSS-0.4	VDD+0.4	V

Table 7 : Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Rating		Min	Max	Unit
Operating Temperature Range		-30	85	°C
IO Voltage	VDD_PADS	1.7	3.7	V

Table 8 : Recommended Operating Conditions

7.3 Input/Output Terminal Characteristics

7.3.1 Linear Voltage Regulator

Normal Operation	**Min**	**Typ**	**Max**	**Unit**
Input voltage	2.7	-	4.9	V
Output voltage (I_{load} = 70 mA / VREG_IN = 3.0 V)	1.7	1.8	1.9	V
Temperature coefficient	-250	0	250	ppm/°C
Output noise	-	-	1	mV rms
Load regulation (I_{load} < 70 mA)	-	-	50	mV/A
Settling time	-	-	50	µs
Maximum output current	70	-	-	mA
Minimum load current	5	-	-	µA
Drop-out voltage (I_{load} = 70 mA)	-	-	600	mV
Quiescent current (excluding load, I_{load} < 100µA)	30	40	60	µA
Low Power Mode				
Quiescent current (excluding load, I_{load} < 100µA)	10	13	21	µA
Standby Mode				
Quiescent current (excluding load, I_{load} < 100µA)	1.5	2.5	3.3	µA

Table 9 : Recommended Voltage Operating Conditions

7.3.2 Digital

Digital Terminals	**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels				
V_{IL} input logic level low 1.7V ≤ VDD ≤ 3.6V	-0.4	-	0.25xVDD	V
V_{IH} input logic level high 1.7V ≤ VDD ≤ 3.6V	0.7VDD	-	VDD+0.3	V
Output voltage levels				
V_{OL} output logic level low 1.7V ≤ VDD ≤ 3.6V, (I_o = 4.0 mA)	-	-	0.125	V
V_{OH} output logic level high 1.7V ≤ VDD ≤ 3.6V, (I_o = -4.0 mA)	VDD-0.4	-	VDD	V
Input Tri-state Current with:				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	10	40	100	µA
Weak pull-up	-5	-1	-0.2	µA
Weak pull-down	0.2	1	5	µA
I/O pad leakage curren	-1	0	1	µA
CI input capacitance	1	-	5	pF

Table 10 : Digital terminal electrical characteristics

7.3.3 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE ([a] falling threshold)	1.13	1.24	1.3	V
VDD_CORE ([a] rising threshold)	1.2	1.31	1.35	V
Hysteresis	0.05	0.07	0.15	V

(VDD_CORE is a core voltage supplied by the internal 1.5 V voltage regulator.)

Table 11 : Power on reset characteristics

7.3.4 32 kHz External Reference Clock

Parameter	Conditions/Not	Specifications			Units
Parameter	**Conditions/Not**	**Min**	**Nom**	**Max**	**Units**
Frequency		32748	32768	32788	Hz
Frequency deviation	@25°C	-	-	20	+/- ppm
Frequency deviation	-25°C to 85°C	-	-	150	+/- ppm
Input high level	Square wave	0.625xVDD_PADS	-	-	V
Input low level	Square wave	-	-	0.425xVDD_PADS	V
Duty cycle	Square wave	30	-	70	%
Rise and fall time		-	-	50	ns
Integrated frequency jitter	Integrated over the band 200 Hz to 15 kHz	-	-	-	Hz (rms)

Table 12 : External Reference Clock

7.4 Power Consumption

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.4	mA
Inquiry and page scan, time interval1,28s	-	0.8	mA
ACL no trafic	Master	4	mA
ACL with file transfer	Master	9	mA
ACL 40ms sniff	Master	2	mA
ACL 1,28s sniff	Master	0.2	mA
eSCO EV5	Master	12	mA
eSCO EV3	Master	18	mA
eSCO EV3 - hands-free - setting S1	Master	18.5	mA
SCO HV1	Master	37	mA
SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	17	mA
ACL no traffic	Slave	14	mA
ACL with file transfer	Slave	17	mA
ACL 40ms sniff	Slave	1.6	mA
ACL 1.28s sniff	Slave	0.2	mA
eSCO EV5	Slave	19	mA
eSCO EV3	Slave	23	mA
eSCO EV3 - hands-free - setting S1	Slave	23	mA
SCO HV1	Slave	37	mA
SCO HV3	Slave	23	mA
SCO HV3 30ms sniff	Slave	16	mA
Standby host connection (Deep-Sleep)	-	40	µA
Reset (active low)	-	39	µA

Note:
Conditions 20°C
VREG_IN 3.15V
VDD_PADS 3.15V
UART BAUD rate 115.2 kbps

Table 13 : Power Consumption

7.5 FCC RF Exposure Requirement

1. At least 20cm separation distance between the antenna and the user's body must be maintained at all times. And must not transmit simultaneously with any other antenna or transmitter, except in accordance with FCC multi transmitter product procedures.

2. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile-only exposure condition must not exceed 0dBi in the 2.4G band.

3. A user manual with the end product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

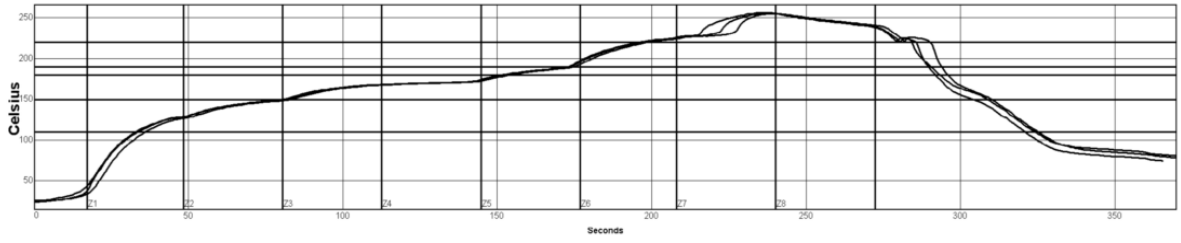
SUGGESTED REFLOW PROFILE

Oven Name: WQ **Process Window Name: 无铅**

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8
Top	140	155	170	170	190	230	265	240
Bottom	140	155	170	170	190	230	265	240

Conveyor Speed (cm/min): 75.0



PWI= 313%	Max Rising Slope		Preheat 110-190C		Soak Time 150-180C		Reflow Time /220C		Peak Temp	
2	3.9	189%	139.2	146%	69.9	301%	88.4	284%	256.2	125%
3	4.1	205%	138.2	141%	69.7	303%	87.9	279%	256.7	133%
4	3.9	194%	137.4	137%	70.2	298%	91.3	313%	255.4	108%

Process Window:

Solder Paste: SYSTEM DEFAULT

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.0)	0.0	3.0	Degrees/Second
Preheat Time 110-190C	90	130	Seconds
Soak Time 150-180C	90	110	Seconds
Time Above Reflow - 220C	50	70	Seconds
Peak Temperature	245	255	Degrees Celsius

Please be noticed following information and instructions should be placed in the end-user's operating manual

The GOC-MD-630_SPECv3.0_EN Module has been granted as limited modular approval for mobile applications. GOC-MD-630_SPECv3.0_EN Module must be installed in the designated host as specified in this manual.

1. Separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

2. The GOC-MD-630_SPECv3.0_EN Module and its antenna must not be co-located or operating in conjunction with any other transmitter or antenna within a host device. This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment.

3. A label must be affixed to the outside of the end product into which the GOC-MD-630_SPECv3.0_EN module is incorporated, with a statement similar to the following: For GOC-MD-630_SPECv3.0_EN: This device contains FCC ID: PCC-GOC20121009.

4. The module shall be in non-detachable construction protection into the finished products, so that the end-user has to destroy the module while remove or install it.

5. This module is to be installed only in mobile or fixed applications. According to FCC part 2.1091(b) definition of mobile and fixed devices is:.

Mobile device:
A mobile device is defined as a transmitting device designed to be used in other than fixed locations and to generally be used in such a way that a separation distance of at least 20 centimeters is normally maintained between the transmitter's radiating structure(s) and the body of the user or nearby persons. In this context, the term ''fixed location'' means that the device is physically secured at one location and is not able to be easily moved to another location.

Portable device:
For purposes of this section, a portable device is defined as a transmitting device designed to be used so that the radiating structure(s) of the device is/are within 20 centimeters of the body of the user.

6. Separate approval is required for all other operating configurations, including portable configurations with respect to FCC Part 2.1093 and different antenna configurations.

7. A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labelled with an FCC ID: PCC-GOC20121009. The OEM manual must provide clear instructions explaining to the OEM the labelling requirements, options and OEM user manual instructions that are required

For a host using a this FCC certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: PCC-GOC20121009" or "Contains FCC ID: PCC-GOC20121009" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

8. Host product is required to comply with all applicable FCC equipment authorizations regulations, requirements and equipment functions not associated with the transmitter module portion. compliance must be

demonstrated to regulations for other transmitter components within the host product; to requirements for unintentional radiators (Part 15B). To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. If a host was previously authorized as an unintentional radiator under the Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements. Since this may depend on the details of how the module is integrated with the host, we suggest the host device to recertify part 15B to ensure complete compliance with FCC requirement: Part 2 Subpart J Equipment Authorization Procedures , KDB784748 D01 v07, and KDB 997198 about importation of radio frequency devices into the United States.

FCC Certification Requirement:

The end product with an embedded - GOC-MD-630_SPECv3.0_EN Module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

Note: If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093.

This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications made to this equipment not expressly approved by Shenzhen Goodocomm Information Technology Co., Ltd may void the FCC authorization to operate this equipment.