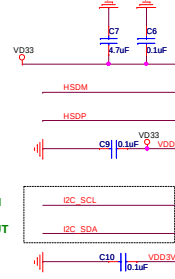


Note:
If SPS mode, then R11 10k ohm pull-low, R21 NC and L2 2.2 uH.
If LDO mode, then R11 NC, R21 10k ohm pull-high and L2 0 ohm.

C7(4.7 uF) -> C6(0.1 uF) -> Pin1
placing order in PCB layout



Note:
Must be placed
the reserved 0 ohm
resistor for BQB Uart test.



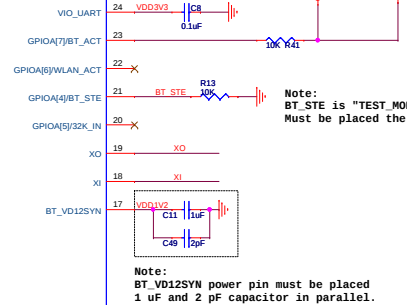
RTL8761BUV QFN32



Note:
3.3 V power pin recommended cap type is X5R/10V or above.
1.2 V power pin recommended cap type is X5R/5.3V or above.
RF power pin (Pin 13, 14, 16 & 17) cap value can not
be less than 1 uF.

Note:
BT_WAKE_HOST is "EEPROM_SEL"
power on latch pin.
Must be placed the pull-low 10 kohm
resistor to GND.

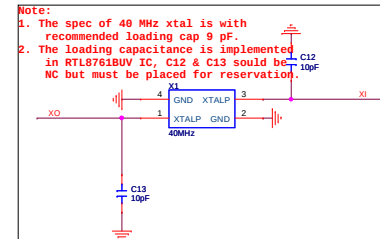
Note:
"DIS_BT_N" pin could be
connected to the host to
implement reset function.



Note:
BT_STE is "TEST_MODE_SEL" power on latch pin.
Must be placed the pull-low 10 kohm resistor to GND.

40MHz xtal clock

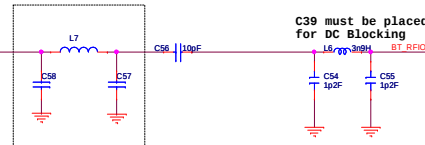
USB plug-in connection



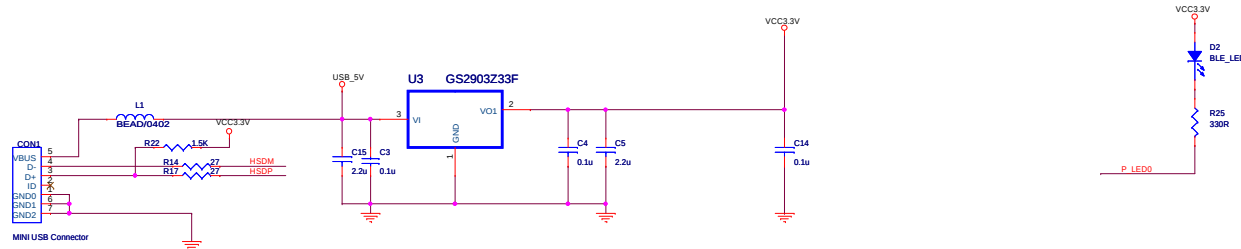
Note:
1. The spec of 40 Mhz xtal is with
recommended loading cap 9 pF.
2. The loading capacitance is implemented
in RTL8761BUV IC, C12 & C13 should be
NC but must be placed for reservation.

RFIO & pi-matching circuit

Depending on antenna design,
this pi-matching is decided by customer



RFIO



RTL8761BUV_QFN32			
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A2	<Doc>		
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