Aditus System
16-Line RAU RF Module
(RRFM)

Design Description

11/2/99

Approved by: JP Cole
Author: Bill Fujimoto
Document Number: 95-000114-00
Revision Number: 1

Revision History:

Revision 1: November 2,1999 Original

Table of Contents

TABLE OF CONTENTS 3

1. REFERENCE DOCUMENTS 4

2. OVERVIEW AND SCOPE 4

3. BLOCK DIAGRAM 4

4. RADIO SPECIFICATIONS 5

4.1 RECEIVE PATH SPECIFICATIONS 5
4.2 TRANSMIT PATH SPECIFICATIONS 5
4.3 LO SYNTHESIZER SPECIFICATIONS 6

5. DATALINK AND INTERFACE SPECIFICATIONS 6

5.1 DATALINK SPECIFICATIONS 6
5.2 INTERFACE SPECIFICATIONS 6

6. DESCRIPTION OF OPERATION 7

1. Reference Documents

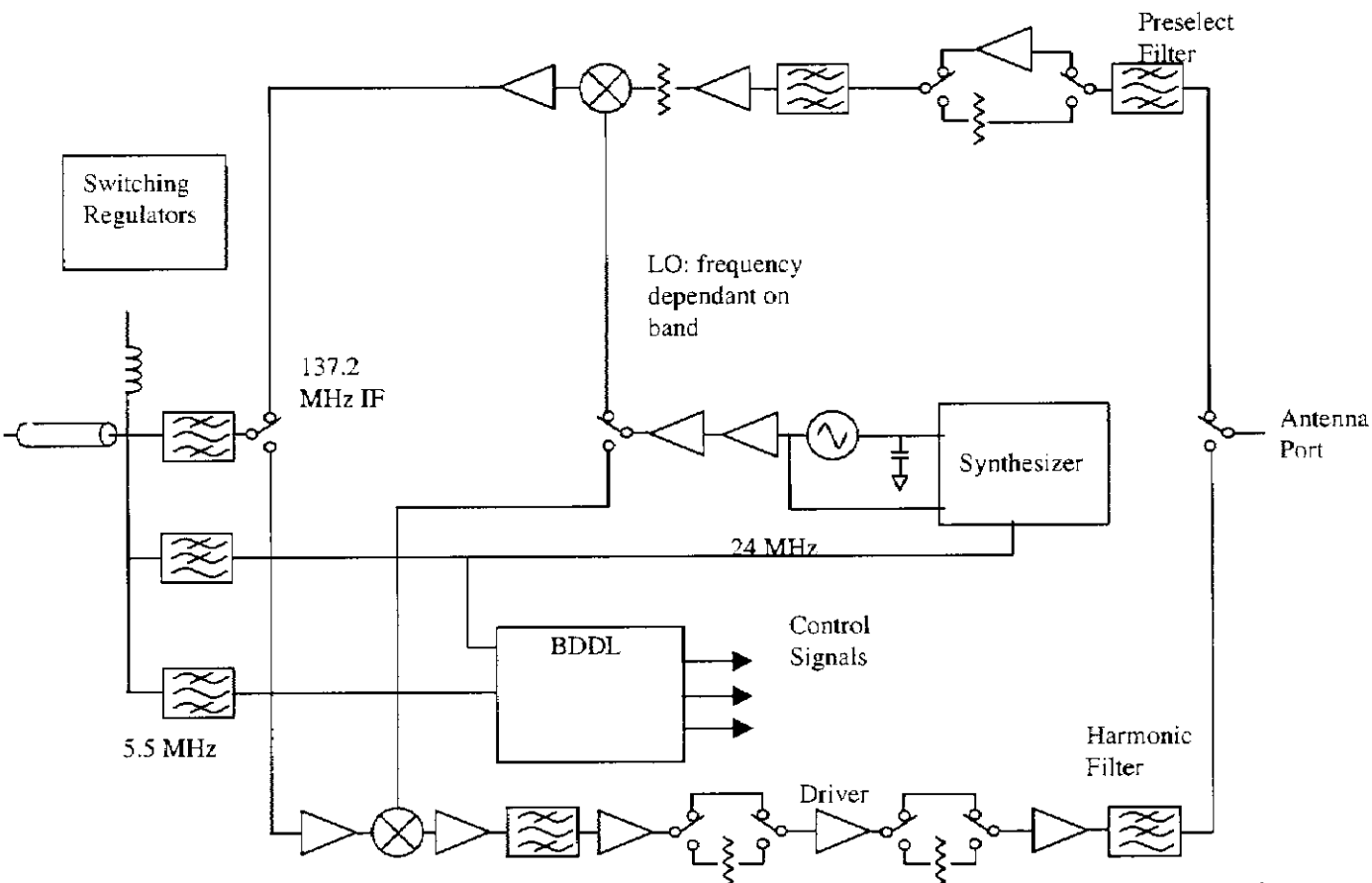
- •RRFM schematic drawing
- •BRFM schematic drawing
- •RF System Design Description
- •Digital Datalink FPGA Design Description

2. Overview and Scope

The purpose of this document is to describe the block level functionality of the RRFM and BRFM. This will include the tuner operation, datalink operation, and power supply operation. Additionally, sub-system specifications derived from the overall RF system specs will be included. Since this document will be mostly common to both the RRFM and BRFM, the term RRFM will imply both modules, except where specifically noted, to improve readability.

These commodity code 03 assemblies are frequency independent designs. In combination with a frequency kit (commodity code 12) they become a frequency specific assembly having a commodity code 02. The main elements of the frequency kits are the ceramic bandpass filters and the synthesizer VCO. These are described later in this document. The frequency kits also contain a number of other passive components related to the synthesizer and PA matching network.

3. Block Diagram



4. Radio Specifications

The specifications for the Receive path and Transmitter path sections are a subset of the RF System specifications. Refer to the Aditus system Principles of operation for more details.

4.1 Receive Path Specifications

Parameter	*Specification Limit*	*Comments*
Noise Figure	8 dB max.	Stepped attenuator disabled.
Input signal level range	RRFM: -32dBm to –98dBm BRFM: -55dBm to -98dBm	Refers to in-band signals only. Refers to single CDMA bearer power.
Input signal level, No damage	RRFM: +10dBm max.	This includes wideband PEP and assumes stepped attenuator is enabled.
Coarse AGC range	25 dB +/-2 dB	
IM3 Rejection (2 Tone)	-30dBc max. for P_{RF} +4dBm to –90dBm per tone.	Stepped attenuator enabled at predetermined power lvl.
Conversion gain	+35 dB typ. max. gain +5 dB typ. min. gain	Stepped attenuator disabled. Stepped attenuator enabled
Image frequency rejection	70 dB	F_{IM} = 1.91GHz +2IF
Half IF (2x2) rejection	70 dB	F_{HALF} = 1.91GHz +IF/2
RF to IF rejection	80 dB	Isolation of Rx path
LO leakage	-13 dBm max.	At antenna jack
Receiver input match	2:1 VSWR max. over operating frequency range.	

4.2 Transmit Path Specifications

Parameter	*Specification Limit*	*Comments*
Transmit power	Maximum Peak Envelope Power: +33.3 dBm Maximum Burst Average Power: +26.5 dBm Maximum Total Average Power: +23 dBm	
Coarse AGC range	17 dB to 51 dB in 17 dB steps.	3 discrete ranges.
Conversion gain (small signal)	+60 dB min (max. gain range) +9 dB min (min. gain range)	Stepped attenuator disabled. Stepped attenuator

		enabled Measurement taken with Pout less than +20 dBm.
IM3 Rejection (2 Tone)	RRFM: -30dBc max. for P_{RF} +25dBm to –42dBm per tone.	Measured at antenna jack. BRFM meas'd at max. power only.
Transmit mask Adj. Channel Alt. Channel Spurious	 -27dBc max., +/-0.84 to 2.51 MHz -40dBc max., +/-2.51 to 4.18 MHz -45dBc max., +/-4.18 to 5.85 MHz	Relative power levels are measured in 1.67 MHz BW with +28 dBm 7-bearer CDMA signal in desired channel
Power level stability	+/- 5dB over full temperature range.	No gain adj.
Power amp stability	2.5:1 VSWR, all angles, over operating frequency range.	Load at antenna jack, tested with +28 dBm output and zero output.
Transmitter output match	2:1 VSWR max. over operating frequency range.	Measured at antenna jack with no output.

4.3 LO Synthesizer Specifications

Parameter	*Specification Limit*	*Comments*
Frequency range	RF frequency + 137.2 MHz	
Phase detector reference frequency	1 MHz	
LO power	+7 dBm min, +15 dBm max.	Measured at mixer LO port.
RMS Phase jitter	+/- 2 degrees max.	
TDD pulling/pushing	+/- 500Hz max. deviation.	

5. Datalink and Interface Specifications

5.1 Datalink Specifications

Refer to the the BDDL Design Description for the specifications and principals of operation.

5.2 Interface Specifications

Parameter	*Specification Limit*	*Comments*
DC Power input	+12V +/-5%, 1A max,	

	muxed via bias-T to coax.	
Reference time base input	24 MHz, 0 dBm min., BPF multiplexed to coax.	
Datalink signal	~5.5 MHz FSK signal, -3 dBm min., BPF multiplexed to coax.	TDD signal
IF signal	137.2 MHz, HPF multiplexed to coax.	TDD signal
RF signal	400 to 2.05 GHz, 2 way spacial diversity antenna connection.	

6. *Description of Operation*

The RRFM basically serves as a remoteable transverter for the IF module which resides in the RSPM. The general topology of the RRFM is a conventional bi-directional, time division duplexed transverter, i.e. the Tx/Rx modes are orthogonal in time to one another. This orthogonal relationship enables use of a common RF channel in both radio modes.

Since the RRFM is a remote unit, all power, timing, data, and RF must be multiplexed onto a single coaxial cable that connects the RRFM to the RSPM. To accomplish this, four separate filters are used. The 137.2 MHz IF is multiplexed through a high pass filter; the 24 MHz reference frequency is passed through a low pass filter, and the 5.5 MHz datalink carrier is passed through a band pass filter. The DC power uses a very simple bias-T arrangement to multiplex power onto the cable.

The FPGA performs two primary functions in the RRFM. First, it serves as a modem interface, delivering timing and control signals, demodulated from the FSK modulated carrier, to the radio, and sending various radio data, via FSK modulated carrier, to the RSPM. Second, it contains the frequency locking mechanism for the 5.5 MHz datalink carrier VCO.

T/R mode switch synchronization occurs under the direct control of the FPGA. The switching of the T/R switches is synchronized to the TX_ON signal in the BSPM. In general, the datalink packet, which contains the timing information, is transmitted by the RSPM a fixed amount of time preceding the actual mode switch event; the packet itself contains delay information referenced to the end of its own packet (or other such predetermined point in time) that instructs the FPGA of the actual instant in time to effect mode switch. The 24 MHz reference is used as the common timebase between the RSPM and RRFM FPGA.

The local oscillator is common to both transmit and receive modes; since the RRFM is time division duplexed on a single RF channel, the LO remains at a fixed frequency. The RRFM employs high side injection, i.e. the LO frequency is greater than the carrier frequency. The LO is synthesized by an integrated PLL device with channel frequency

and spacing an integer multiple of 62 kHz; the time base is the same 24 MHz reference mentioned earlier. The synthesizer receives its programming data from the datalink FPGA.

In transmit mode, the IF carrier is upconverted to the RF frequency. A multi-pole ceramic bandpass filter is used to attenuate the LO leakage and carrier image frequency to a level significantly lower than the carrier level. A series of cascaded small signal amplifiers and stepped attenuators provide the requisite gain and power range control. The two stepped attenuators provide coarse attenuation ranging from 17 dB to 51 dB in 17 dB steps. Fine power control resolution takes place in the RSPM AGC/IF strip. The combined power range control is 70 dB minimum, controlled by the RSPM via the datalink interface. The coarse gain ranges are overlapped to provide several dB of hysteresis. In the BSPM, this power range feature is disabled; the carrier remains at full power at all times during transmit. The PA is a pair of MMIC amplifiers configured as a balanced amplifier; this allows each device to operate at 3 dB less power output than would be the case for a single amplifier device and therefore to operate more linearly.

In receive mode, the RF carrier is downconverted to the same 137.2 MHz IF frequency as used in transmit mode. A wideband, reasonably low loss preselector filter is used at the receiver front end to minimize interference as well as noise figure. A monolithic wideband LNA is switched in parallel with a 17 dB attenuator to provide a total of 30 dB coarse AGC, controlled by the RSPM via the datalink interface. Additional coarse and fine AGC control takes place in the IF portion of the RSPM. Following the LNA is an additional image filter and gain buffer preceding the mixer. A passive mixer is used due to its broadband operation and relatively high linearity. Two additional gain buffers are used following the mixer to provide sufficient system gain prior to being sent to the RSPM.

The power supply consists of two switching (buck type) regulators and three low drop-out linear regulators. The switching regulators supply the higher current demands to improve overall power conversion efficiency; +6.3V is supplied to the PA's and +3V is supplied to numerous amplifiers. A low noise linear regulator is dedicated to the synthesizer and local oscillator to minimize phase noise. The remaining linear regulators supply +9V to the T/R and diversity switches and +5V to various logic devices.