Operational Description of Pacific Microwave Research DT-200S Microwave Video/Audio Transmitter

Introduction

The DT-200S Microwave Video and Audio Transmitter from Pacific Microwave Research is a compact transmitter designed for short-range transmission applications under FCC Part 90 and Part 74. Common uses include law enforcement surveillance and electronic field production. The DT-200 is a compact unit designed for portable and field applications to transmit remote video to a central receive location. The DT-200S is designed to transmit one NTSC (or PAL) video signal plus two high quality audio signals. The DT-200S operates from a nominal +12 Vdc power source and is capable of 0.1Watts of output power. The DT-200S may be equipped with up to 10 channels consistent with parameters listed on the user's FCC station license.

Power Supply

The DT-200S power supply is housed in a common housing with the transmitter and produces all required DC voltages for the operation of the transmitter. Nominal input voltage is in the range of +11 – +36 Vdc with a typical current consumption of 1.2 A @12Vdc. Primary power is applied to J3 Pin A with the return on J3 Pin C. Reverse polarity protection is provided by D2.

Voltage regulator U9 regulates the primary input voltage to +5.0 Vdc for application to the microprocessor (U8), the RF power amplifier (U11), modulator (U16) and subsequent regulation. This +5 Vdc is then converted to 3.3 Vdc by U10 for application to the clock oscillator (U13). U12 converts regulated +5 Vdc to -5 Vdc for application to the video and audio amplifiers (U7, U22, U23, and U24). U14 converts the +5 Vdc regulated voltage to +15 Vdc for application to the phase-lock-loop (PLL U21) and loop filter (U20).

Frequency Generation

The output frequency of the DT-200S is generated by the combination of PLL (U21), loop filter (U20), and VCO (U17). The frequency of operation is loaded into the serial PLL by microprocessor (U8) according to the position of the selector switch (S1) or via RS-232 command (U11). The customer channel table is stored in the microprocessor (U21). Frequency data is input to U21 through RS-232 (U11) at the time of manufacture. A clock oscillator (U13) operates at a frequency of 16 MHz and provides primary frequency stability for the transmitter.

The tuning voltage from U20 is applied to the VCO (U17). The output of U17 is sampled for input to the PLL (U21). The sample signal is compared to the desired frequency and an error tuning voltage is applied to U20 to maintain operating frequency.

Video Modulation

Video modulation is applied to the video encoder module through front panel BNC connector J4. The video encoder converts the analog video signal (NTSC or PAL) to an

MPEG2 compressed digital video signal. The video signal is multiplexed into a serial data stream with the digital audio signal and transformed into a balanced quadrature signal consisting of in-phase (I) and quadrature-phase (Q) signals representing the COFDM waveform. The I/Q signals are applied to the modulator (U1) resulting in an 8 MHz wide digital signal. The output level of the modulator is maintained at a precise level by the combination of U2, U5, and U3. A voltage controlled step attenuator (U2) is controlled by the microprocessor (U8) through a digital-to-analog converter (U5) and dc amplifier (U3) to adjust the modulator level to the voltage-controlled-oscillator (VCO) as the operating frequency is adjusted. Temperature stability is maintained by U4. The leveled output of the modulator (U2) is applied to the VCO (U17).

Audio Modulation

Audio modulation is applied to U24 which acts as a balanced to unbalanced amplifier. Audio levels are controlled via the microprocessor (U8) by the digital attenuator (U22). The output of each audio channel is amplified by U23A:B and then applied to the audio encoder module. The audio encoder digitizes the audio and multiplexes it into a serial data stream along with the video signal as above.

RF Amplification

Modulated RF energy is output from the VCO (U17) and amplified by U18. This output is up-converted by application to a 2X frequency multiplier (U19) and subject to filtering by FL1 and additional gain by U25. The output of U25 is fed to the power amplifier board. The power amplifier board provides additional gain (U2) and filtering (FL1) prior to application to the final amplifier stage (U1).

The RF output of U1 is applied to isolator ISO 1. This provides greater than 20 dB of isolation between the output device and the antenna. The isolator prevents reflections from poor antenna matches from entering the sampling circuit and causing PLL locking problems. Finally, the output is applied to a low pass filter with a cutoff frequency of 3300 MHz. This filter prevents the transmission of any harmonic signals that may have been generated in the transmitter as well as those that could be generated as a result of the non-linear characteristics of the ferromagnetic isolator. The output of the filter is connected to a front panel female SMA connector.

In the event of a PLL unlock condition, the microprocessor (U8) commands the power amplifier (U1) to the standby condition to prevention the transmission of energy on a frequency not licensed to the user.