UAA3537 GSM/EDGE transceiver

Quad-band, one-chip RF transceiver for Class 12 GSM/GPRS/EDGE (Rx + Tx)

Semiconductors

The UAA3537 single-chip transceiver supports GSM/GPRS and the *full* EDGE (Rx + Tx) standard. Only 36 mm² in size, it can operate in the 4 GSM/DCS/PCS bands (850, 900, 1800 and 1900 MHz) used worldwide. Combining a high integration level with high performance, this versatile radio is suitable for many applications - from low cost/highly-integrated handsets up to highly-featured terminals/PDAs.

Key features

- Single-chip RF transceiver in small HVQFN40 package (6 x 6 x 0.85 mm) with quad-band capability: 850, 900, 1800 and 1900 MHz
- GSM/GPRS Class 12 and full EDGE Rx & Tx Class 12 operation
- Low-IF receiver with low noise, wide dynamic range and more than 68 dB gain control
- Direct up-conversion transmitter with excellent noise capabilities (−163 dBc/Hz @ 20 MHz offset) eliminating the need for a SAW filter before the power amplifier (PA)
- Fully-integrated fractional-N synthesizer with AFC control option, fully-differential design to minimize crosstalk and spurs, and all supply regulators, the VCO and reference oscillator are on-chip
- Functions from a 2.4–3.0 V supply
- Outputs to control front-end switches (pin diodes) and 3-wire serial bus interface
- Compatible with Philips' 3G (WCDMA) RF chipset, optimized for Philips' 2G/2.5G baseband and PA, and provides the RF core of Philips' 2.5G system solutions.

General information

The UAA3537 is a complete RF solution for developing cost- and performance-optimized 2G, 2.5G/EDGE handsets and terminals. The IC is a 3rd generation Philips Semiconductors GSM RF transceiver, using Philips' pioneering Near-Zero IF (N-ZIF) architecture in the receiver. Now recognized (and copied) by many, this is the most cost-effective and performance-capable receiver architecture.

The transmitter architecture uses a new, direct up-conversion approach. Leveraging the advantages of Philips Semiconductors' advanced BiCMOS process (QUBiC 4), this provides the necessary transmit noise performance without using any transmit SAW filters. And it's this architecture that makes the transmitter not only compliant with EDGE, but also very cost-effective.

The IC's high level of integration has also made it cost-effective to have four receiver Low Noise Amplifiers (LNAs) on-chip. Though suitable for quad-band applications, not all have to be used. LNAs are simply enabled or disabled by programming, making it easy for manufacturers to have compatible designs between different platforms: dual band, triple band or quad band. For example, triple band platforms can use this flexibility to enable any of the following configurations:

- 850 + 1800 + 1900 or 900 + 1800 + 1900 MHz
- 850 + 900 + 1800 or 850 + 900 + 1900 MHz.

The UAA3537 is optimized to work with Philips Semiconductors' baseband and power amplifier (PA) products. Full system functionality has been successfully proven — the UAA3537 is essentially the radio in our widely-used 2.5G system solution. What's more, the IC can be combined with our 3G (UMTS) RF chipset in multimode phones, where it also delivers the reference clock for cross-mode synchronization and optimization.

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In summary, the UAA3537 offers a unique feature set in the mobile communications market by combining the following capabilities:

- a very high integration level
- complete flexibility for many application/phone designs
- a low bill-of-materials for all system developments - from dual band to quad band, and from GSM up to full EDGE.

Key blocks in detail

Receiver

The receiver consists of the RF receive front-end and the IF section. The front-end amplifies the GSM (869–894 or 925–960 MHz), DCS (1805–1880 MHz) or PCS (1930–1990 MHz) antenna signal and down-converts the chosen channel to a low IF of 100 kHz, providing more than 35 dB image suppression. Of the four on-chip LNAs, two are connected to the same package outputs - selectivity is provided by an on-chip low-pass filter. Channel selectivity is provided by a high-performance integrated band-pass filter. The IF section then amplifies the selected channel, performs gain control to tune the output level to the required value and rejects DC. For the latter, an active high-pass circuit can be programmed to either operate continuously or keep an acquired DC offset correction during the burst.

Transmitter

The transmitter is fully differential and uses a direct, up-conversion architecture. It consists of a single-sideband power up-mixer. Gain is set over 40 dB via the 3 wire serial programming bus. The fully-integrated VCO and the power mixer provide local oscillator (LO) suppression, quadrature phase-error correction, quadrature amplitude balance and a low noise-floor to meet system specifications without a SAW filter.

IC control

The circuit can be powered-up into four different modes - Rx, Tx, Syn or Ref mode - depending on the particular supply voltages applied, the logical level at the Ctrl pin, and the 3-wire serial bus programming. In Rx or Tx mode, all sections required for receiving/transmitting are turned on. The Syn mode is used to power-up the Synthesizer and the VCO prior to the Rx or Tx mode. In the Syn mode, some internal LO buffers are also powered-up so that VCO-pulling is minimized when switching on the receiver or transmitter. The Reference Oscillator (Ref mode) is turned on by applying the appropriate supply voltage (see below). Additionally, the band is selected by programming the IC via the 3-wire serial bus, enabling the required LNAs.

Reference oscillator

The heart of the reference oscillator (26 MHz) is an integrated amplifier - externally only a quartz crystal and few passive components are needed. After buffering, a reference clock of 26 MHz is supplied to other parts of the system through the pin CLKOUT (see Fig.1). An internal supply voltage regulator using $V_{CC(SYN)}$ as input supplies the reference oscillator and minimizes parasitic couplings and pushing. Automatic Frequency Control (AFC) can be performed by the fractional-N synthesizer programming or via an external varactor. Additionally, a coarse AFC control with a resolution of 8 bits is integrated via switchable capacitors. The programming of the coarse AFC capacitors is maintained during sleep mode as the register memory is supplied via the continuous digital supply V_{DD}. If required, a pin is also available for an external 26 MHz reference source.

Local oscillator

LO signals are provided by the on-chip VCO to operate the receiver and transmitter. The VCO is fully integrated and self-calibrating to reduce manufacturing tolerances. The frequencies are set by the internal fractional-N synthesizer PLL circuit, programmable via the 3-wire serial bus. The quadrature-phase LO signals required for IQ mixers are generated internally.

Control of front-end switches

Outputs are provided to drive the RF switches and PA module for the various cellular and DCS/PCS frequency bands.

N-ZIF architecture

The N-ZIF architecture integrates many different features including a high dynamic range IF channel filter, a low-noise amplifier (LNA) with image-rejecting front end, fractional N frequency synthesizers and a transmit offset loop with integrated filters. It provides a definitive advantage compared to Zero-IF (ZIF) solutions in terms of immunity to interference, and the costs/time of RF development and manufacturing. In addition to providing simplified signal processing for GSM applications, the high integration level it achieves provides significant further cost and size reductions.

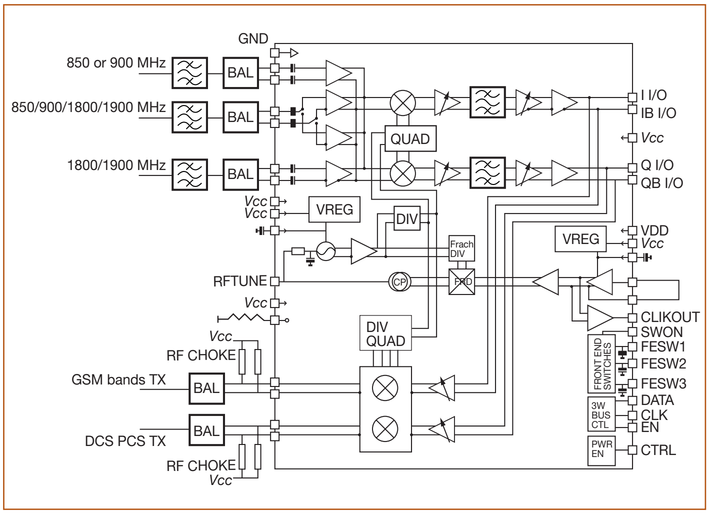

Fig.1 Inside the UAA3537 transceiver

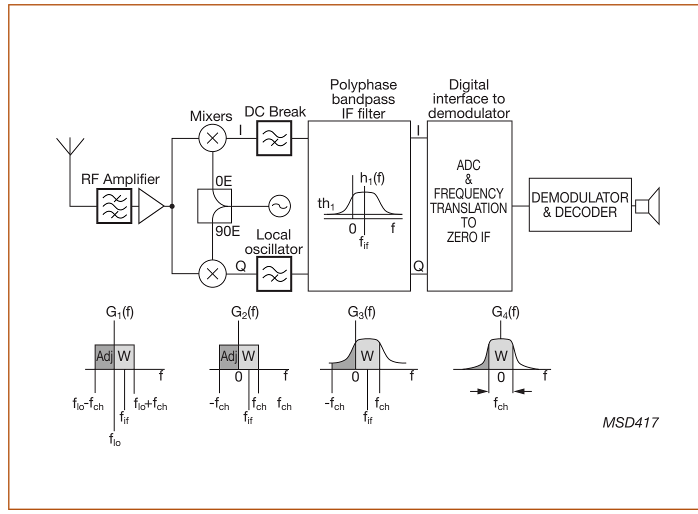

Fig.2 Near-Zero IF architecture used in the receiver — it eliminates the need for an external SAW filter and also prevents DC errors by allowing a DC break to be inserted into the IF path

Direct up-mixer architecture

Two main architectures are competing for use in the phone transmitter for GSM-based cellular standards: the closed-loop modulation concept and the direct up-mixer concept.

Closed-loop modulation has been very efficient and successful for the GSM standard, since this architecture too, did not require any SAW filters. And until recently, silicon processes weren't capable of realizing direct up-mixer architectures. But now, the arrival of EDGE significantly complicates the required performance of transmitter architectures by adding an amplitude modulation requirement on top of GMSK.

For EDGE, the closed-loop concept now needs to have two different loops: one for the phase and the other for the amplitude. The issue is then to have both these loops synchronized. A tiny offset in synchronization of anything more than 39 nanoseconds would lead to significant modulation spectrum degradation, and the concept would not meet EDGE requirements. Such synchronization constraints mean there's a high technical risk in using closed-loop architectures for EDGE, especially when it comes to application or temperature variations.

After Philips Semiconductors developed the QUBiC 4 BiCMOS process, it had a technology capable of manufacturing silicon direct up-mixer

architectures. This was done for other standards (CDMA and 3G) and the company now has quite some experience and expertise with this concept. Thanks to this, we are now able to integrate the direct up-mixer architecture in a single-chip RF transceiver IC.

Today, thanks to the QUBiC 4 we are leading the way in direct up-mixer architectures for GSM and EDGE standards. With the UAA3537, we can still offer manufacturers the size and cost advantages of not using any SAW filters in their transmit chain and offer the full EDGE guarantee.

Future

The UAA3537 is a clear step forward to multimode transceivers and the IC shares both a common architecture and process technology with the other main RF ICs from Philips Semiconductors.

With this new UAA3537 core block manufactured in our QUBiC 4 process, as well as our existing 3G chipset (UAA3580/81) manufactured in the same process, we are now ready for the convergence of standards in the coming years.

Validation and performance guarantee

The UAA3537 concept, specifications and detailed performance characteristics are studied and verified in several ways. Firstly, the architecture studies are done across circuit boundaries, taking into consideration not only the RF transceiver, but also baseband and PA IC performance capabilities. These studies and validations across the whole chipset mean that Philips' UAA3537 transceiver is one of the first fully validated EDGE solutions on the market.

All delivered ICs are tested on their critical RF parameters, guaranteeing a high quality level for final applications. As a single-chip transceiver, this guarantee is even more important for an application developer since the tested and guaranteed parameters will, in turn, directly guarantee the performance of the final application/product.

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Tools

A wide set of development tools are available to support customers including:

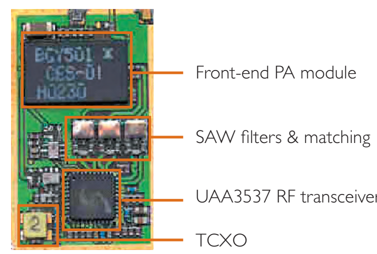
- UAA3537 RF transceiver measurement board & lab control software
- B3 reference board for complete 2.5G sub-system (triple band GSM & GPRS) and lab control software
- B3E reference board for complete 2.5G+ sub-system (triple band GSM/GPRS/EDGE) and lab control software
- Complete system solution reference design for 2G and 2.5G applications.

Technology

The UAA3537 is manufactured in Philips Semiconductors' high-performance BiCMOS process: QUBiC 4 (0.25 µm, F_t = 40 GHz, F_{max} = 90 GHz).

Availability

UAA3537 samples are available now and mass production will start in Q2 2003 (part number: UAA3537HN/C1).



B3 reference board for the UAA3537

Features:

- Complete RF sub-system
- GSM/GPRS class 12 / EDGE Rx
- Triple band (800 or 900 + 1800 + 1900 MHz)
- 450 mm^2

Fig.3 A reference design based on the UAA3537

Philips Semiconductors

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