BGM220S Wireless Gecko Bluetooth® Module Data Sheet

The BGM220S is a module designed and built to meet the performance, security, and reliability requirements of battery-powered IoT products running on Bluetooth networks.

Based on the EFR32BG22 SoC, the BGM220S enables Bluetooth® Low Energy connectivity while delivering best-in-class RF range and performance, future-proof capability for feature and OTA firmware updates, enhanced security features, and low energy consumption.

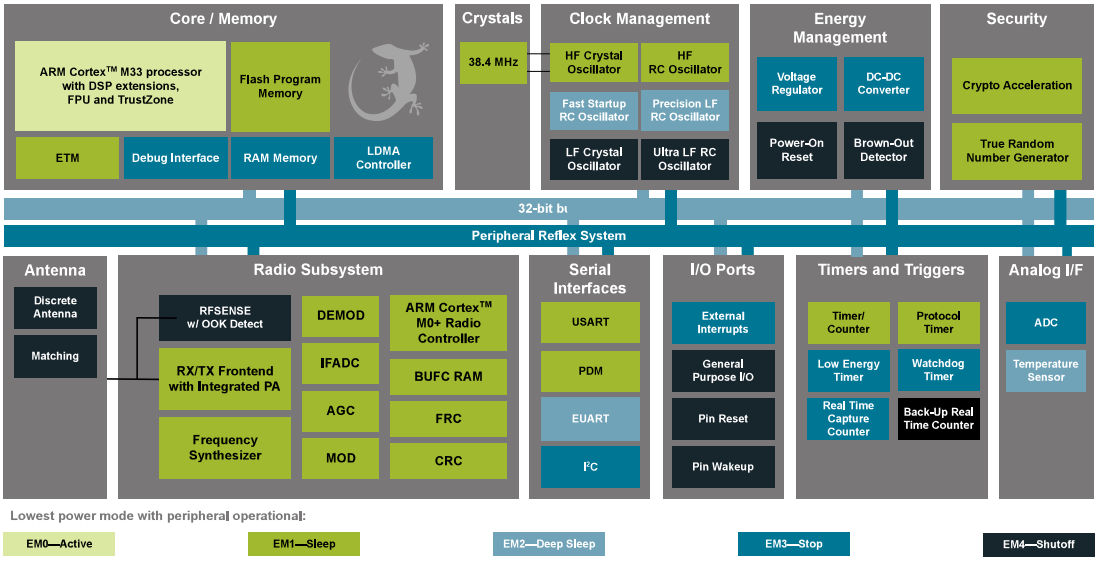
BGM220S modules are a full solution that comes with fully-upgradeable, robust software stacks, world-wide regulatory certifications, advanced development and debugging tools, and support that will minimize and simplify the engineering and development of your end-products helping to accelerate their time-to-market.

The BGM220S is intended for a broad range of applications, including:

- Asset Tags and Beacons
- Portable Medical
- Sports, Fitness, and Wellness devices
- Connected Home
- Industrial and Building Automation
- Bluetooth mesh Low Power Nodes

KEY FEATURES

- Bluetooth 5.4
- Built-in antenna or RF pin
- Up to 6 dBm TX power
- -98.6 dBm BLE RX sensitivity at 1 Mbps
- 32-bit ARM Cortex-M33 core at up to 76.8 MHz
- 512/32 kB of Flash/RAM memory
- Optimal selection of MCU peripherals
- 25 GPIO pins
- 6 mm × 6 mm × 1.1 mm



1. Feature List

- **Supported Protocols**
  - Bluetooth Low Energy (Bluetooth 5.4)
    - Direction finding
    - 1M, 2M, and LE Coded PHYs
  - Bluetooth Mesh Low Power Node
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to 6 dBm
  - High-performance 32-bit ARM Cortex-M33® with DSP instruction and floating-point unit for efficient signal processing
  - Up to 512 kB flash program memory
  - 32 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **High Receiver Performance**
  - -106.4 dBm sensitivity (0.1% BER) at 125 kbps GFSK
  - -102.3 dBm sensitivity (0.1% BER) at 500 kbps GFSK
  - -98.6 dBm sensitivity (0.1% BER) at 1 Mbps GFSK
  - -95.9 dBm sensitivity (0.1% BER) at 2 Mbps GFSK
- **Low-Energy Consumption**
  - 4.2 mA RX current at 1 Mbps GFSK
  - 4.6 mA TX current at 0 dBm output power
  - 26 µA/MHz in Active Mode (EM0)
  - 1.40 µA EM2 DeepSleep current (RTCC running from LFXO, Full RAM retention)
- **Regulatory Certifications**
  - CE and UKCA - EU and UK
  - FCC - USA
  - ISED - Canada
  - MIC - Japan
  - KC - South Korea
  - NCC - Taiwan
  - ANATEL - Brazil
- **Wide Operating Range**
  - 1.8 to 3.8 V
  - -40 to +105 °C and -40 to +85 °C Versions Available
- **Dimensions**
  - 6 mm × 6 mm × 1.1 mm
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **Wide Selection of MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 25 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 1 × Enhanced Universal Asynchronous Receiver/Transmitter (EUART)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - RFSENSE with selective OOK mode

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	TX Power Rating	Max CPU Speed	Antenna	RF Shield	Flash (kB)	RAM (kB)	GPIO	Temp Range	Packaging
BGM220SC12WGA2	Bluetooth 5.4	0 dBm	38.4 MHz	Built-in	No	352	32	25	-40 to 85 °C	Cut Tape
BGM220SC12WGA2R	Bluetooth 5.4	0 dBm	38.4 MHz	Built-in	No	352	32	25	-40 to 85 °C	Reel
BGM220SC22HNA2	Bluetooth 5.4 • Direction Finding Rx	6 dBm	76.8 MHz	Built-in	Yes	512	32	25	-40 to 105 °C	Cut Tape
BGM220SC22HNA2R	Bluetooth 5.4 • Direction Finding Rx	6 dBm	76.8 MHz	Built-in	Yes	512	32	25	-40 to 105 °C	Reel
BGM220SC22WGA2	Bluetooth 5.4	6 dBm	76.8 MHz	Built-in	Yes	352	32	25	-40 to 85 °C	Cut Tape
BGM220SC22WGA2R	Bluetooth 5.4	6 dBm	76.8 MHz	Built-in	Yes	352	32	25	-40 to 85 °C	Reel

Note:

1. End-product manufacturers must verify that the module is configured to meet regulatory limits for each region in accordance with the formal certification test reports.
2. Devices are pre-programmed with BGAPI UART DFU bootloader v1.10.2.
3. Throughout this document, the devices in the table above may be referred to by their product family name (e.g. BGM220S), by their model name (BGM220S12A for 0 dBm TX power, BGM220S22A for 6 dBm TX power), or by the full ordering code.
4. LE Long Range (125 kbps and 500 kbps) PHYs are only supported on part numbers which include direction-finding capability.
5. In accordance with the Bluetooth specification, the module operates over the following frequency range: 2402 - 2480 MHz. The module is also capable of operating in a separate BLE-like custom SRD transmit-only mode where proprietary packets are sent over the channels 2401 MHz and 2481 MHz using the same 1 Mbps GFSK modulation.
6. All devices in the table above support transmitting CTE (Constant Tone Extension) which is required in Direction Finding, but only specific devices support CTE receive. These devices are marked with "Direction Finding Rx" in the Protocol Stack Column.
7. The **SLWSTK6103A Wireless Starter Kit** is available for BGM220S evaluation and development, as well as the **SLWRB4312A** radio board.

Table of Contents

3. System Overview

3.1 Introduction

The BGM220S module combines an energy-friendly MCU with a highly integrated radio transceiver in a SiP module with a robust, integrated antenna. This section gives a short introduction to the features of the module.

The block diagram for the BGM220S module is shown in the figure below. The wireless module includes the EFR32BG22 wireless System on a Chip (SoC), required decoupling capacitors and inductors, 38.4 MHz crystal, RF matching circuit, and integrated antenna.

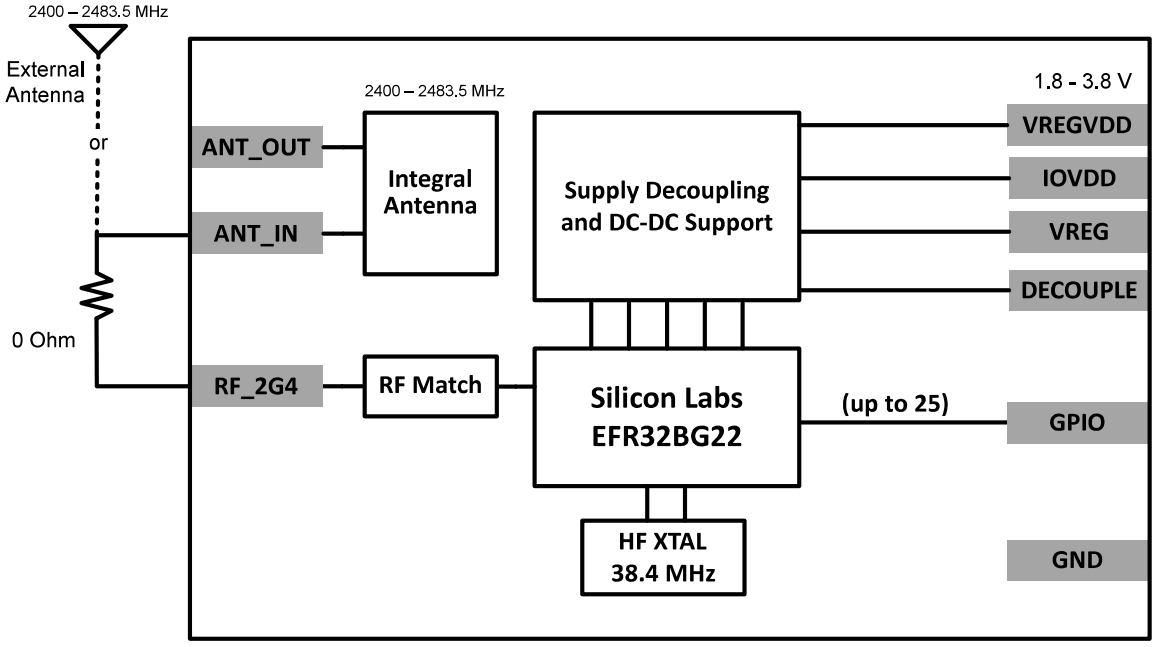


Figure 3.1. BGM220S Block Diagram

A simplified internal schematic for the BGM220S module is shown in the figure below.

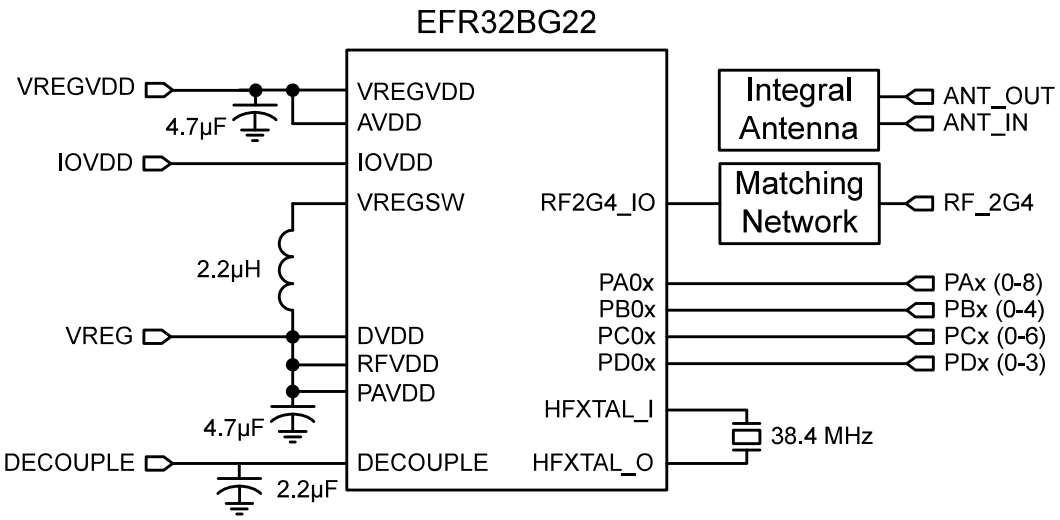


Figure 3.2. BGM220S Module Schematic

3.2 EFR32BG22 SoC

The EFR32BG22 SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 512 kB of flash memory, a rich set of MCU peripherals, and various clock management and serial interfacing options. Consult the EFR32xG22 Wireless Gecko Reference Manual and the EFR32BG22 Data Sheet for details.

3.3 Antenna

BGM220S modules include an integral antenna on board with the characteristics detailed in the tables below.

Table 3.1. Antenna Efficiency and Peak Gain (BGM220S12A)

Parameter	With optimal layout	Note
Efficiency	-1.4 to -2.6 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to 7. Design Guidelines for recommendations to achieve optimal antenna performance.
Peak gain	1.5 dBi	

Table 3.2. Antenna Efficiency and Peak Gain (BGM220S22A)

Parameter	With optimal layout	Note
Efficiency	-1 to -2 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to 7. Design Guidelines for recommendations to achieve optimal antenna performance.
Peak gain	2.3 dBi	

3.4 Power Supply

The BGM220S requires a single nominal supply level of 3.0 V to operate. All necessary decoupling and filtering components are included in the module, and the supply is fully regulated internally.

4. Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VREGVDD supply at 3.0 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+125	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Junction temperature	T_{JMAX}	-G grade	—	—	+105	°C
		-N grade	—	—	+105	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
Input RF level on RF pin RF_2G4	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pin RF_2G4	V_{MAX2G4}		-0.3	—	V_{VREG} + 0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

4.2 General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specifed over this operating range, unless otherwise noted.

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade	-40	—	+85	°C
		-N temperature grade	-40	—	+105	°C
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DCDC in regulation[1]	2.2	3.0	3.8	V
		DCDC in bypass	1.8	3.0	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	76.8	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2	—	—	50	MHz
		VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency[2]	f_{RHCLK}	VSCALE2 or VSCALE1	—	38.4	—	MHz

Note:

1. The supported maximum $V_{VREGVDD}$ in regulation mode is a function of temperature and 10-year lifetime average load current. See more details in 4.2.1 DC-DC Operating Limits.
2. The recommended radio crystal frequency is 38.4 MHz. Any crystal frequency other than 38.4 is expressly not supported.

4.2.1 DC-DC Operating Limits

The maximum supported voltage on the VREGVDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 4.1 Lifetime average load current limit vs. Maximum input voltage on page 10 shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, an application that is continuously powered which spends 99% of the time asleep consuming 2 µA and 1% of the time active and consuming 10 mA has an average lifetime load current of about 102 µA.

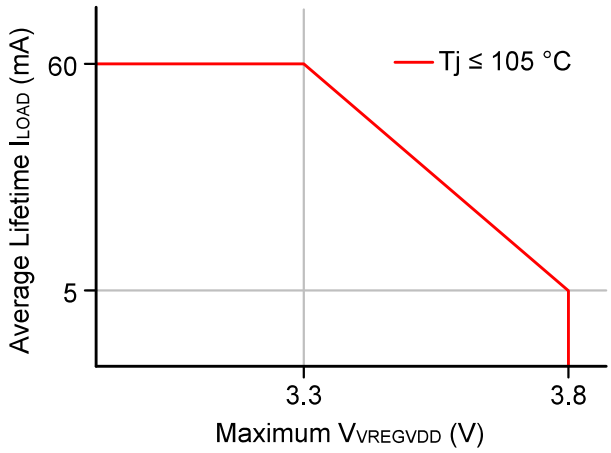


Figure 4.1. Lifetime average load current limit vs. Maximum input voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4.2 Transient maximum load current vs. Minimum input voltage on page 10 shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

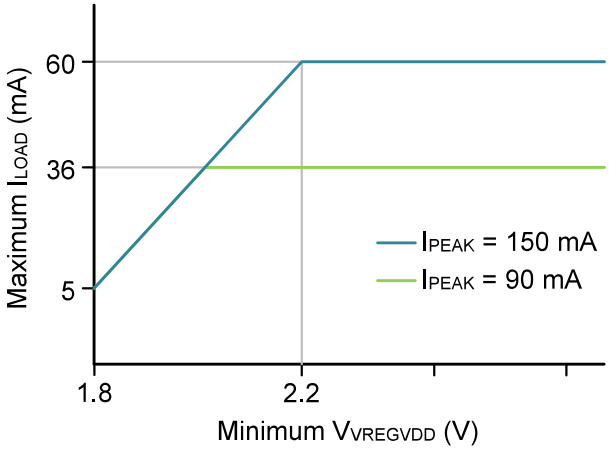


Figure 4.2. Transient maximum load current vs. Minimum input voltage

4.3 MCU Current Consumption with 3 V Supply

Unless otherwise indicated, typical conditions are: Module supply voltage = 3.0 V. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.3. MCU Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	27	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	37	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	28	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	38	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	28	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	17	—	µA/MHz
		38.4 MHz crystal	—	17	—	µA/MHz
		38 MHz HFRCO	—	13	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO in precision mode	—	1.75	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.32	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	1.66	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.21	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.20	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.05	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4 mode	I_{EM4}	No BURTC, No LF Oscillator, DCDC bypassed	—	0.17	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.37	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

4.4 Radio Current Consumption with 3 V Supply

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.4. Radio Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.8	—	mA
System current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.7	—	mA
System current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm output power	—	4.6	—	mA
		f = 2.4 GHz, CW, 6 dBm output power	—	8.8	—	mA

4.5 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 4.5. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power[1]	$POUT_{MAX}$	6 dBm output power	—	6.0	—	dBm
		0 dBm output power	—	-0.5	—	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-27	—	dBm
Output power variation vs VREGVDD supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	6 dBm output power with VREGVDD voltage swept from 1.8 V to 3.0 V	—	0.04	—	dB
		0 dBm output power, with VREGVDD voltage swept from 1.8 to 3.0 V	—	0.04	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	6 dBm output power, (-40 to +105 °C)	—	0.2	—	dB
		0 dBm output power, (-40 to +105 °C)	—	1.3	—	dB
		6 dBm output power, (-40 to +85 °C)	—	0.1	—	dB
		0 dBm output power, (-40 to +85 °C)	—	1.0	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	6 dBm output power	—	0.09	—	dB
		0 dBm output power	—	0.15	—	dB

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.6 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 4.6. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

4.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 4.7. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-98.6	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-97.2	—	dBm
		With non-ideal signals[3 1]	—	-96.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-6.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-6.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-39.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-45.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-46.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-23.5	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-6.6	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-17.1	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 4.8. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-95.9	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-94.3	—	dBm
		With non-ideal signals[3 1]	—	-94.0	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	8.8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-9.2	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-6.6	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 5 4 6]	—	-43.3	—	dB
		Interferer is reference signal at -4 MHz offset[1 5 4 6]	—	-44.0	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 5 4 6]	—	-48.6	—	dB
		Interferer is reference signal at -6 MHz offset[1 5 4 6]	—	-50.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-23.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 6]	—	-43.3	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 6]	—	-9.2	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-18.8	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -64 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 4.9. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-102.3	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-100.9	—	dBm
		With non-ideal signals[3 1]	—	-99.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	2.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-8.0	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-7.9	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-46.5	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-49.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-48.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-53.8	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-48.3	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-49.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-46.5	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -72 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.

4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 4.10. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-106.4	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-106.0	—	dBm
		With non-ideal signals[3 1]	—	-105.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-13.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-13.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-55.8	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-53.7	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-59.0	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-52.7	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-53.7	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -79 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.

4.11 High-Frequency Crystal

Table 4.11. High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	38.4	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-10	—	10	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-20	—	20	ppm

4.12 Low Frequency Crystal Oscillator

Table 4.12. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kOhm, CL = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	357	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kOhm, CL = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	63	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.13 Precision Low Frequency RC Oscillator (LFRCO)

Table 4.13. Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	204	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	175	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	655	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.14 GPIO Pins

Unless otherwise indicated, typical conditions are: IOVDD = 3.0 V.

Table 4.14. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3*IOVDD	V
		RESETn	—	—	0.3*DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7*IOVDD	—	—	V
		RESETn	0.7*DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*IOVDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.15 Microcontroller Peripherals

The MCU peripherals set available in BGM220S modules includes:

- ADC: 12-bit at 1 Msps, 16-bit at 76.9 ksps
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- EUART (UART/IrDA)
- I^2C peripheral interfaces
- PDM interface
- 12 Channel Peripheral Reflex System

For details on their electrical performance, consult the relevant portions of Section 4 in the SoC datasheet.

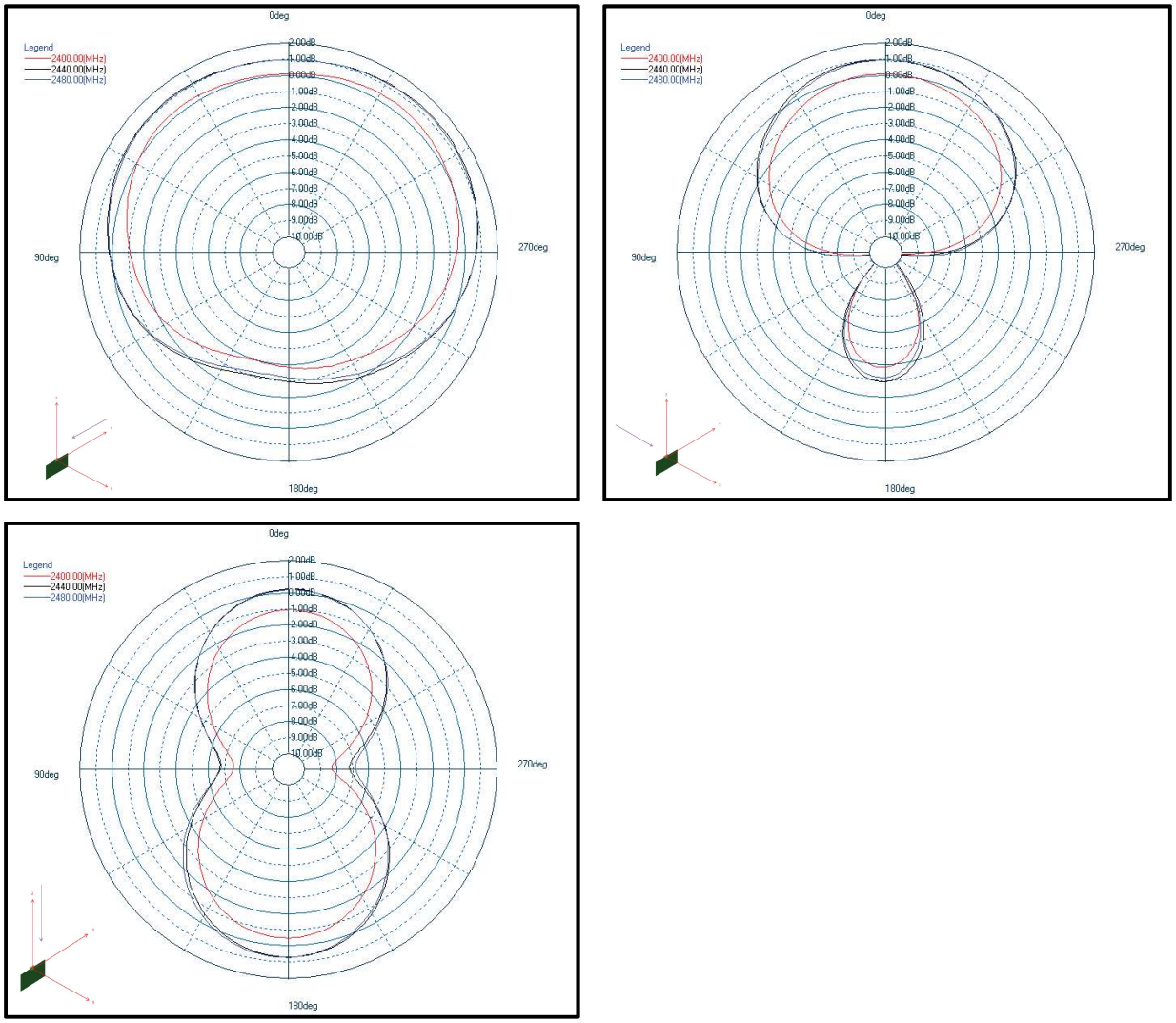
To learn which GPIO ports provide access to every peripheral, consult Analog Peripheral Connectivity and Digital Peripheral Connectivity.

4.16 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

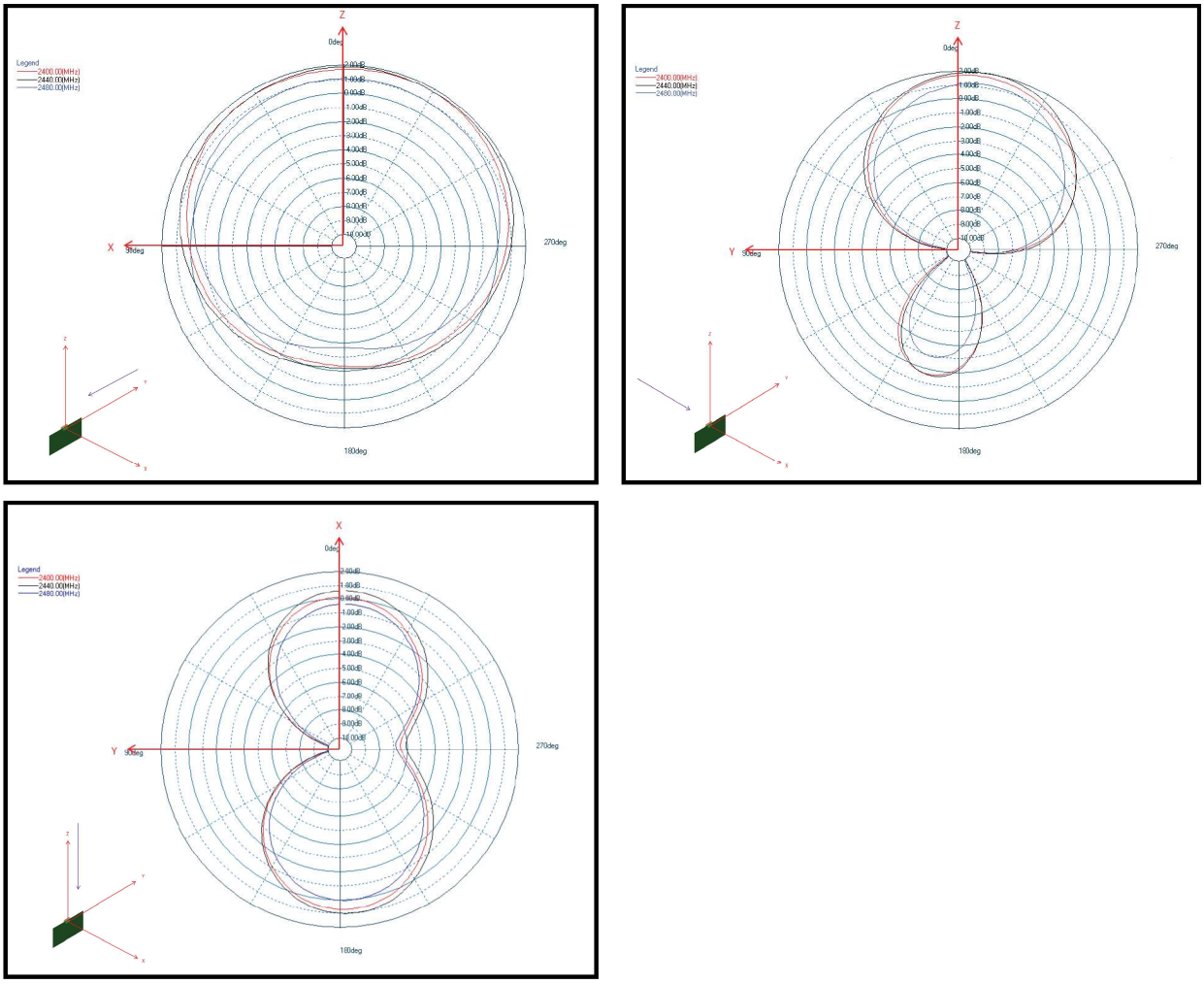
4.16.1 Antenna Typical Characteristics

Typical BGM220S radiation patterns for the on-board chip antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.



Top Left: Phi 0°, Top Right: Phi 90°, Bottom Left: Theta 90°

Figure 4.3. BGM220S12A Typical 2D Antenna Radiation Patterns on 50 mm x 30 mm board



Top Left: Phi 0°, Top Right: Phi 90°, Bottom Left: Theta 90°

Figure 4.4. BGM220S22A Typical 2D Antenna Radiation Patterns on 55 mm x 20 mm board

5. Reference Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The BGM220S can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. For more details, refer to *AN958: Debugging and Programming Interfaces for Custom Designs*.

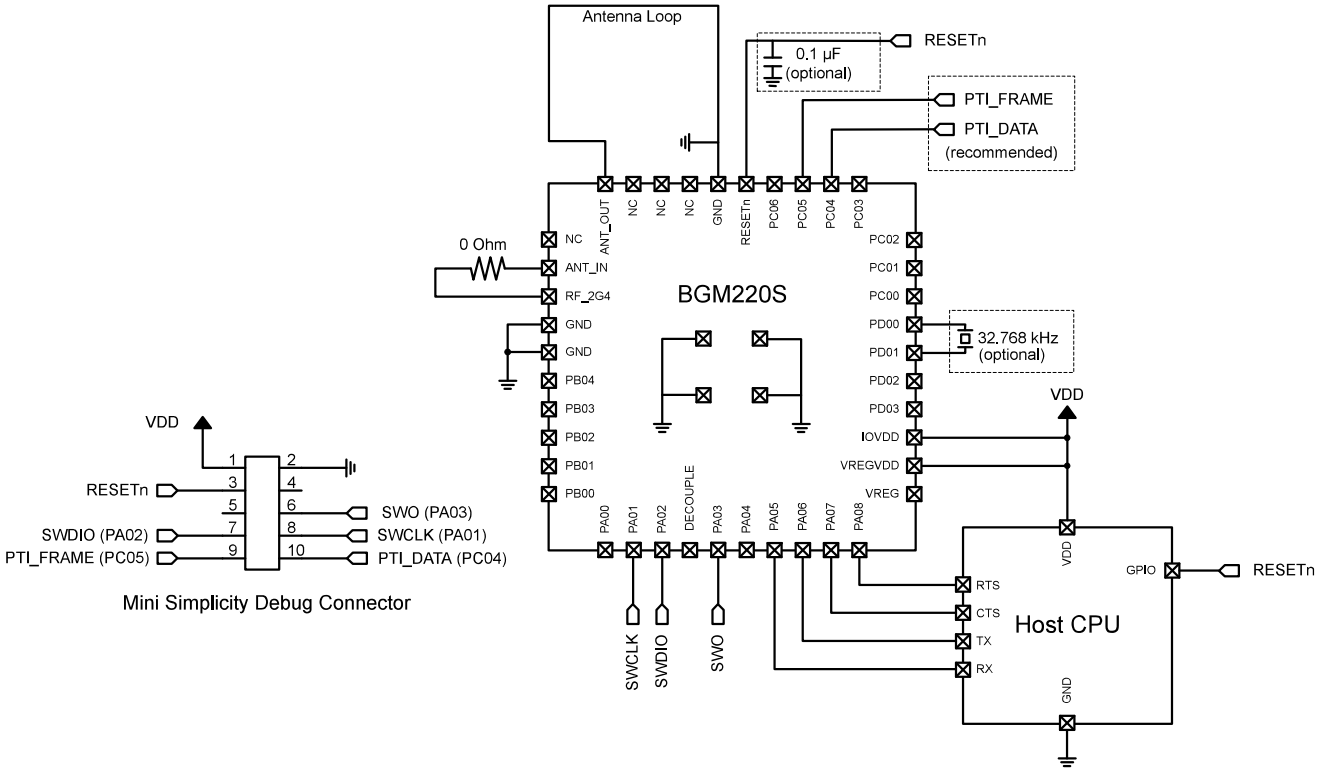


Figure 5.1. UART NCP Configuration

5.2 SoC Application

The BGM220S can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below. For more details, refer to *AN958: Debugging and Programming Interfaces for Custom Designs*.

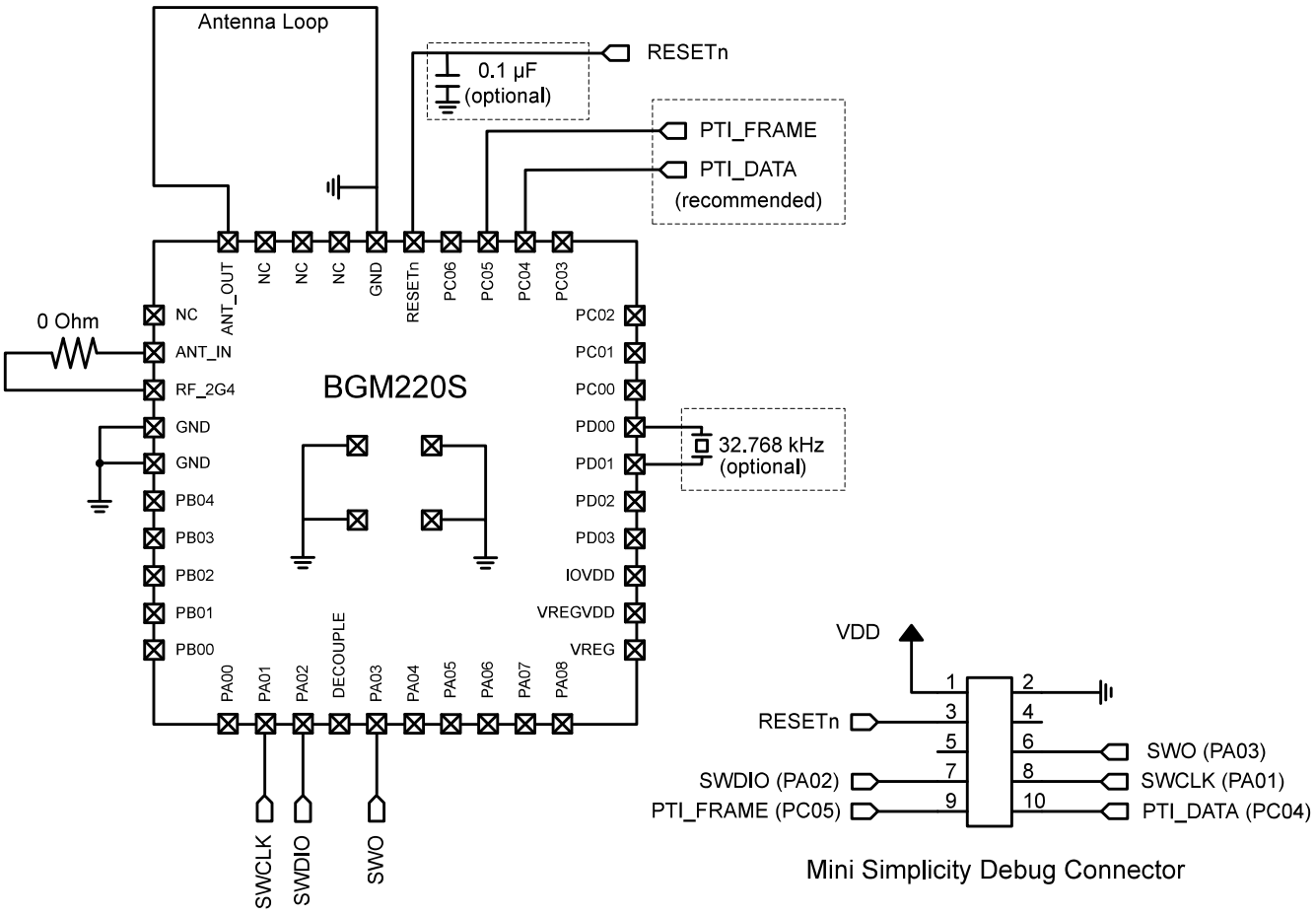


Figure 5.2. Stand-Alone SoC Configuration

6. Pin Definitions

6.1 44-Pin SiP Module Device Pinout

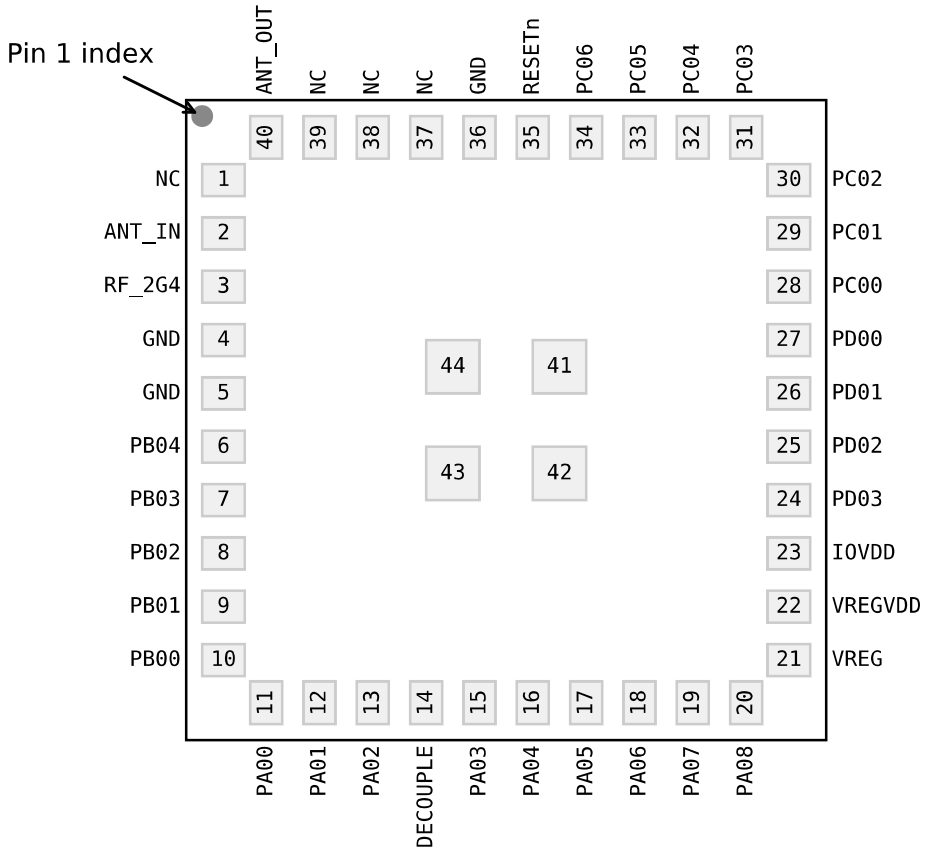


Figure 6.1. 44-Pin SiP Module Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.2 Alternate Function Table, 6.3 Analog Peripheral Connectivity, and 6.4 Digital Peripheral Connectivity.

Table 6.1. 44-Pin SiP Module Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
NC	1	Do not connect	ANT_IN	2	Antenna In
RF_2G4	3	2.4 GHz RF input/output	GND	4	Ground
GND	5	Ground	PB04	6	GPIO
PB03	7	GPIO	PB02	8	GPIO
PB01	9	GPIO	PB00	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA00	11	GPIO	PA01	12	GPIO
PA02	13	GPIO	DECOUPLE	14	Decouple output for on-chip voltage regulator. This pin is internally decoupled, and should be left disconnected.
PA03	15	GPIO	PA04	16	GPIO
PA05	17	GPIO	PA06	18	GPIO
PA07	19	GPIO	PA08	20	GPIO
VREG	21	Regulated supply voltage. This pin is internally connected to the SoC DVDD, RFVDD, and PAVDD supply lines. It is not intended to power external circuitry.	VREGVDD	22	Module input power supply. This pin is internally connected to the SoC AVDD and VREGVDD supply lines.
IOVDD	23	I/O power supply	PD03	24	GPIO
PD02	25	GPIO	PD01	26	GPIO
PD00	27	GPIO	PC00	28	GPIO
PC01	29	GPIO	PC02	30	GPIO
PC03	31	GPIO	PC04	32	GPIO
PC05	33	GPIO	PC06	34	GPIO
RESETn	35	Reset Pin. The RESETn pin is internally pulled up to VREG (DVDD).	GND	36	Ground
NC	37	Do not connect	NC	38	Do not connect
NC	39	Do not connect	ANT_OUT	40	Antenna Out
GND	41	Ground	GND	42	Ground
GND	43	Ground	GND	44	Ground

6.2 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

Table 6.2. GPIO Alternate Function Table

GPIO	Alternate Functions			
PB03	GPIO.EM4WU4			
PB01	GPIO.EM4WU3			
PB00		IADC0.VREFN		
PA00		IADC0.VREFP		
PA01	GPIO.SWCLK			
PA02	GPIO.SWDIO			
PA03	GPIO.SWV GPIO.TDO GPIO.TRACEDATA0			
PA04	GPIO.TDI GPIO.TRACECLK			
PA05	GPIO.EM4WU0			
PD02	GPIO.EM4WU9			
PD01		LFXO.LFXTAL_I LFXO.LF_EXTCLK		
PD00		LFXO.LFXTAL_O		
PC00	GPIO.EM4WU6 GPIO.THMSW_EN			
PC05	GPIO.EM4WU7			

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is avaliable on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Table 6.3. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 6.4. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUART0.CTS	Available	Available	Available	Available
EUART0.RTS	Available	Available	Available	Available
EUART0.RX	Available	Available	Available	Available
EUART0.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

7. Design Guidelines

7.1 Layout and Placement

For optimal performance of the BGM220S the following guidelines are recommended:

- Place the module 1.50 mm from the edge of the copper “keep-in” area at the middle of the long edge of the application PCB, as illustrated in Figure 7.1 Recommended Layout for BGM220S on page 32.
- Copy the exact antenna design from Figure 7.2 Antenna Layout With Coordinates on page 33 with the values for coordinates A to L given in Table 7.1 Antenna Polygon Coordinates, Referenced to Center of BGM220S on page 33.
- Make a cutout in all lower layers aligned with the right edge and the bottom edge of the antenna as indicated by the yellow box in Figure 7.3 Antenna Clearance in Inner and Bottom Layers on page 34.
- Connect all ground pads directly to a solid ground plane in the top layer.
- Connect RF_2G4 to ANT_IN through a 0-ohm resistor.
  - The 0-ohm gives the ability to test conducted and to evaluate the antenna impedance in the design.
- Place ground vias as close to the ground pads of the BGM220S as possible.
- Place ground vias along the antenna loop right and bottom side.
- Place ground vias along the edges of the application board.
- Do not place plastic or any other dielectric material in contact with the antenna.
  - A minimum clearance of 0.5 mm is advised.
  - Solder mask, conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region.

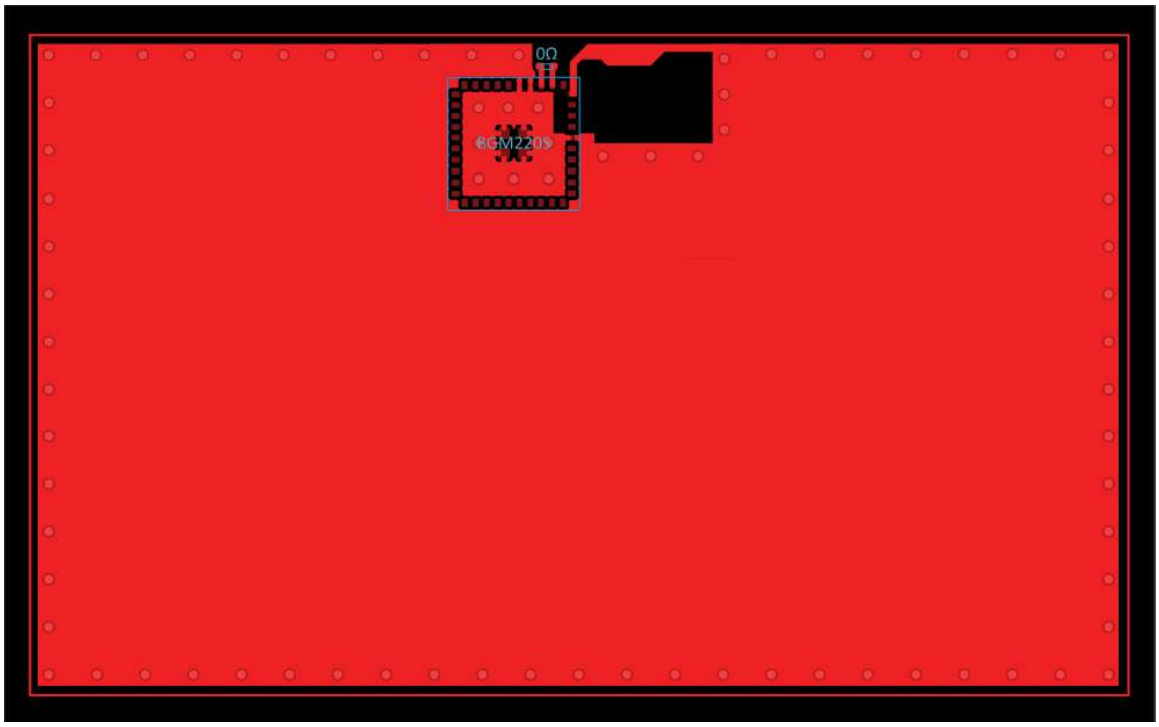


Figure 7.1. Recommended Layout for BGM220S

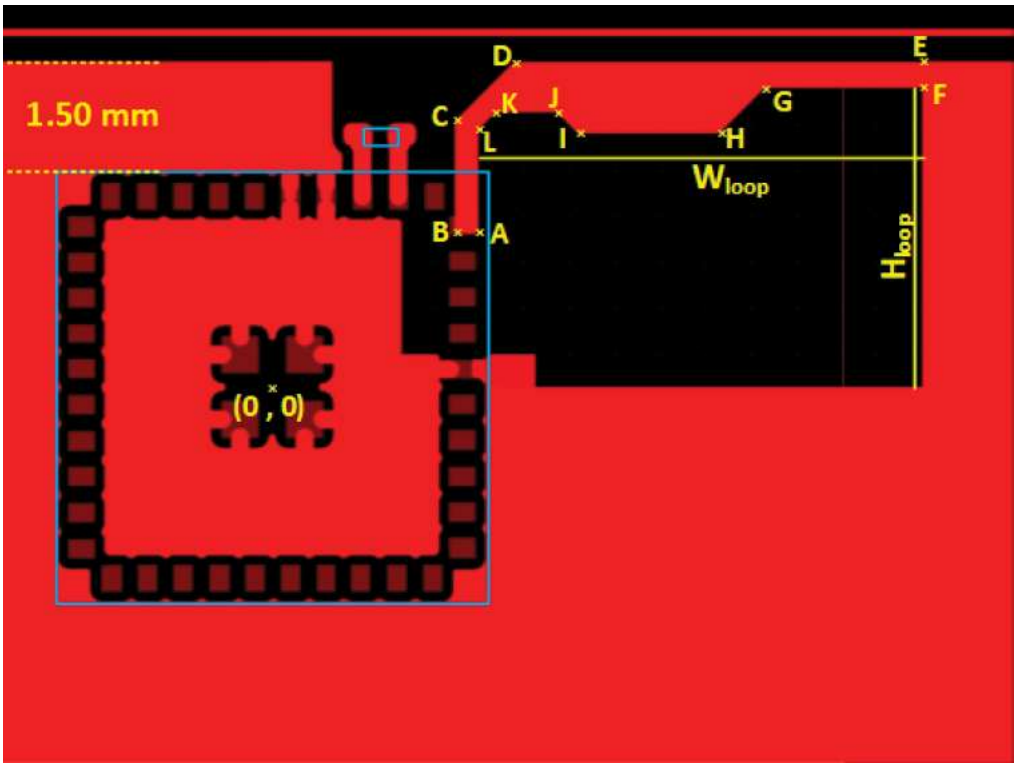


Figure 7.2. Antenna Layout With Coordinates

Table 7.1. Antenna Polygon Coordinates, Referenced to Center of BGM220S

Point	BGM220SC12WGA2	BGM220SC22WGA2 BGM220SC22HNA2
A	(2.87, 2.13)	(2.87, 2.13)
B	(2.54, 2.13)	(2.54, 2.13)
C	(2.54, 3.69)	(2.54, 3.69)
D	(3.36, 4.51)	(3.36, 4.51)
E	(8.85, 4.51)	(7.75, 4.51)
F	(8.85, 4.15)	(7.75, 4.15)
G	(6.84, 4.15)	(6.84, 4.15)
H	(6.21, 3.52)	(6.21, 3.52)
I	(4.26, 3.52)	(4.26, 3.52)
J	(3.97, 3.81)	(3.97, 3.81)
K	(3.10, 3.81)	(3.10, 3.81)
L	(2.87, 3.58)	(2.87, 3.58)
W_{loop}	5.98	4.88
H_{loop}	4.15	4.15

Note:
1. All coordinates and dimensions listed in mm.

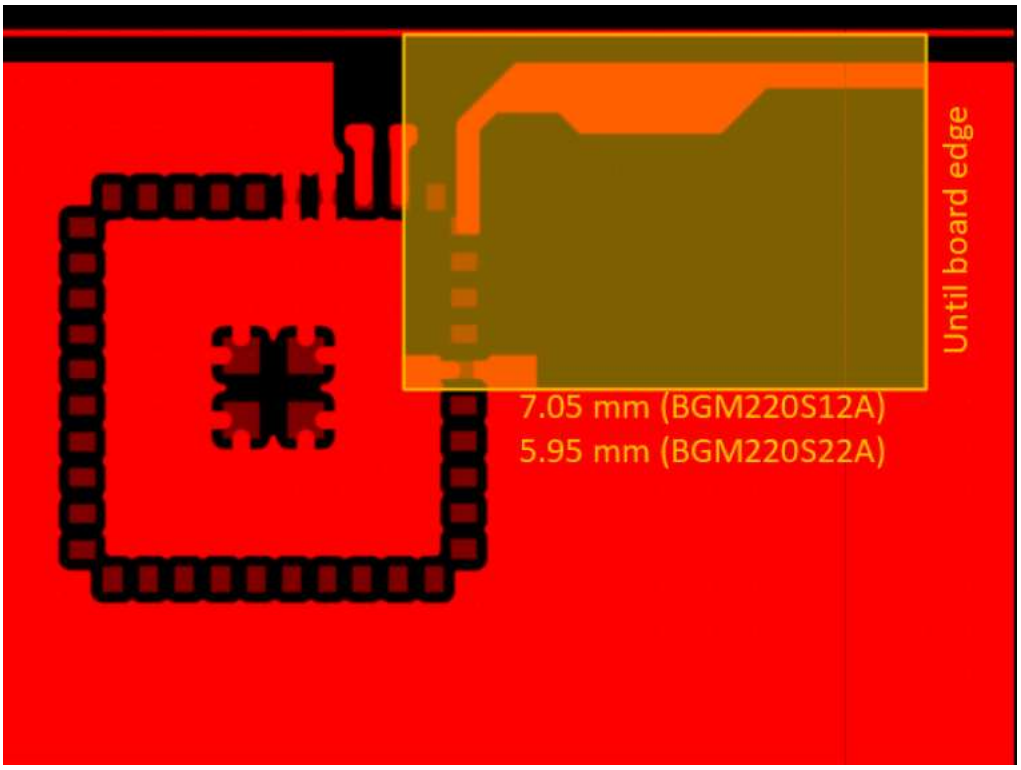


Figure 7.3. Antenna Clearance in Inner and Bottom Layers

7.2 Best Design Practices

The design of a good RF system relies on thoughtful placement and routing of the RF signals. The following guidelines are recommended:

- Place the BGM220S and antenna close to the center of the longest edge of the application board.
- Do not place any circuitry between the board edge and the antenna.
- Make sure to tie all GND planes in the application board together with as many vias as can be fitted.
- Generally ground planes are recommended in all areas of the application board except in the antenna keep-out area shown in Figure 7.3 Antenna Clearance in Inner and Bottom Layers on page 34.
- Open-ended stubs of copper in the outer layer ground planes must be removed if they are more than 5 mm long to avoid radiation of spurious emissions.
- The width of the GND plane to the sides of the BGM220S will impact the efficiency of the on-board chip antenna.
  - To achieve optimal performance, a GND plane width of 50 mm for BGM220S12A or 55 mm for BGM220S22A is recommended as seen on Figure 7.4 Illustration of Recommended Board Width on page 35.
  - See 4.16.1 Antenna Typical Characteristics for reference.

Figure 7.5 Non-Optimal Layout Examples on page 36 illustrates layout scenarios that will lead to severely degraded RF performance for the application board.

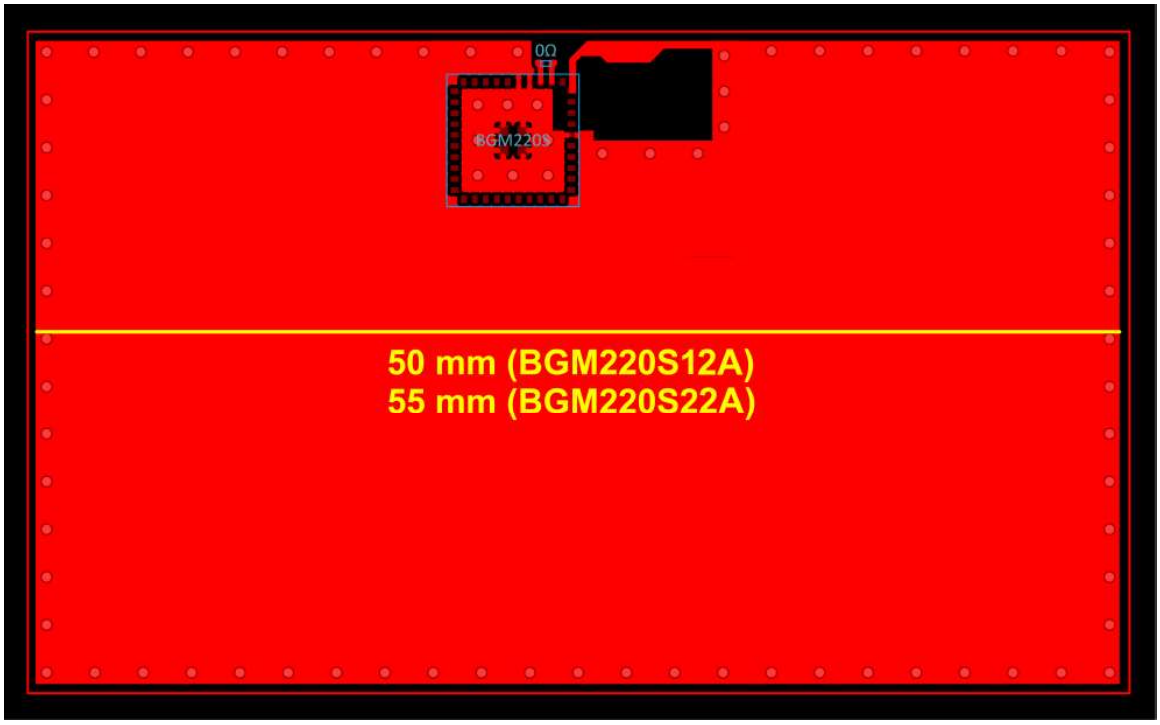


Figure 7.4. Illustration of Recommended Board Width