IDT524 OPERATIONAL DESCRIPTION

The IDT524 RFID controller is designed to read passive fixed code tags with a range of up to 1 meter.
The controller is used with a 17cm round antenna per photo and attached spec sheet .
The RFID method used "Magnetic Induction" where an antenna is driven from the controller at 125khz producing a magnetic field. The RFID tag has in integral antenna winding which, when placed within the excitation magnetic field will magnetically couple so producing power in the tag and a clocking signal from the excitation frequency.
The tag on receipt of the excitation and clock starts to read out its integral number in a binary form and transmits this data back to the controller by modulating the excitation signal with the binary data at a clock rate of 125,000 divided by 64 giving a bit rate of 1935 bits per second.

EXCITATION CIRCUITRY

The IDT524 controller provides a 125khz drive frequency from a 16mhz clock (Kinseki EXO-C3) which has an integral 16mhz crystal driving a binary divider, which divides the 16mhz by 128. The output of this clock generator drives a power amplifier, which drives a square wave pulse into a series 30mh inductor.
The output of this inductor produces a sine wave; the sine wave is shape and cleaned up by a 33nf capacitor to ground. The sine wave passes on to a series 4n7 capacitor, which both isolates the DC element of the drive and provides series tuning for the antenna.
The antenna coil of 300uh (28 turns copper wire) is tuned to resonance by parallel capacitors C1, C2 and trimmer.
The antenna when in resonance produces approximately 160pp which generates the magnetic excitation frequency for the tag.

READ CIRCUITRY

The read signal from the tag is received as a modulated signal carried in the excitation frequency. It is read off the antenna coil by two series diodes which demodulate the signal down to a dc signal, which is further filtered, cleaned up and AC isolated by a parallel and series capacitors and resistors.
The modulated signal is fed into a two stage amplifier which amplifies the input signal from a few millivolts to a ttl/cmos signal level which is fed into an internal comparator on the microprocessor,
The digital data string read by the comparator is decoded by software into binary data for further processing and transmission to an external control system.

PROCESSOR CIRCUITRY

The microprocessor is an 8 bit Atmel device, with integral flash program memory clocked by an external crystal at 11.059mhz, programmed to perform three functions: -

1. **Read demodulated signal from the amps and decode the Manchester code.**
2. **Convert the decoded data into a data string**
3. **Transmit the decoded data to the host system.**

IDT524 CHARACTERISTICS

These characteristics assume the antenna supplied by SWISSLOG in their configuration is as specified in Swisslog drawing 86345001 also the tuning capacitance on the antenna switch PCB is 0-500pf.

Diameter ID	**-**	**6.54"**
Turns	**-**	**approx. 28**
Inductance	**-**	**300mH**
Conductor	**-**	**18 awg round copper**

Then the following parameters are valid: -

1. Excitation Frequency in antenna	**-**	**125khz single frequency**	
2. Excitation Modulation	**-**	**None**	
3. Excitation duty cycle	**-**	**Continuous**	
4. Fixed station	**-**	**Duplex transceiver**	
5. Oscillator Frequency	**-**	**16mhz**	
6. Frequency stability (crystal)	**-**	**100ppm from -10 to 75C degree**	
7. Processor clock (crystal)	**-**	**11.059mhz**	
8. Antenna Inductance	**-**	**300mh**	*****
9. Antenna current	**-**	**125ma**	*****
10. Antenna power	**-`**	**20watts**	*****
11. Antenna Bandwidth	**-**	**3600 c/s**	
12. Tag power type	**-**	**Passive**	
13. Read Modulation type	**-**	**ASK**	
14. Read data rate	**-**	**1935 bits/sec**	
15. Tag data encoding	**-**	**Manchester**	
16. Reader	**-**	**Software read of demodulated signal**	
17. Controller power requires	**-**	**12vdc maximum 1amp. (Translogic)**	
18. Power supply swing	**-**	**10 to 14 vdc**	
19. Operating temperature	**-**	**-10 to 55 degrees C**	

*** Estimated values based on Translogic component values.**