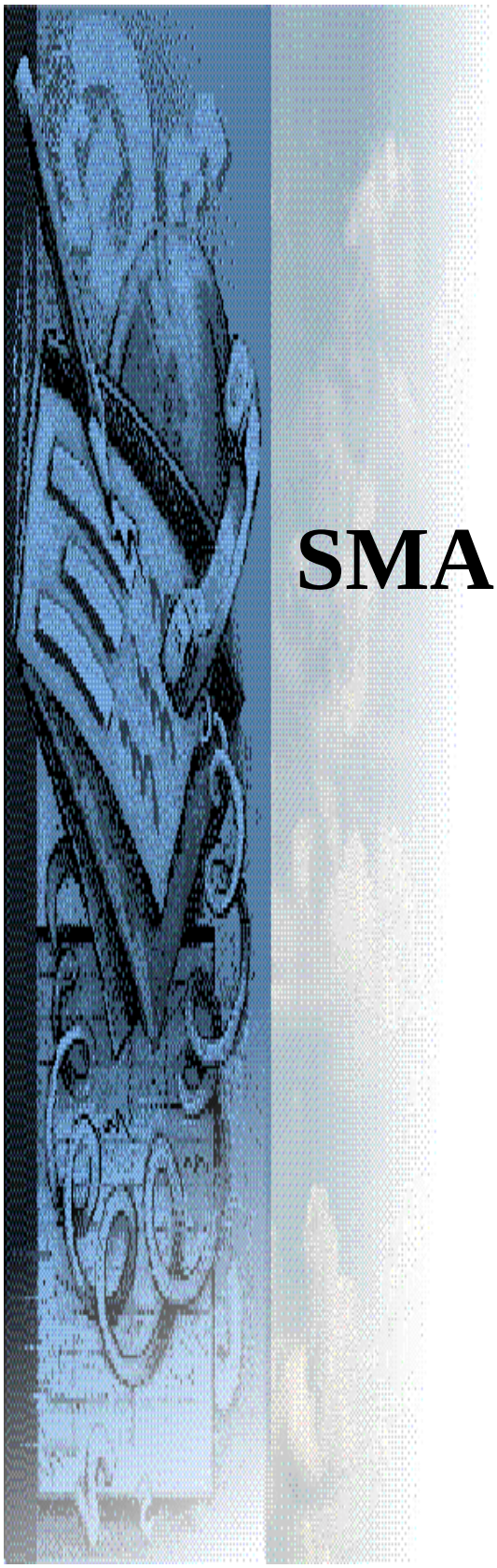
COMUNIQ



SMAS E1/T1 BOARD

Block Diagram

Comuniq ASA

Version 2.0 – March 2000

NOTICE

The information in this publication is subject to change without notice. This document contains proprietary information disclosed under a non-disclosure agreement. Disclosure to any third party without written permission from Comuniq ASA is in violation of the non-disclosure agreement.

COMUNIQ ASA SHALL NOT BE HELD LIABLE FOR TECHNICAL OR EDITORIAL ERRORS OR OMISSIONS CONTAINED HEREIN, NOR FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES RESULTING FROM THE FURNISHING, PERFORMANCE, OR USE OF THIS MATERIAL.

Corporate HQ
Comuniq ASA
Solakrossen 11
N-4050 Sola
Norway

Phone: +47 51 71 55 55
Fax: +47 51 71 55 56

WEB: http://www.comuniq.com

Customer Support
Comuniq Inc.
2046 Samco Rd.
Rapid City, SD 57701
USA

Phone: 1-605-388-3251
Fax: 1-605-348-4030

E-Mail: support@comuniq.com

This document will give the reader an understanding of the functionality of the SMAS. The first section describes the system, followed by a functional description of the SMAS board.

1.1 The SMAS System

SMAS is a firmware platform that enables system integrators to implement services such as Automatic Call Distribution (ACD), Interactive Voice Response (IVR), Private Branch Exchange (PBX), and IP-telephony for E1/T1 connections. The SMAS system is a scalable telephony system, which may consist of a maximum of 36 SMAS cards per Compact PCI PC. The main host of the system is a Windows NT server. The block diagram in Figure 1 illustrates the scalability where a large number SMAS cards can be attached on the PCI bus under supervision of Windows NT or a user defined host.

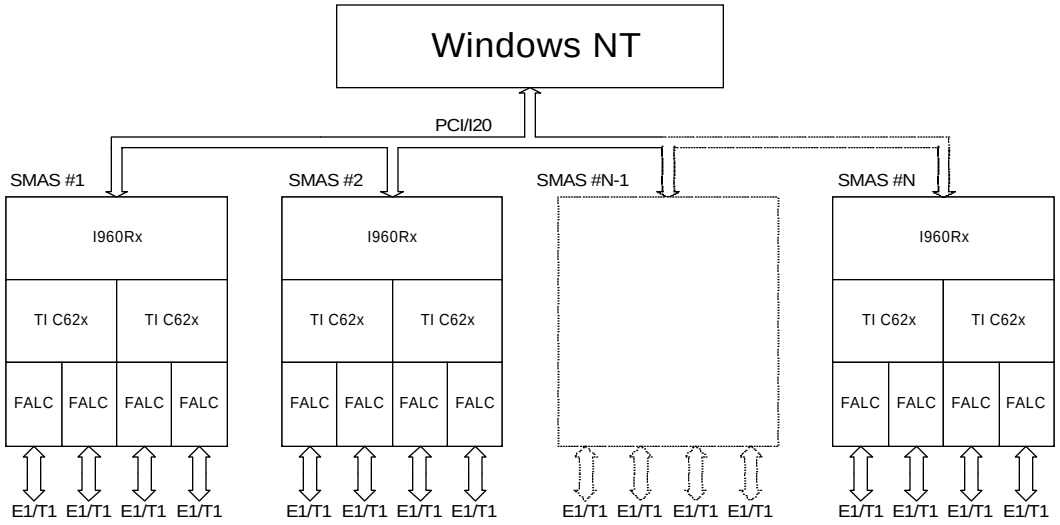


Figure 1 – A block diagram of the SMAS telephony system.

The system utilizes the PCI bus to transfer telecommunication data in a maximum configuration of 4320 voice channels for E1 and 3456 voice channels for T1.

1.2 Hardware

The hardware is divided into four layers. Of these four layers, all but the host computer are physically located on the SMAS card.

- Host computer, Windows NT (NT)
- Embedded I_2O Processor, Intel 80960RD (i960)
- Digital Signal Processor, Texas Instrument's TMS320C6201 (C6)
- Line Interface Adapter, Siemens Falc'54 (FALC'54)

The architecture enables a total of 120 full duplex voice channels per card for an E1 interface and a total of 92 (or 96) full duplex voice channels per card for a T1 interface. The E1 has, in addition, four D-channels and four synchronization channels, and T1 may have four D-channels when it is configured for use with 92 voice channels. For E1 the line interface runs at 2.048 Mbps, and for the T1 line interface runs at 1.544 Mbps. The data format on the E1/T1 side is G.711, which is standard A-Law (Europe) or μ-Law (USA and Japan). Figure 2 show the SMAS card architecture, which consists of three main components: Falc'54, C6 and i960.

Figure 2 also shows the memory configuration and the data flow throughout the system. The PCI interface is 32 bits and runs at 33 MHz, and it interfaces with the i960, which also runs at 33 MHz. The C6 has a 50 MHz external clock allowing 200 MHz internal operation. The Flash contains the IxWorks operating system for the i960 and the firmware code for the Altera, not illustrated in Figure 2. Downloading the program code directly from an NT application configures the system. The i960 has 16 Mbytes external DRAM memory to store data and programs. The i960 runs at 33 MHz on the peripheral interface but has a core clock frequency of 66 MHz. The C6's each have 16 Mbytes of DRAM for storage of algorithms and data. When fully configured, the SMAS board will handle four full duplex E1/T1 trunks, with each Falc'54 handling one trunk.

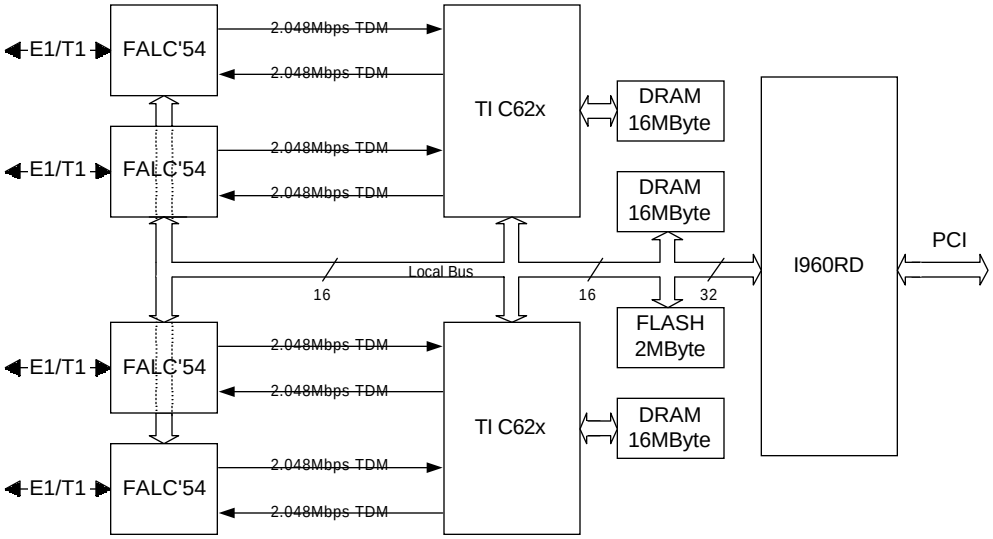


Figure 2 – A block diagram of the SMAS hardware.

The FALC54 requires a 16.384 MHz crystal between XTAL1 and XTAL2 for E1/T1 operation; in addition a 12.352 MHz crystal is required between XTAL3 and XTAL4 for proper T1 operation. XTAL1 and XTAL2 are the in-/outputs for the DCO1, these internal PLL circuitry generates the jitter free system clocks (16 MHz, 8 MHz, 4 / 2 MHz and 8 KHz). XTAL3/4 are the in-/outputs for the DCO2, the main task of the DCO2 in T1 is to generate the dejittered transmit clocks. The crystals should be connected as illustrated in figure 3.

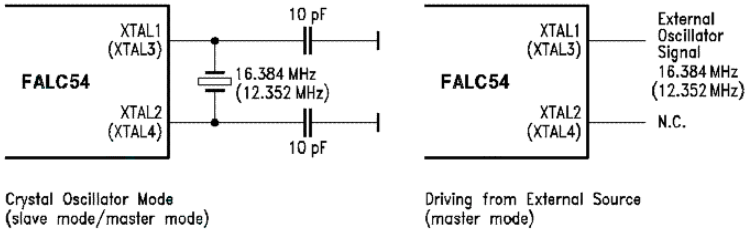


Figure 3 -- Jitter free transmit clock requires crystal interconnection.

The jitter attenuator requires unique performance specifications for the crystals. The following typical crystal parameters will meet these specifications:

- Motional capacitance C1 = 25fF min.
- Shunt capacitance C0 = 7pF max.
- Load capacitance CL = 15pF typ.

The motional capacitance C1 is responsible for the overall pulling range of the crystal. The load capacitance CL defines the accuracy of the free running frequency. The FALC requires 10pF load capacitance to GND at XTAL1 (XTAL3) and XTAL2 (XTAL4). With additional internal capacitance (about 20pF to GND in free running mode) the crystal sees a CL of 15pF. With the help of internal switched capacitance the crystals frequency can be changed in steps of 25 ppm to a tuning range of max. +/- 200 ppm.