2.4GHz 11Mbps MACless DSSS Radio HWB1151 User's Guide

Application Note | **February 1999** | **AN9835**

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The Radio Card product provides all the hardware required to implement wireless communication using Direct Sequence Spread Spectrum (DSSS) technology. Only an external Media Access Controller is required.

DSSS technology provides interference rejection in the presence of narrow band noise. Since the output power is spread across such a large bandwidth, the DSSS signal is low level and wide bandwidth and therefore not intrusive to other equipment.

Evaluation kits include two MACless cards in a PCMCIA Type II form factor and this application note. The HWB1151-KIT MACless radio kit does not include any software.

THE PCMCIA BUS INTERFACE HAS NOT BEEN IMPLEMENTED IN THIS CARD, THEREFORE A PROPER INTERFACE IS REQUIRED, (SEE SIGNAL DESCRIPTION).

This product has been designed to allow evaluation of the Harris PRISM™ Direct Sequence chip set.

The HWB1151-KIT is not FCC approved as an intentional radiator and is intended for use with cabled connections only (30dB attenuation recommended antenna port to antenna port). An FCC experimental license is required while transmitting over the air with unapproved equipment.

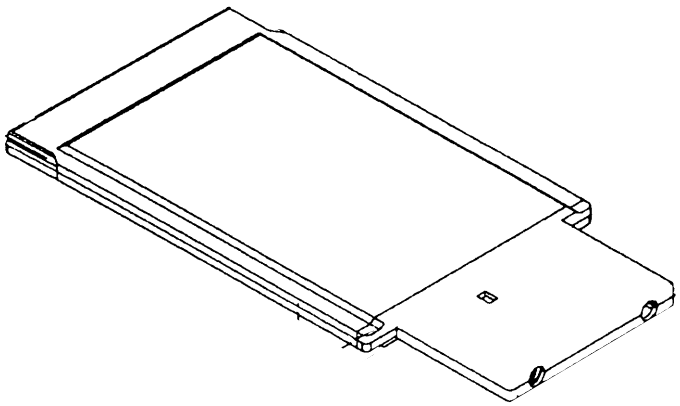
Features

- Provides Antenna-to-Bits™ Data Stream
- Single Heterodyne Conversion
- Autonomous Half Duplex Direct Sequence Modem
- Selectable CCK, MBOK DBPSK and DQPSK Signalling
- Antenna Diversity Selection
- Differential Data Encoding/Decoding
- Programmable 11-Bit PN Code
- Data Rates Up to 11Mbps
- Power Management Control
- Low Profile PCMCIA PC Card Type II

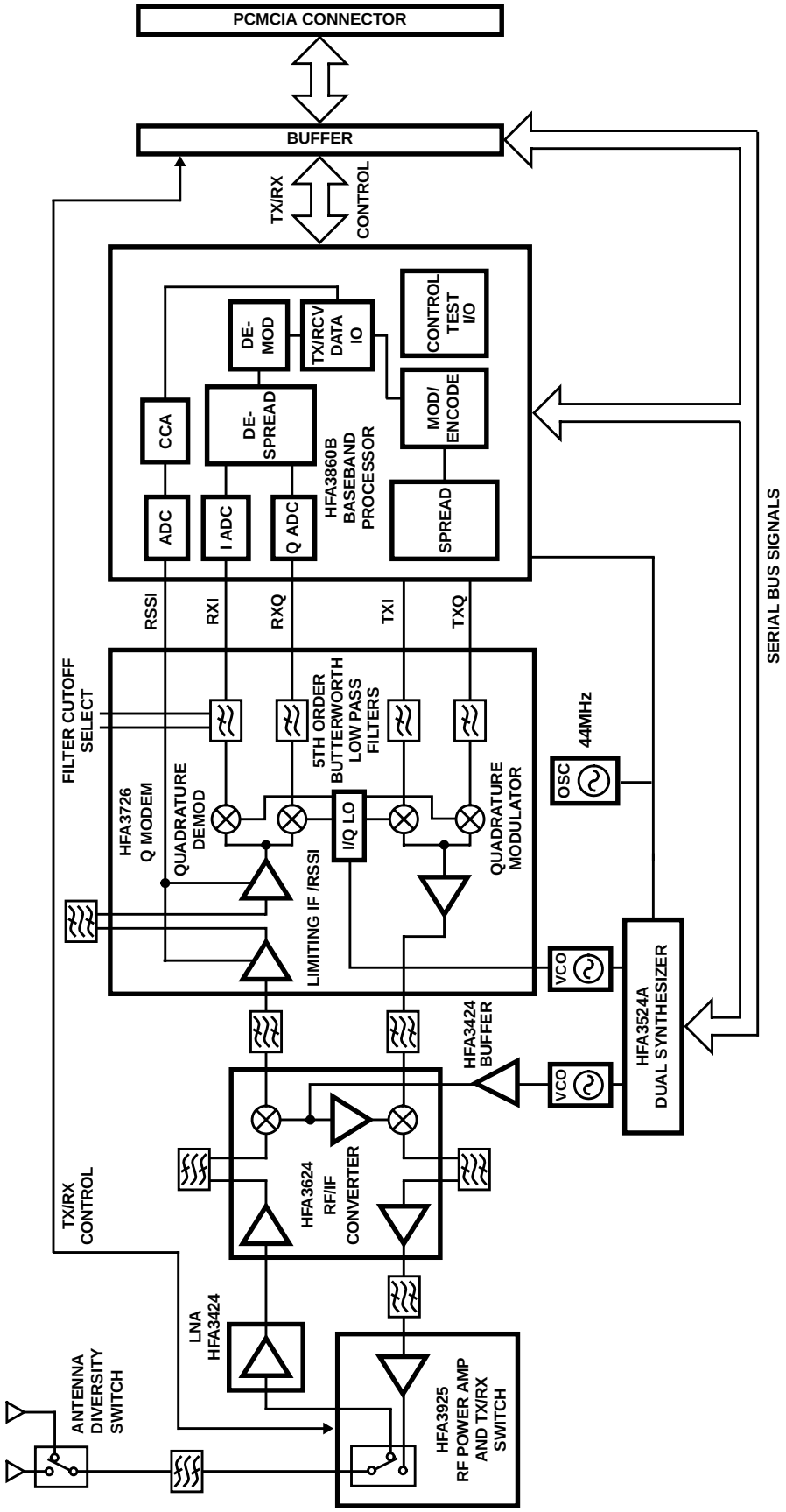
Ordering Information

PART NUMBER	DESCRIPTION	CARDS PER KIT
HWB1151-EVAL	Point-to-Point Evaluation Kit	2
HWB1151-EVALPAK	System Evaluation Kit	10

Packaging



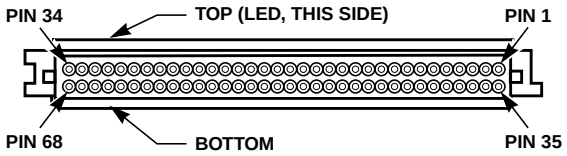
HWB1141 Block Diagram



Connector Pin Assignments:

NOTE: Digital signals preceded by “C_” (e.g. C_BB_CS) are CMOS (5V logic) signals. Others are 3.5V logic signals. Data lines are routed through bi-directional level converters to change from 3.5V to 5V logic levels and vice versa.

SIGNAL NAME	PCMCIA PIN NUMBER
GND	1, 34, 35 and 68
Unused	2-10, 13, 15, 16, 18, 22, 23, 31, 32, 37, 47, 49, 50, 52-58, 60, 61, 64-66
C_OSC_START	11
C_RX_PE_BB	12
C_BB_CS	14
V_{CC}	17 and 51
C_R_WB	19
C__SPCLK	20
C_SYNTH_LE	21
C_RADIO_PE	24
C_PA_PE	25
C_RESET_BB	26
C_RX_PE	27
C_TXD	28
C_TX_PE	29
C_SPD	30
C_TXC	33
C_RXCIN	36
C_Test_CK	38
C_Test7	39
C_Test6	40
C_Test5	41
C_Test4	42
C_Test3	43
C_Test2	44
C_Test1	45
C_Test0	46
C_SYNTH_LD	48
C_MD_RDY	59
C_CCA	62
C_RXDATA	63
C_TX_RDY	67



VIEW, LOOKING INTO 68 PIN FEMALE CONNECTOR

Operating Conditions

Voltage . . . . . 4.5V to 5.5V Temperature Range . . . . . 0^oC to 55^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT CONSUMPTION					
Average Current					
Without Power Saving Mode [3]	2% Transmit, 98% Receive	-	225	-	mA
With Power Saving Mode [3]	2% Transmit, 8% Receive, 90% Standby	-	53	-	mA
Continuous Receive Mode [3]		-	221	-	mA
Continuous Transmit Mode [3]		-	422	-	mA
Standby Mode [3]		-	30	-	mA
INPUT/OUTPUT CHARACTERISTICS					
Input LOW Level		-	-	0.8	V
Input HIGH Level		2.0	-	-	V
Output LOW Level					
V_{OL} (I_{OL} = 0.1mA)		-	-	0.2	V
V_{OL} (I_{OL} = 24mA)		-	-	0.5	V
Output HIGH Level					
V_{OH} (I_{OH} = -3mA)		2.4	3.0	-	V
V_{OH} (I_{OH} = -0.1mA)		V_{CC}-0.2V	-	-	V
Input LOW Current	(V_{CC} = Max)	-	-	±5	µA
Input HIGH Current	(V_{CC} = Max)	-	-	±5	µA
Output Capacitance		-	-	8.0	pF
Input Capacitance		-	-	8.0	pF
RF SYSTEM CHARACTERISTICS					
Output Power	25^oC	14	18	-	dBm
Transmit Spectral Mask	At First Sidelobe	-	-32	-	dBc
Receive Sensitivity					
1Mbps DBPSK 8% PER		-	-89	-	dBm
2Mbps DQPSK 8% PER		-	-86	-	dBm
5.5Mbps CCK 8% PER		-	-86	-	dBm
11Mbps CCK 8% PER		-	-83	-	dBm
Input Third Order Intercept		-	-22	-	dBm
Image Rejection	8% PER	-	65	-	dB
IF Rejection	8% PER	-	80	-	dB
Adjacent Channel Rejection	8% PER at 25MHz Offset	-	63	-	dB

Functional Overview

The Radio Card is based on the Harris PRISM Direct Sequence Chip Set.

There are ten basic units in this card:

1. Baseband Processor
2. Modulator/Demodulator
3. Dual Synthesizer
4. Up/Down Converter
5. Power Amplifier
6. Low Noise Amplifier (LNA)
7. RF VCO
8. IF VCO
9. Antenna
10. Buffer Interface

During transmission, the data to be transmitted should be placed on the TX data line going into the baseband processor. This data will be modulated according to the format selected (CCK, MBOK, DBPSK or DQPSK) and then spread using a programmable PN code. Two signals will be generated (I & Q).

The I & Q signals are sent to the Modulator/Demodulator where they will be first filtered and then modulated with the IF frequency (280MHz). The IF oscillator generates 560MHz which is divided by two inside the Modulator/Demodulator, so the final IF signal is 280MHz. Next, the two signals are combined into a single signal and sent over to the Up/Down converter.

The Up/Down converter will shift this signal to the RF channel programmed in the synthesizer, in the 2.4GHz ISM band.

In the final stage this signal is amplified to produce a typical power output of 18dBm, measured in the middle of the ISM Band at the antenna.

In the receive mode, the radio signal is received by one of the two external antennas. The antenna selected is optionally determined by an Antenna Diversity algorithm in the Baseband Processor which compares the quality of the received signal in each antenna during the Preamble and selects the better signal. This substantially improves the multipath performance of the assembly. Alternately, the antenna selection may be directly controlled by the software.

The signal is amplified by the LNA, and then sent to the Up/Down converter. The Up/Down converter down-converts this signal from the 2.4GHz range to the IF frequency, 280MHz.

The Modulator/Demodulator converts the signal to baseband and splits the signal into the In-Phase (I) and Quadrature (Q) components, before it is sent to the Baseband Processor.

Finally, the Baseband Processor despreads and demodulates the data from DBPSK or DQPSK form, and places it on the RX data line.

The bi-directional Buffer Translators are used to interface between computer 5V and card 3.5V logic.

The RF and IF Local Oscillator signals are generated using the synthesizer and the voltage controlled oscillators. The dual synthesizer should be programmed with the desired RF channel frequency less the IF frequency.

Example:

	RF		IF		LO
CH1	2412MHz	-	280MHz	=	2132MHz

The baseband processor and the synthesizer are driven from a common 44MHz oscillator to control the timing of these chips.

Refer to Application Note AN9624 [1] for a more detailed radio description.

Edge Connector Pin Descriptions

The block diagram in Figure 1 shows control signal connections from the edge connector to the radio integrated circuits.

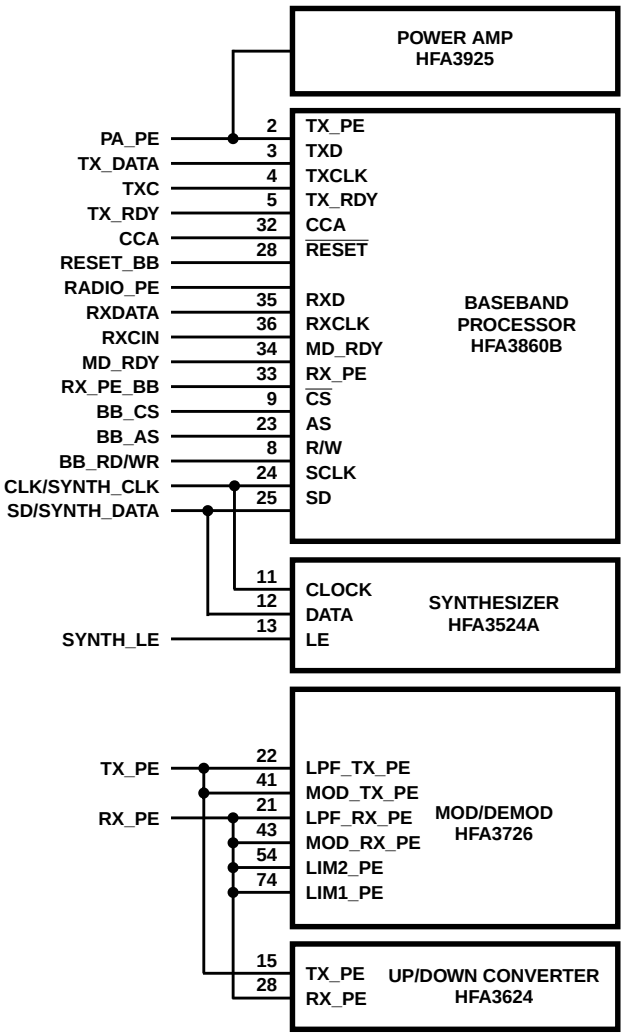


FIGURE 1. CONTROL SIGNAL CONNECTIONS

NOTE: Digital signals preceded by “C_” (e.g. C_BB_CS) are CMOS (5V logic) signals. Others are 3.5V logic signals. Data lines are routed through bi-directional level converters to change from 3.5V to 5V logic levels and vice versa.

In the Discussion below, (I) refers to an Input signal whereas (O) refers to an Output.

C_PA_PE (I) Pin 25

When active high the baseband processor and power amplifier are in transmit mode, otherwise they are in standby mode (see Figure 6). This signal is usually obtained from a MAC or a network processor.

The internal transmit state machine will be activated by the rising edge of PA_PE, the falling edge will deactivate it. The PA_PE envelopes the transmit data.

This signal switches the power amplifier (PA) from TX to RX as follows:

PA_PE = high--> TX mode
PA_PE = low --> RX mode

C_TXD (I) PIN 28

This pin is used to transfer serial data or preamble/header data from a MAC or network processor to the baseband processor. The LSB is received first and the data is clocked in the baseband processor at the falling edge of TXC. A data bit high = “one”.

C_TXC (O) Pin 33

Output clock signal to the MAC or network processor used to input serial data to the baseband processor. The data is clocked into the baseband processor using the falling edge of TXC.

C_TX_RDY (O) Pin 67

Output to the MAC or network processor which indicates that the preamble or header has been generated. This signals that the baseband processor is ready to receive serial data for transmitting over the TXDATA serial line from the MAC or network processor.

TX_RDY signal returns to the inactive state when the PA_PE goes low indicating the end of transmission.

C_CCA (O) Pin 62

Clear Channel Assessment signal indicates the availability of the channel for transmission. The CCA algorithm is user programmable. The detailed operation of this pin may be found in the PRISM Baseband Processor data sheet [5]. The active level of this signal is programmable.

C_RXDATA (O) Pin 63

Output to a MAC or a network processor which transfers demodulated header information and data in serial format. The LSB is sent first and is aligned with the MD_RDY signal (see Figure 7).

C_RXCIN (O) Pin 36

This clock signal is used to serially transfer the header and data from the RXDATA pin to the MAC or network processor. The signal is held low when not transferring data.

C_MD_RDY (O) Pin 59

Signal to a MAC or network processor indicating a data packet is ready. The signal indicates the data transfer over the RXD serial line.

C_RX_PE_BB (I) Pin 12

When set high the baseband processor is in receive mode.

C_SPD (I/O) Pin 30 {SD/SYNTH_DATA}

There are two purposes for this pin. In regards to the baseband processor, this serial line is used to transfer address and data to and from the baseband processor. The MSB is always transferred first. In regards to the synthesizer, the address and data are programmed through this line. The MSB is always first (see Figures 3 and 4).

C_SPCLK (I) Pin 20 {CLK/SYNTH_CLK}

This clock signal is used for serial bus transfers to program the baseband processor and the synthesizer. The data is clocked on the rising edge of the signal at a maximum rate of 10MHz. Even though, CLK/SYNTH_CLK are low frequency, rise and fall times of less than 10ns should be observed.

C_BB_CS (I) Pin 14

An active low signal which enables programming of the Baseband Processor.

C_R_WB (I) Pin 19

Used to change the direction of the SD/SYNTH_DATA line while programming the baseband processor. This signal must be set up prior to the rising edge of CLK/SYNTH_CLK. A high on this line allows data to be inputted to the Baseband Processor whereas a low is used to write data from the Baseband Processor.

C_RESET_BB (I) Pin 26

Active low signal. Baseband processor reset. Must be inactive during programming. When active RX and TX functions are disabled (see Figure 5).

C_RADIO_PE (I) Pin 24

This signal, when asserted high, enables the radio card. Power is applied to all chips.

This signal should be kept high during operation of this card.

C_TX_PE (I) Pin 29

This signal, when asserted high, enables the transmit section of the Modulator/Demodulator and RF/IF Up/Down converter circuits.

C_RX_PE (I) Pin 27

This signal, when asserted high, enables the receiver section of the Modulator/Demodulator and RF/IF Up/Down converter circuits.

C_SYNTH_LE (I) Pin 21

SYNTH_LE, CLK/SYNTH_CLK and SD/SYNTH_DATA signals are used to program the synthesizer. SYNTH_LE latches a frame of 22 bits after it has been shifted by the CLK/SYNTH_CLK into the synthesizer registers. Please note that the clock and data lines are shared also by the baseband processor

C_OSC_START (I) Pin 11

This signal is an active low pulse which ensures start-up of the VCO (see Figure 5). Some brands of VCO's will not reliably start oscillating at low control voltages due to the reduced tank circuit Q caused by this condition. This line forces the control pin on the VCO to the +3.5V supply rail to ensure oscillator start-up. The currently recommended Motorola KXN1332A VCO does not require activation of this line.

C_SYNTH_LD (O) Pin 48

Lock detect signal coming back from the synthesizer which signals an out-of-lock condition in either Phase Lock Loop. May be used to inhibit transmit under these conditions. High state when out-of-lock.

C_TEST_CK (I) Pin 38

Clock signal used to read the test data from the Baseband Processor (see the HFA3860B Data Sheet).

C_TEST7 through C_TEST0 (O) Pins 39-46

Reads out the test data from the Baseband Processor (see the HFA3860B Data Sheet).

Radio Card Programming

Programming Sequence

1. At power up, set all input signals to default values, see Table 1.
2. Set signal values to baseband processor programming mode (see Figures 2, 3).
3. Program baseband processor as specified in technical data sheet. Example is provided below.
4. Set signal values to synthesizer programming mode (see Figure 4).
5. Program synthesizer as specified in technical data sheet. Example is provided below.
6. Start TX or RX sequence.

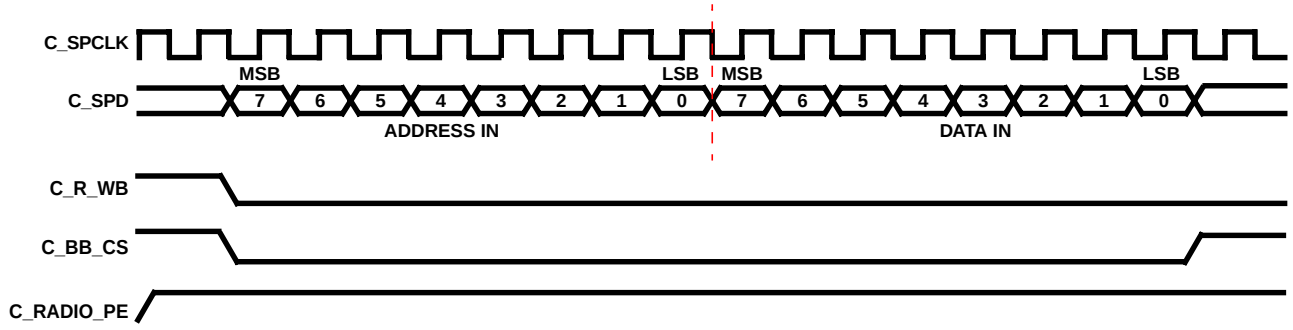
Important - If power is removed from the card, all set ups will be lost.

All (I) signals are input signals into this card. These signals are assumed to be controlled by a MAC (Media Access Controller) and are to be programmed as specified.

Examples are provided as reference only.

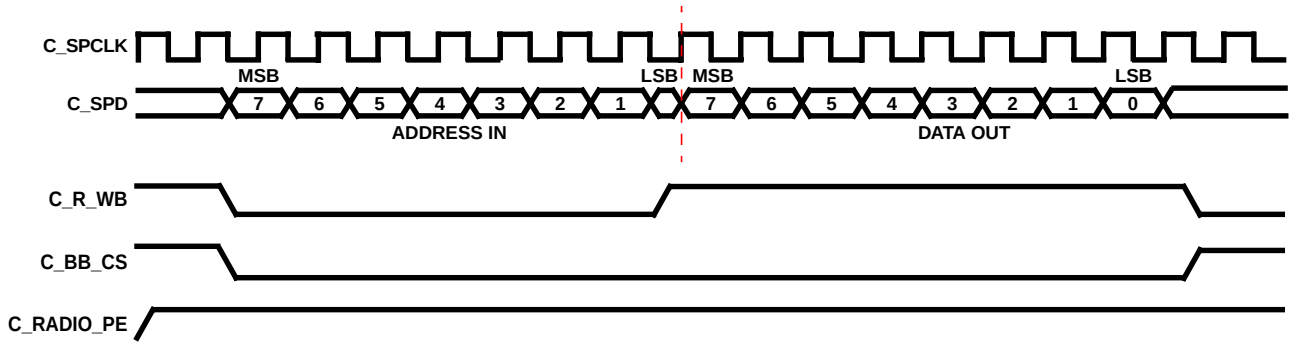
TABLE 1. CONTROL SIGNAL DEFAULT VALUES

CONTROL SIGNAL	VALUE
C_PA_PE (I)	Low
C_TXD (I)	Do Not Care
C_RX_PE_BB (I)	Low
C_SPD (I/O)	Do Not Care
C_SP_CLK (I)	Low
C_R_WB (I)	Do Not Care
C_BB_CS(I)	High
C_RESET_BB (I)	High
C_RADIO_PE (I)	High
C_TX_PE (I)	Low
C_RX_PE (I)	Low
C_SYNTH_LE (I)	Low
C_OSC_START (I)	High
C_TEST_CLK	Do Not Care



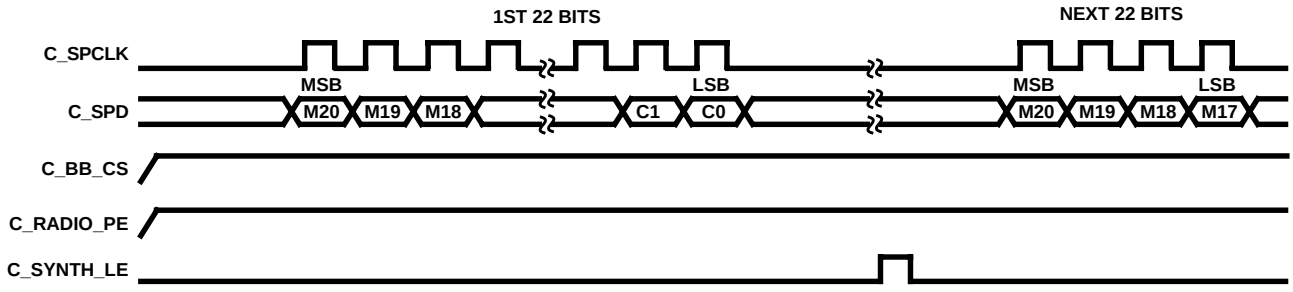
NOTE: Check baseband processor data sheet for timing details.

FIGURE 2. BASEBAND PROCESSOR CONTROL PORT WRITE TIMING



NOTE: Check baseband processor data sheet for timing details.

FIGURE 3. BASEBAND PROCESSOR CONTROL PORT READ TIMING



NOTE: Check synthesizer data sheet for timing details. When the synthesizer is powering up or coming out from Power Down Mode, some registers should be written into it first; refer to the HFA3524, HFA3524A data sheet. After that, the synthesizer is in Power Up mode and it can be programmed according to the data sheet.

FIGURE 4. SYNTHESIZER PROGRAMMING

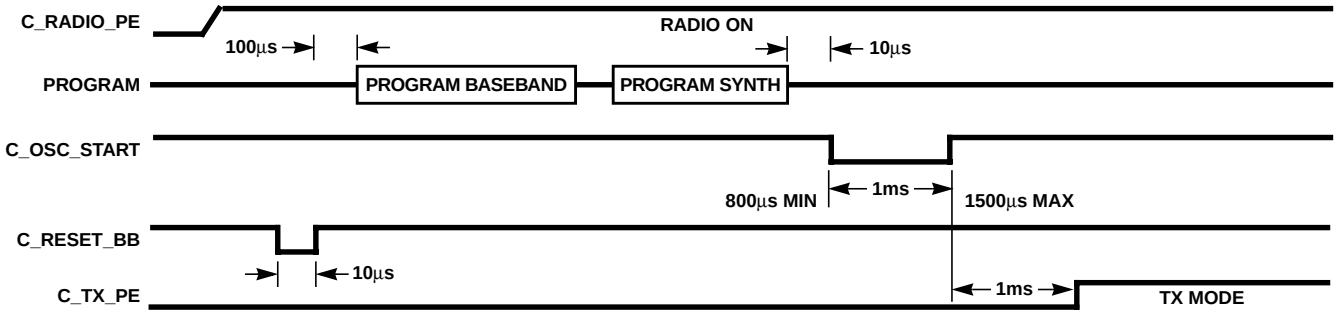


FIGURE 5. PROGRAM SEQUENCE

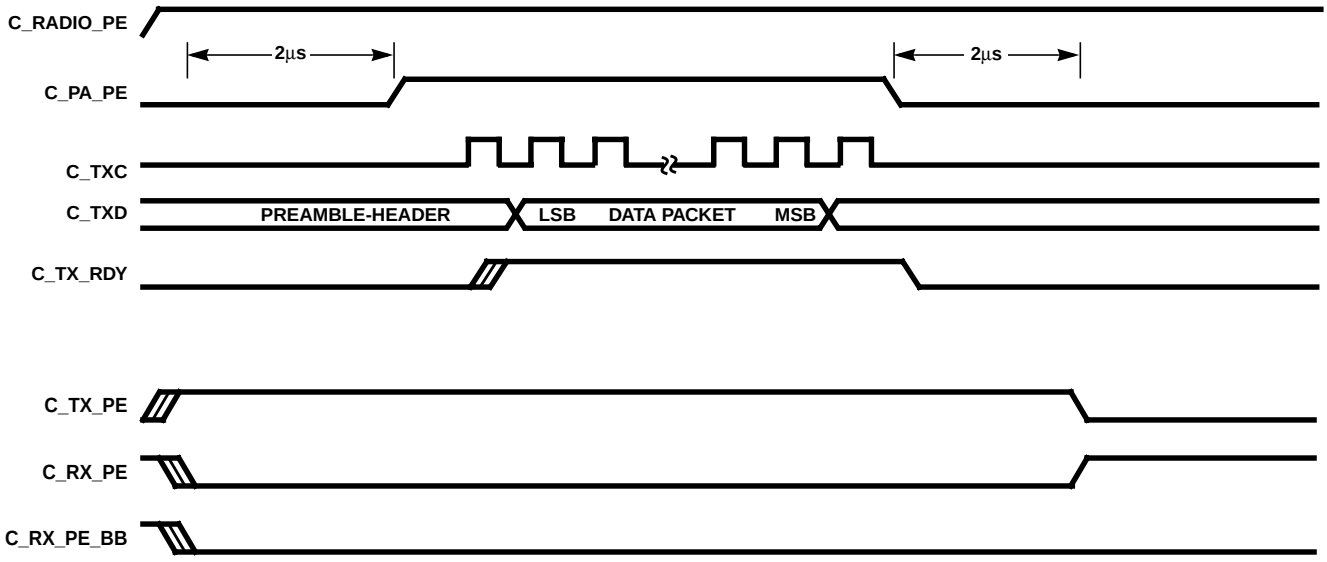


FIGURE 6. TX MODE TIMING

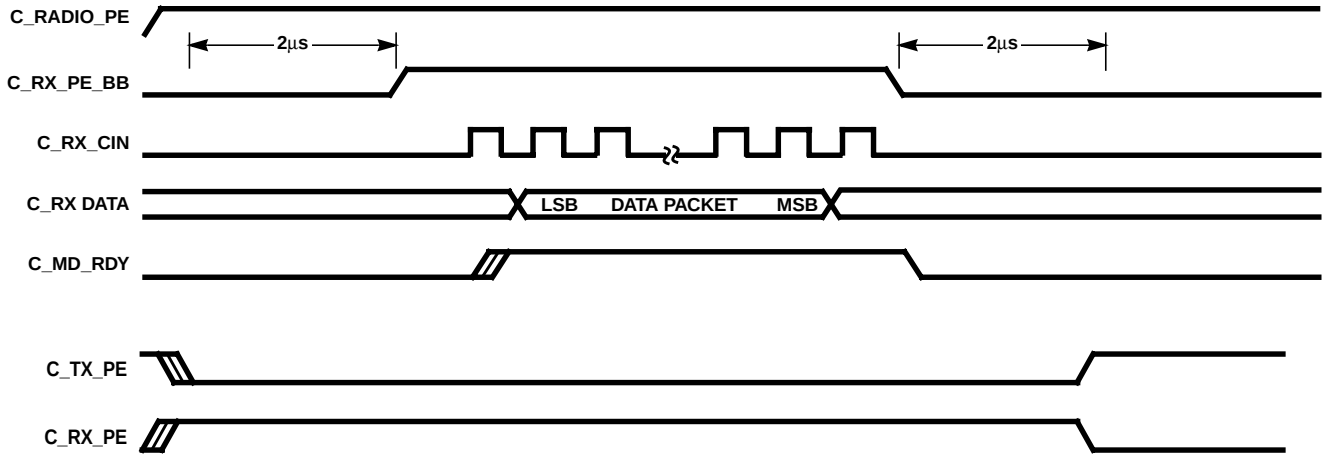


FIGURE 7. RX MODE TIMING

Programming Examples

HFA3860B Baseband Processor programming, 11Mbsp CCK mode, no Antenna Diversity. **NOTE:** In CCK mode, it is necessary to download data twice, designated CCK Initial and CCK Final.

TABLE 2. CCK INITIAL DOWNLOAD

REGISTER NAME	HEX VALUE	COMMENT
CR1	00	I/O Polarity
CR2	14	TX & RX Control
CR3	02	A/D_CAL_POS Register
CR4	FF	A/D_CAL_NEG Register
CR5	82	CCA antenna Control
CR6	80	Preamble Length
CR7	48	Scramble_Tap (RX & TX)
CR8	01	RX_SQ1_ACQ (High) Threshold
CR9	88	RX_SQ1_ACQ (Low) Threshold
CR10	00	RX_SQ2_ACQ (High) Threshold
CR11	98	RX_SQ2_ACQ (Low) Threshold
CR12	01	SQ1 CCA Threshold (High)
CR13	98	SQ1 CCA Threshold (Low)
CR14	01	ED or RSSI Threshold
CR15	98	SFD Timer
CR16	48	I Cover Code
CR17	48	Q Cover Code
CR18	37	Signal Field
CR19	6E	Signal Field
CR20	00	TX Signal Field
CR21	00	TX Service Field
CR22	FF	TX Length Field (High)
CR23	FF	TX Length Field (Low)
CR28	00	Test Bus Address
CR30	00	Test Register 1
CR31	19	RX Control MBOK/CCK

TABLE 3. CCK FINAL DOWNLOAD

REGISTER NAME	HEX VALUE	COMMENT
CR05	02	Control
CR16	0A	Signal
CR17	14	Signal

Example for synthesizer (HFA3524A or HFA3524) programming CH1 (RF and IF), 44MHz Clock, 1MHz steps.

IF R Counter (Read in MSB First, IFR =1802C0h)

LSB MSB

0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0
C1C2	R																16 17 18 19 20				

R16 = 1 --> IF positive
R17 = 0 --> Low current
R18 = 0 --> D_{OUT} IF normal operation
R19 = 0, R20 = 0 --> F_O/LD disable

IF N Counter

LSB MSB

1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	0
C1C2	A								B											P, 20	

F_{VCO} = [(P x B) + A] x 44MHz/R <-- see IF R counter set up for “R” value.
IF_{VCO} = [(16 x 023h) + 0] x 44MHz/(2Ch) = 560MHz
N19 = P = 1 --> /16
N20 = 0 = IF powered

RF R Counter (Read in MSB First, RFR = 1802C8h)

LSB MSB

0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0
C1C2	R																16 17 18 19 20				

R16 = 1 --> RF positive
R17 = 1 --> High current
R18 = 0 --> D_{OUT} RF normal operation
R19 = 0, R20 = 0 --> F_O/LD disable

RF N Counter

LSB MSB

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
C1C2	A								B											P, 20	

F_{VCO} = [(P x B) + A] x 44MHz/R
RF_{VCO} = [(32 x 42h) + 14h] x 44MHz/(2Ch) = 2.132GHz
N19 = P = 0 = /32
N20 = 0 = RF powered

Please check synthesizer technical data sheet (HFA3524A or HFA3524) [7] for more information.

TABLE 4. IEEE 802.11 OPERATING CHANNEL FREQUENCIES

CHANNEL ID	FCC/IC CHANNEL FREQUENCIES (U.S.A./CANADA)	MKK CHANNE FREQUENCIE (JAPAN)	ETSI CHANNEL FREQUENCIE (EUROPE)	FRENCH CHANNEL FREQUENCIES	SPANISH CHANNEL FREQUENCIES
1	2412MHz	N/A	2412 MHz	N/A	
2	2417MHz	N/A	2417 MHz	N/A	
3	2422MHz	N/A	2422MHz	N/A	
4	2427MHz	N/A	2427MHz	N/A	

TABLE 4. IEEE 802.11 OPERATING CHANNEL FREQUENCIES (Continued)

CHANNEL ID	FCC/IC CHANNEL FREQUENCIES (U.S.A./CANADA)	MKK CHANNE FREQUENCIE (JAPAN)	ETSI CHANNEL FREQUENCIE (EUROPE)	FRENCH CHANNEL FREQUENCIES	SPANISH CHANNEL FREQUENCIES
5	2432MHz	N/A	2432MHz	N/A	
6	2437MHz	N/A	2437MHz	N/A	
7	2442MHz	N/A	2442MHz	N/A	
8	2447MHz	N/A	2447MHz	N/A	
9	2452MHz	N/A	2452MHz	N/A	
10	2457MHz	N/A	2457MHz	2457MHz	2457MHz
11	2462MHZ	N/A	2462MHz	2462MHz	2462MHz
12	N/A	N/A	2467MHz	2467MHz	N/A
13	N/A	N/A	2472MHz	2472MHz	N/A
14	N/A	2484MHz	N/A	N/A	N/A

Antenna

The antenna connectors are the Huber Suhner 82MMCX - S50 - 2/111KE. The adapter recommended for SMA connector is the Huber Suhner 33MMCX - SMA - 50 -1.

Antenna select should be programmed by programming the HFA3860B (bits 0 through 3 in Configuration Register 5).See the Radio Card Outline for antenna jack locations.

General Notes

1. This card has been tested and adjusted for operation in Direct Sequence Spread Spectrum. Operation frequency is in the 2.4GHz band.
2. Power spectrum output was checked for CH1, CH6 and CH11.
3. The power output was calibrated to +15dBm and link test was conducted. The operation range is estimated to be 150 ft. for indoor use.
4. ***Always have a 50Ω load installed in the antenna connectors. If the connector is left open it could cause permanent damage to the power amplifier.***
5. The baseband processor MCLK and the synthesizer are driven by a 44MHz oscillator. Please use this frequency when programming either device.
6. If this card is inserted in a PCMCIA slot by accident it will not enable card detect, therefore no damage to card will occur.

Abbreviations

(I) = Input to the Radio Card

(O) = Output from the Radio Card

MAC = Media Access Controller

TX = Transmit

RX = Receive

High = 5V

Low = 0V

LSB = Least Significant Bit

MSB = Most Significant Bit

References

For Harris documents available on the internet, see web site http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

[1] *AN9624 Application Note*, Harris Semiconductor, “PRISM1KIT-EVAL DSSS PC Card Wireless LAN Description”, Carl Andren, Mike Paljug, and Doug Schultz (Integrated RF Solutions, Inc.), AnswerFAX Doc. No. 99624.

[2] “2.4GHz Direct Sequence Wireless LAN Cascade Analysis”, Robert Rood, Doug Schultz, Proc. of the Sixth Annual Wireless Symposium, pp. 532-540.

[3] *AN9665 Application Note*, Harris Semiconductor, “PRISM™ Power Management Modes” Carl Andren, Tim Bozych, Bob Rood and Doug Schultz (Integrated RF Solutions, Inc.), AnswerFAX Doc. No. 99665.

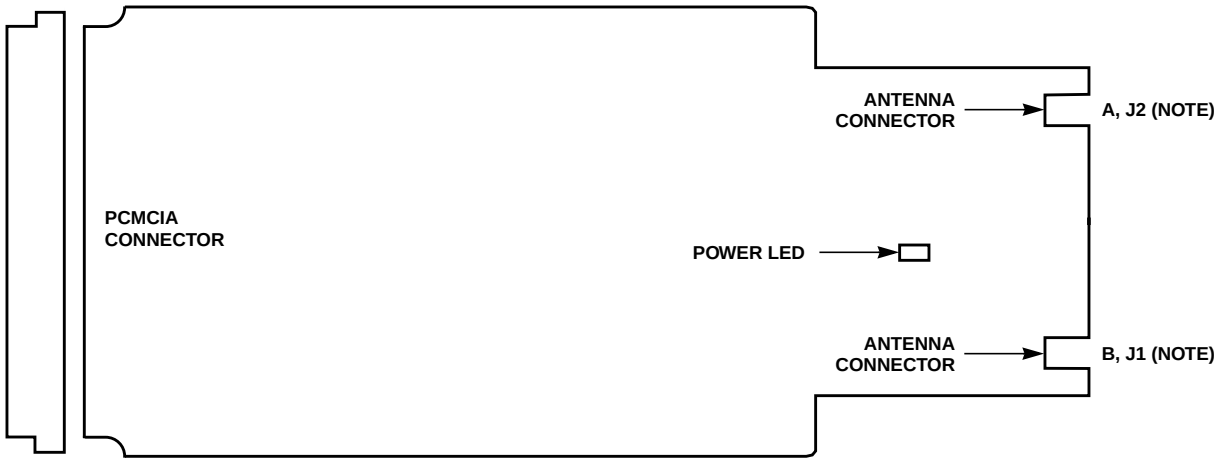
[4] *AN9790 Application Note*, Harris Semiconductor, “PRISM1KIT-EVAL PC Card Wireless LAN Evaluation Kit User’s Guide” Bill Garon, AnswerFAX Doc. No. 99790.

[5] *HFA3860B Data Sheet*, Harris Semiconductor, “Direct Sequence Spread Spectrum Baseband Processor”, AnswerFAX Doc. No. 94594.

[6] *AN9617 Application Note*, Harris Semiconductor, “Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the AM79C930 Media Access Controller”, John Fakatselis and Mike Paljug, AnswerFAX Doc. No. 99617.

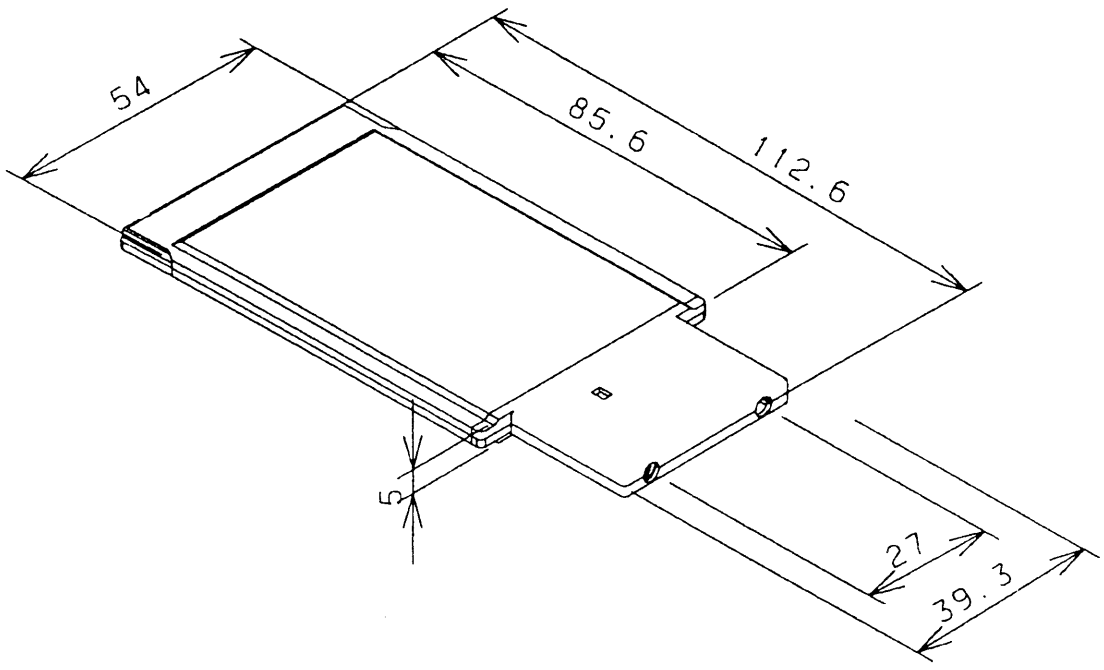
[7] *HFA3524, HFA3524A Data Sheet*, Harris Semiconductor, “2.5GHz/600MHz Dual Frequency Synthesizer”, AnswerFAX Doc. No. 94062.

Radio Card Outline - Top View



NOTE: A and B refer to Baseband Processor HFA3860B data sheet [5], J1 and J2 (refer to HWB1151-EVAL schematic).

Radio Card Dimensional Outline



NOTE: Units are in millimeters.