AN11806

TWR-POSCARD Hardware description

Rev. 1.0 — 3 March 2016
366410

Application note
COMPANY CONFIDENTIAL

Document information

Info	Content
Keywords	TWR_POSCARD, SPI, E.M.V, Kinetis, PN5180, TDA8035
Abstract	This application note describe the TWR_POSCARD evaluation board to be used with NXP’s Kinetis K80 family chip.

Revision history

Rev	Date	Description
1.0	20160303	Initial revision

Contact information

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1. Presentation

TWR-POSCARD is a peripheral module board to be used with NXP's Tower system.

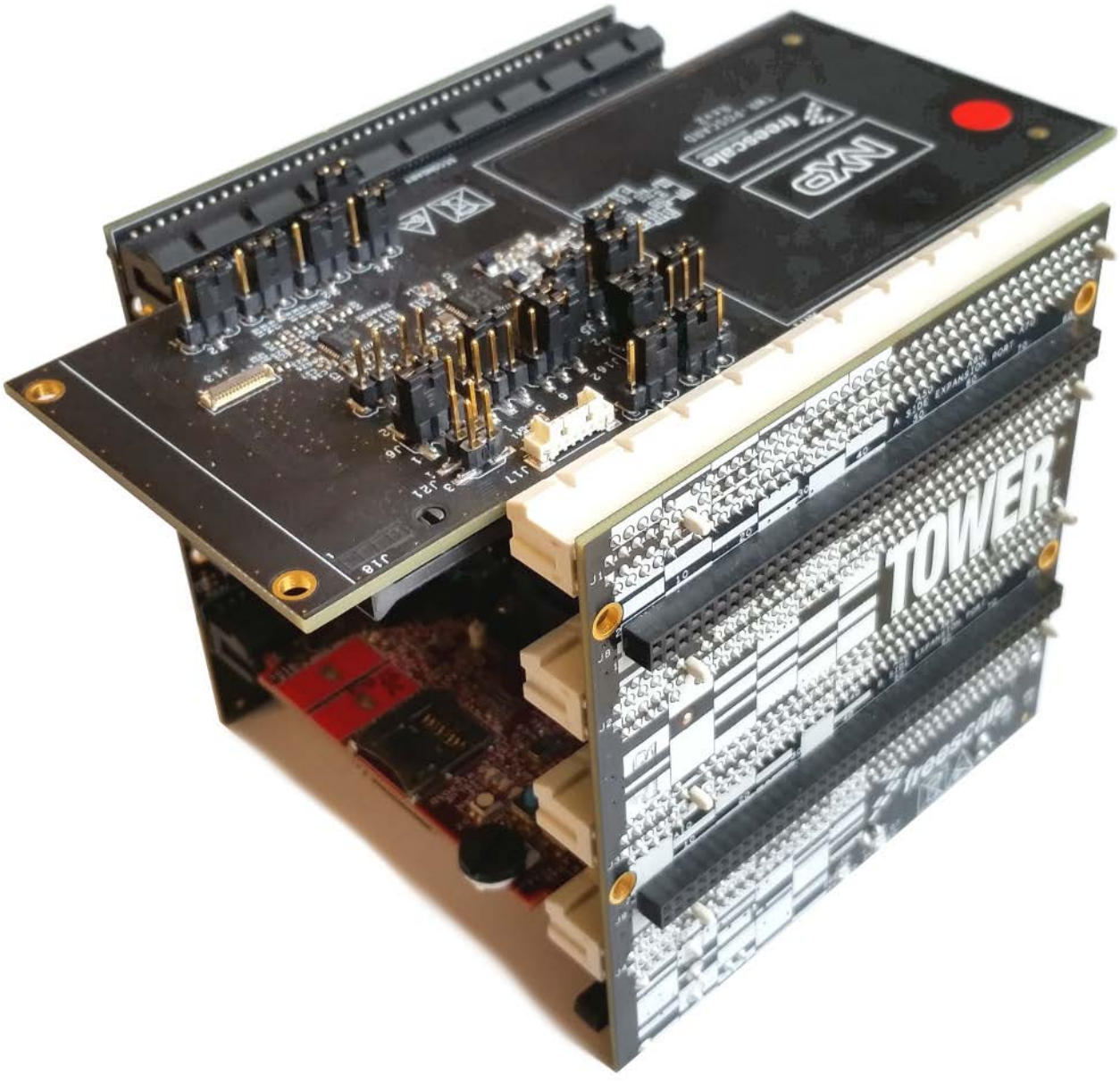


Fig 1. Tower System

1.1 Daughter board

TWR-POSCARD is a peripheral board that can be plugged into a tower system to add Contact and Contactless EMV reader functionality.

TWR-POSCARD is the below board:

Fig 2. TWR-POSCARD V2 Top view

This board can be plugged as in Fig 1, using the TWR-ELEV boards (side connector boards).

When plugging this board, the Primary and Secondary connection sides have to be respected. PCI secondary and primary connector are identified on TWR-POSCARD, and on TWR-ELEV card, see below figure.

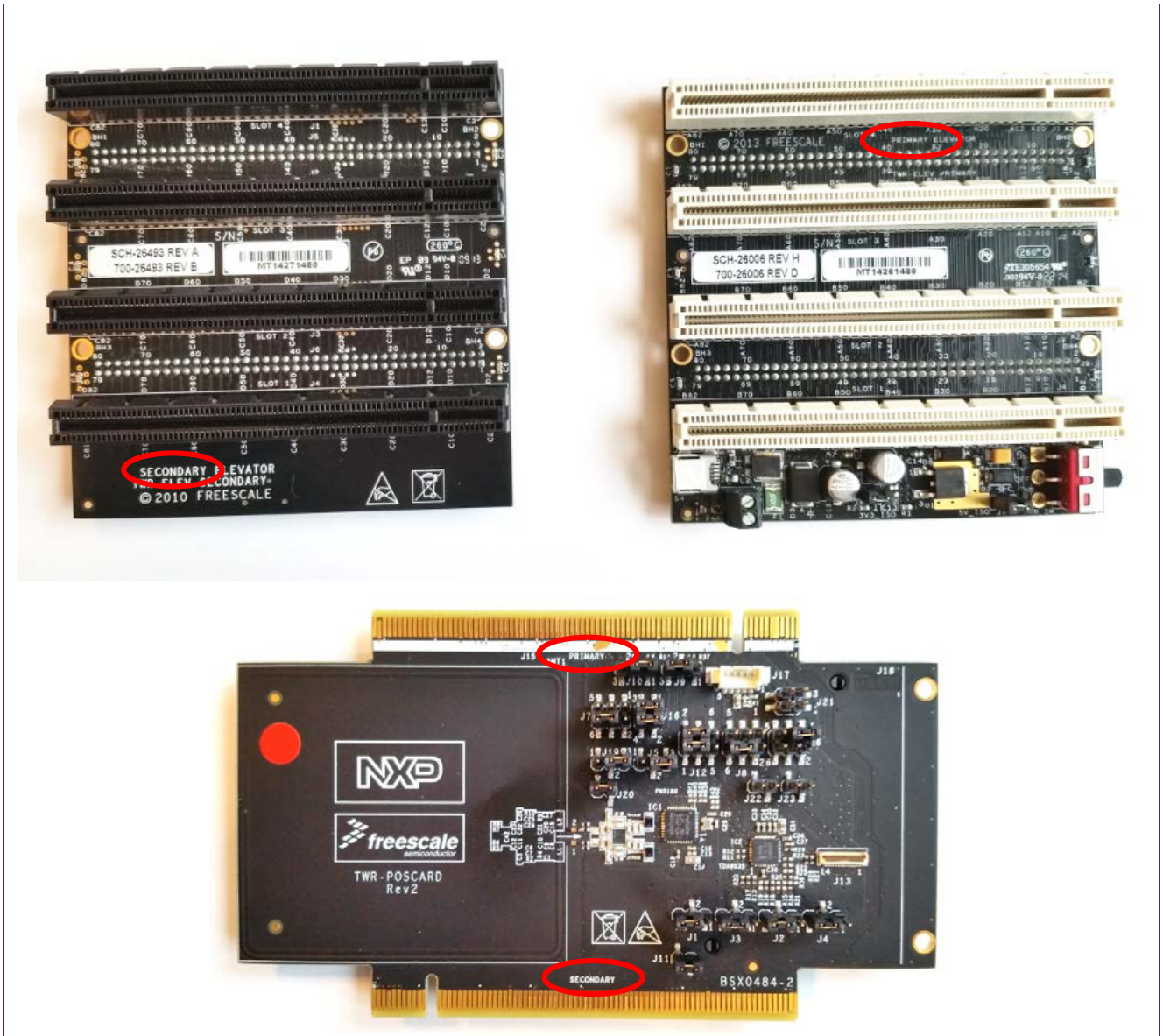


Fig 3. TWR-Elev: Secondary and Primary

1.2 Architecture

The TWR-POSCARD peripheral board embeds ICs to provide Contact and Contactless payment functionalities.

The board uses the following ICs:

- PN5180: NXP Contactless Front-end reader
- TDA8035: NXP Contact Front-end reader device.

Both devices are compliant with latest payment specifications (EMVCo)

The reader ICs are controlled by an MCU or processor module, through the side connectors, plugged on Tower system.

In order to interface with smart cards, the TWR-POSCARD board is autonomous as it embeds an antenna connected to PN5180 to interact with Contactless cards, and a contact smart card connector, connecting the smart card to the TDA8035.

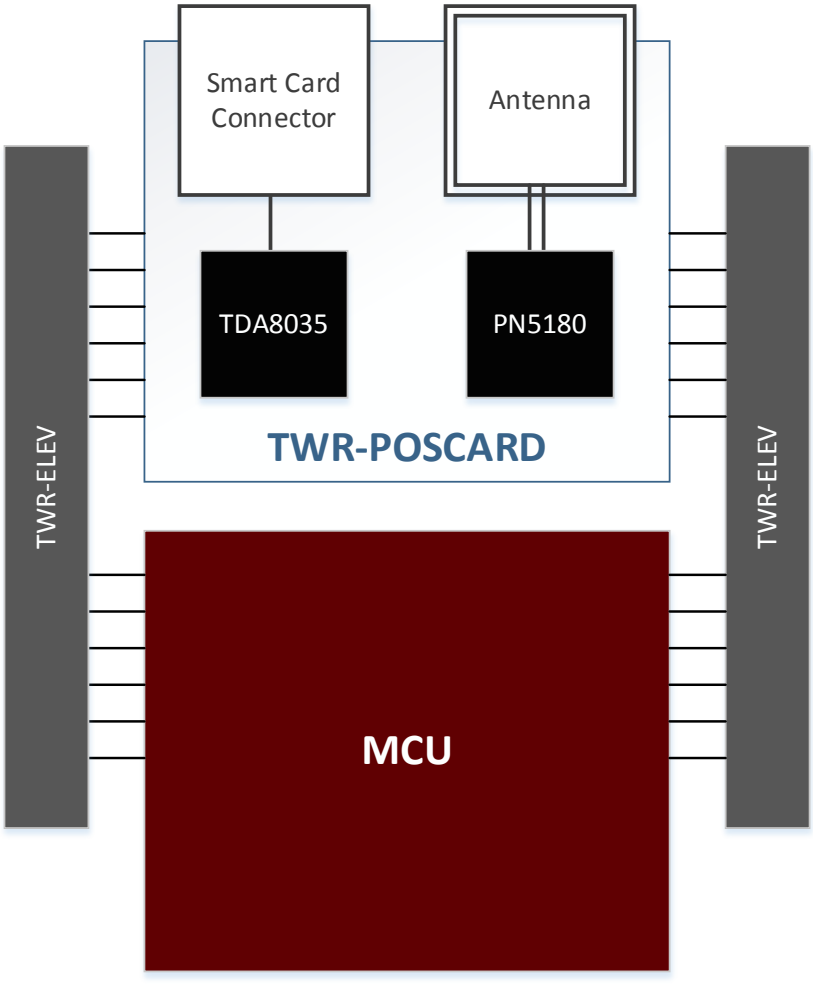


Fig 4. Architecture view

1.3 Configuration

The TWR-POSCARD peripheral board embeds several configuration jumpers. They are used to enable several Tower MCU or processor modules to be used as the controller.

Below table shows the default configuration when the TWR-K80F150M is used as the MCU module. Other configurations can be set depending on the MCU or processor module board that is used.

Table 1. Configuration jumpers for K81

Jumper Name	Function	Options (default in bold)	Connection
J1	PN5180 SPI NSS	SPI1_CS0 - Pin B9 on Elevator	1-2
		SPI0_CS0 - Pin B46 on Elevator	**2-3**
J2	PN5180 SPI MISO	SPI1_MISO - Pin B11 on Elevator	1-2
		SPI0_MISO - Pin B44 on Elevator	**2-3**
J3	PN5180 SPI MOSI	SPI1_MOSI - Pin B10 on Elevator	1-2
		SPI0_MOSI - Pin B45 on Elevator	**2-3**
J4	PN5180 SPI SCL	SPI1_CLK - Pin B7 on Elevator	1-2
		SPI0_CLK - Pin B48 on Elevator	**2-3**
J5	PN5180 IRQ	IRQ_A - Pin B62 on Elevator	1-2
		IRQ_F - Pin B57 on Elevator	**2-3**
J6	TDA8035 Presence N	**PWM3 - Pin A37 on Elevator**	**1-3**
		GPIO14 - Pin A50 on Elevator	3-5
		ULPI_DATA1 - Pin C22 on Elevator	4-6
J7	TDA8035 Clock input	PWM1 - Pin A39 on Elevator	1-3
		PWM0 - Pin A40 on Elevator	3-5
		I2S1_DIN_SCK - Pin C58 on Elevator	**4-6**
J8	TDA8035 RSTIN	GPIO17 - Pin A53 on Elevator	1-3
		PWM2 - Pin A38 on Elevator	3-5
		I2S1_DIN_WS - Pin C59 on Elevator	**4-6**
J9	TDA8035 IOUC	ETH_RXDV_1 - Pin A16 on Elevator	1-2
		I2S0_DOUT_SCK - Pin A22 on Elev.	**2-3**
J10	TDA8035 IOUC	**UART0_TX - Pin A42 on Elevator**	**1-2**
		UART1_TX - Pin A44 on Elevator	2.3
J11	TDA8035 IOUC	**I2S1_DOUT1 - Pin C61 on Elevator**	**1-2**
J12 1-3-5	TDA8035 CMDVCCN	**ULPI_DATA4 - Pin C25 on Elevator**	**1-3**
		GPIO1 - Pin B21 on Elevator	3-5
J12 2-4-6	TDA8035 OFFN	**IRQ_C - Pin B60 on Elevator**	**2-4**
		IRQ_B - Pin B61 on Elevator	4-6
J16 1-2	Connect MCU_ICC_PDA37	PWM3 - Pin A37 on Elevator	1-2

Jumper Name	Function	Options (default in bold)	Connection
J16 3-4	Connect MCU_ICC_RST_A38	PWM2 - Pin A38 on Elevator	3-4
J19	PN5180 BUSY	IRQ_D - Pin B59 on Elevator **IRQ_E - Pin B58 on Elevator**	1-2 **2-3**
J20	PN5180 RESET	**SPI1_CS1 - Pin B58 on Elevator**	**1-2**
J21 1-2	Connect MCU_MSR_DATA	TMR1 - Pin A33 on Elevator	1-2
J21 3-4	Connect MCU_MSR_STROBE	TMR0 - Pin A34 on Elevator	1-2
J22	Connect MCU_ICC_CVVV_SEL0	GPIO3 - Pin B23 on Elevator	1-2
J23	Connect MCU_ICC_CVVV_SEL1	GPIO9 - Pin A9 on Elevator	1-2

2. Design files

2.1 Schematics

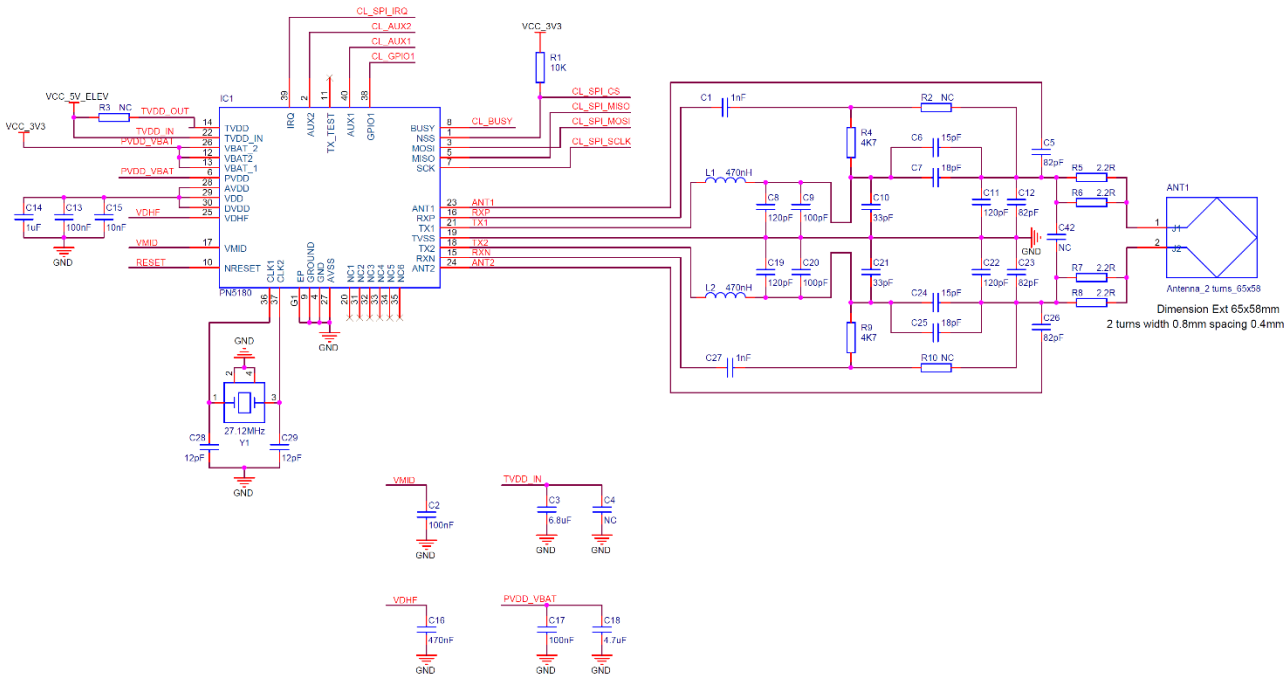


Fig 5. Contactless Front-end

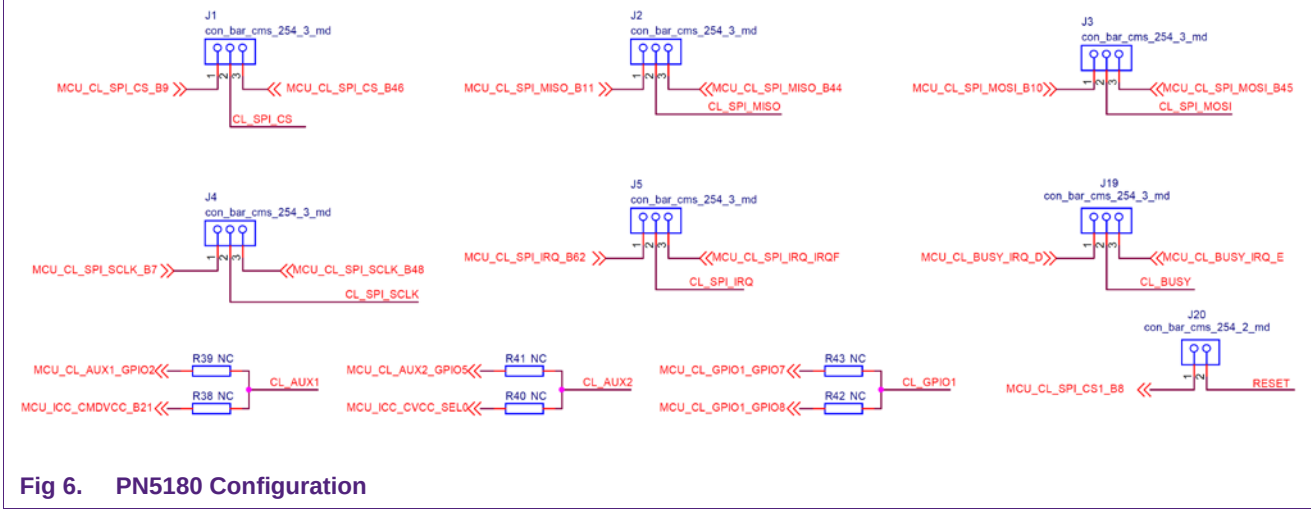


Fig 6. PN5180 Configuration

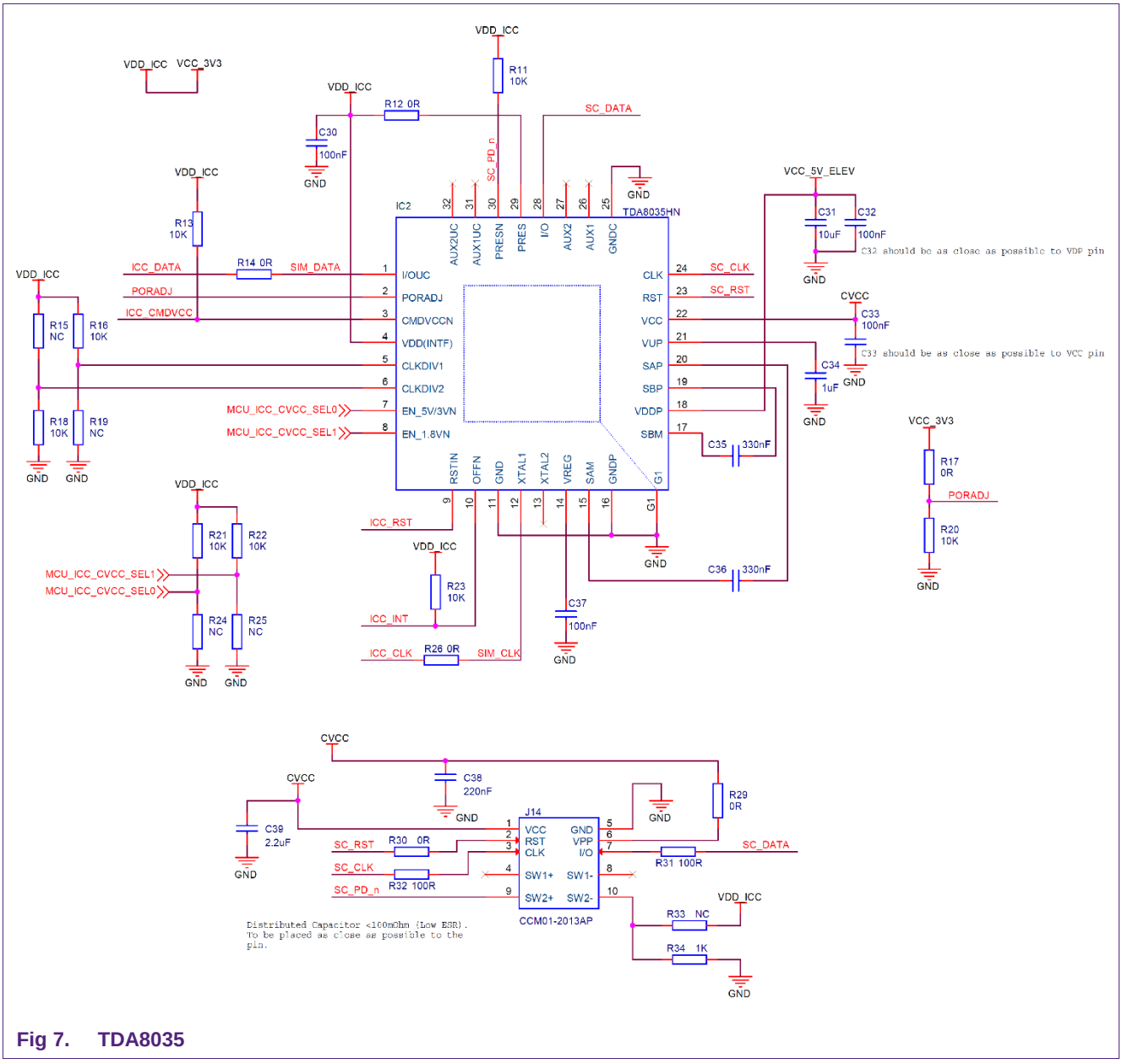
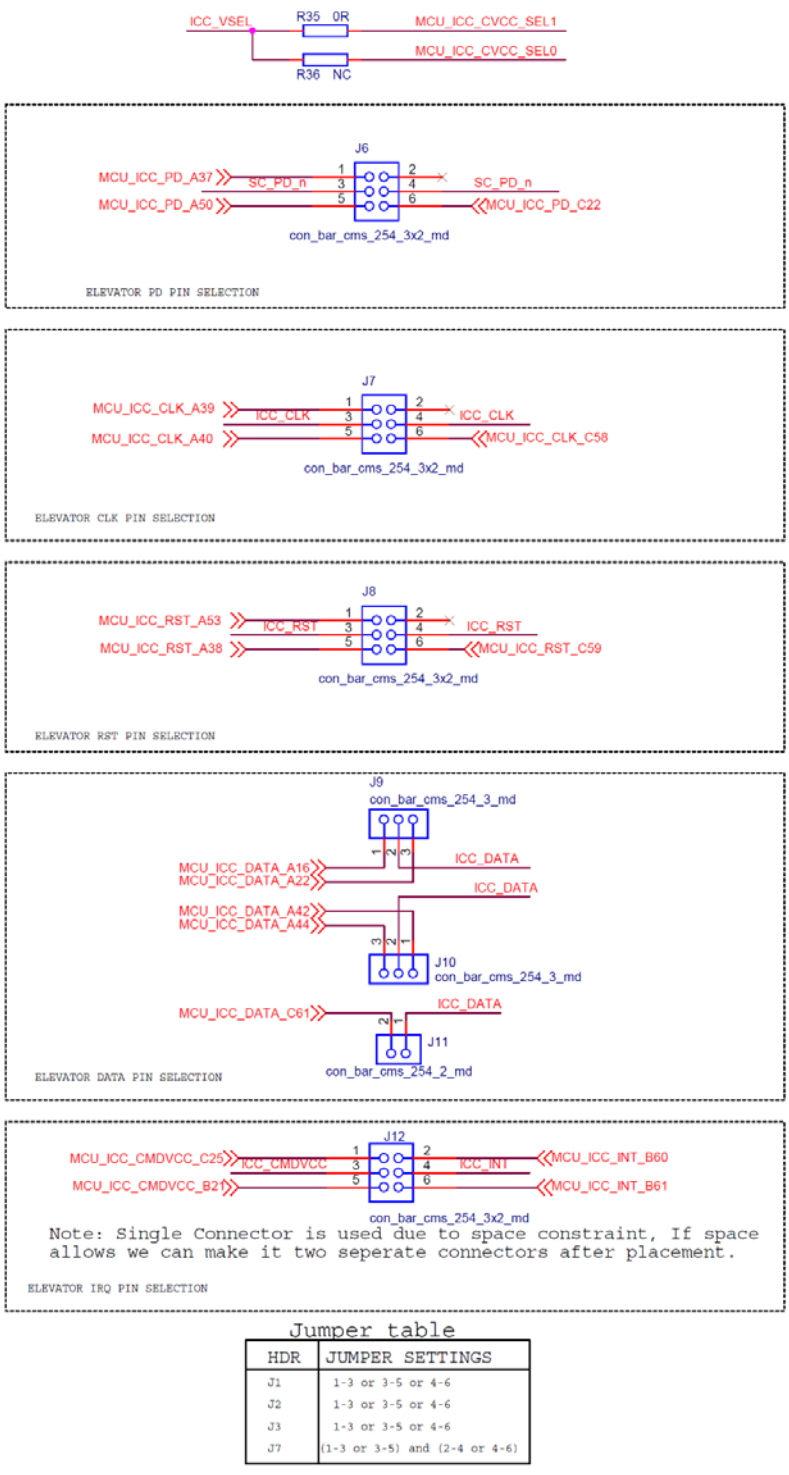


Fig 7. TDA8035



Jumper table

HDR	JUMPER SETTINGS
J1	1-3 or 3-5 or 4-6
J2	1-3 or 3-5 or 4-6
J3	1-3 or 3-5 or 4-6
J7	(1-3 or 3-5) and (2-4 or 4-6)

Fig 8. Contact Jumper settings

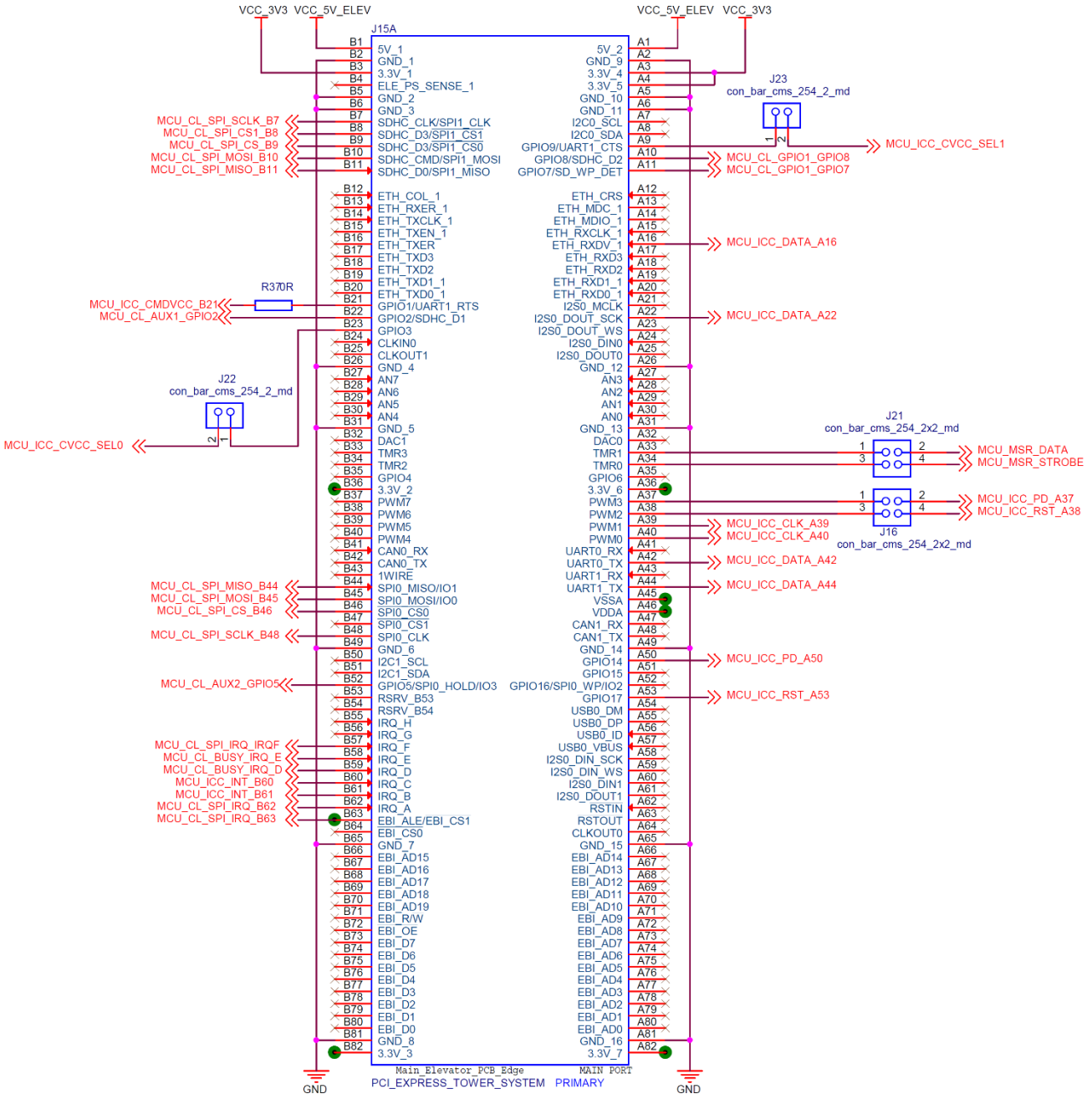


Fig 9. Tower Connector - Primary

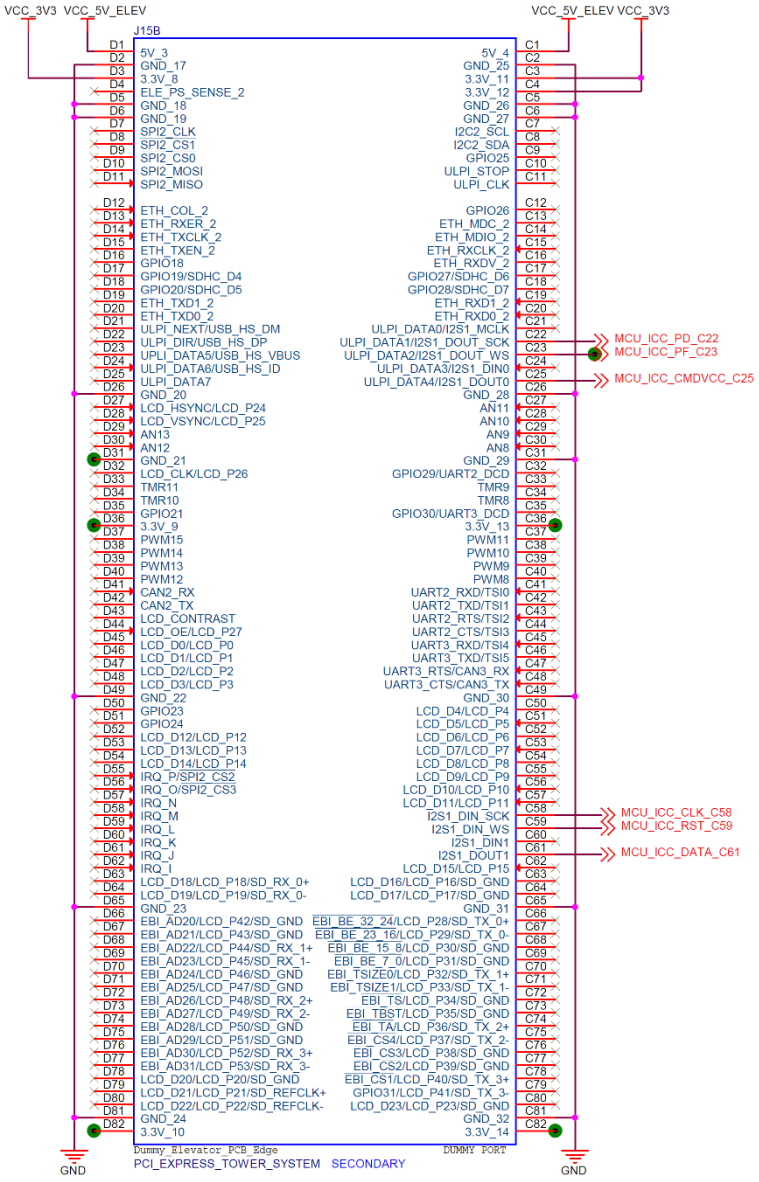


Fig 10. Tower Connector - Secondary

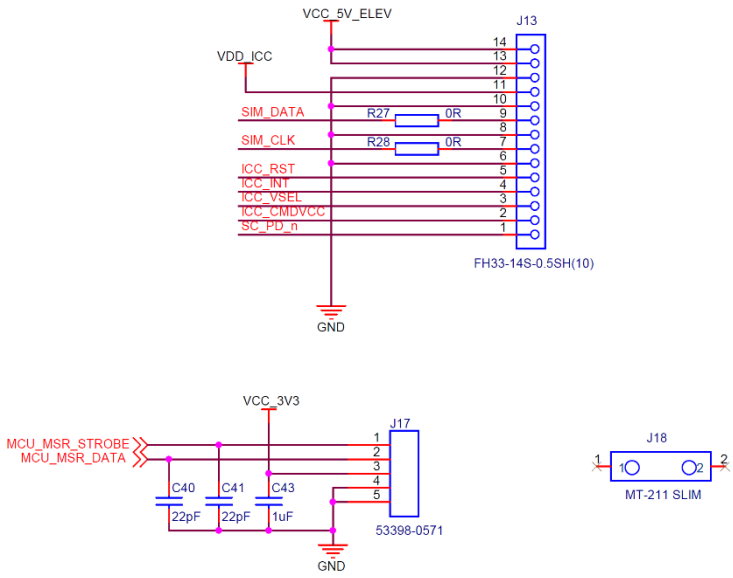


Fig 11. Other

2.2 Layout and placement

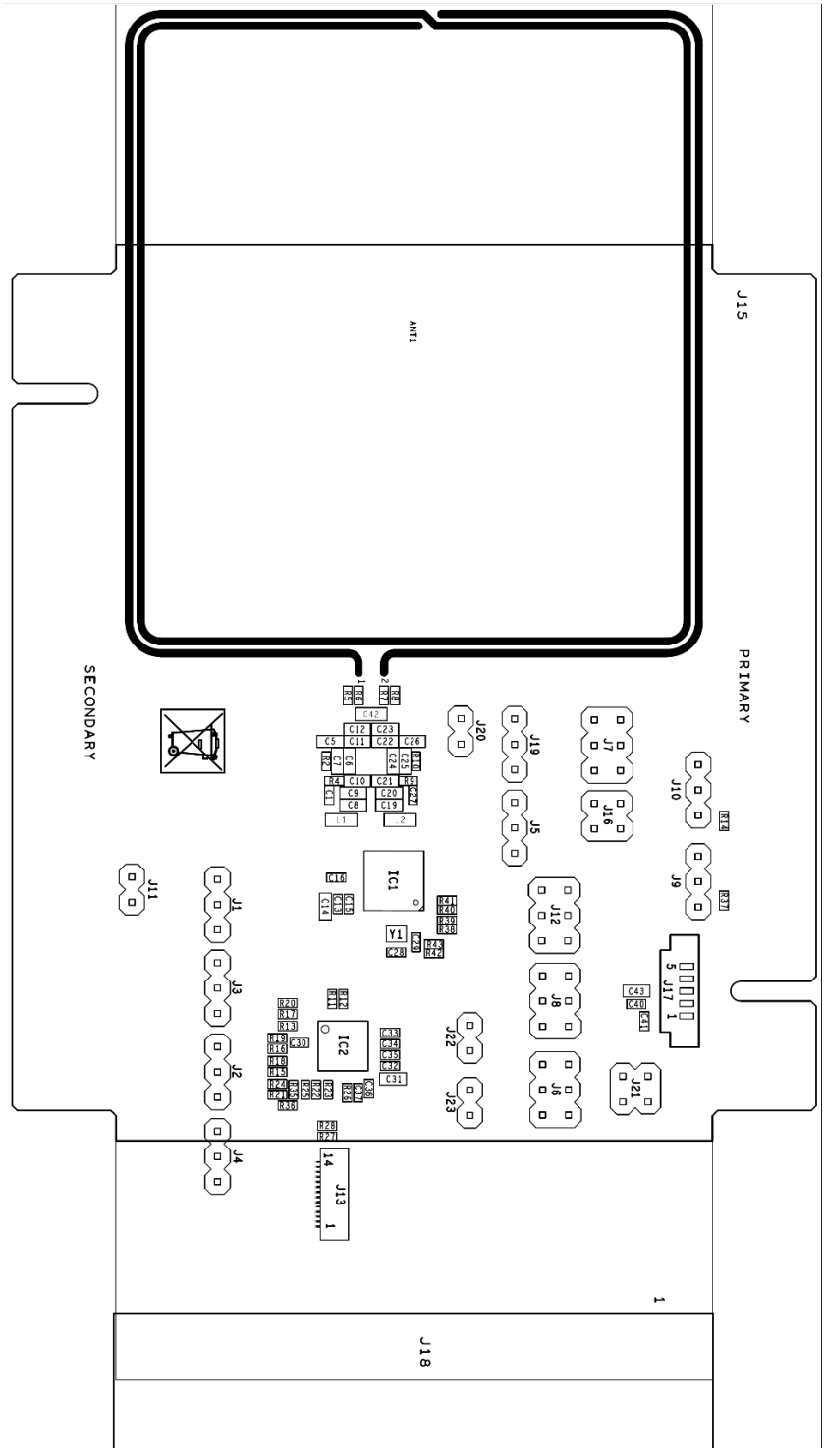


Fig 12. Board placement

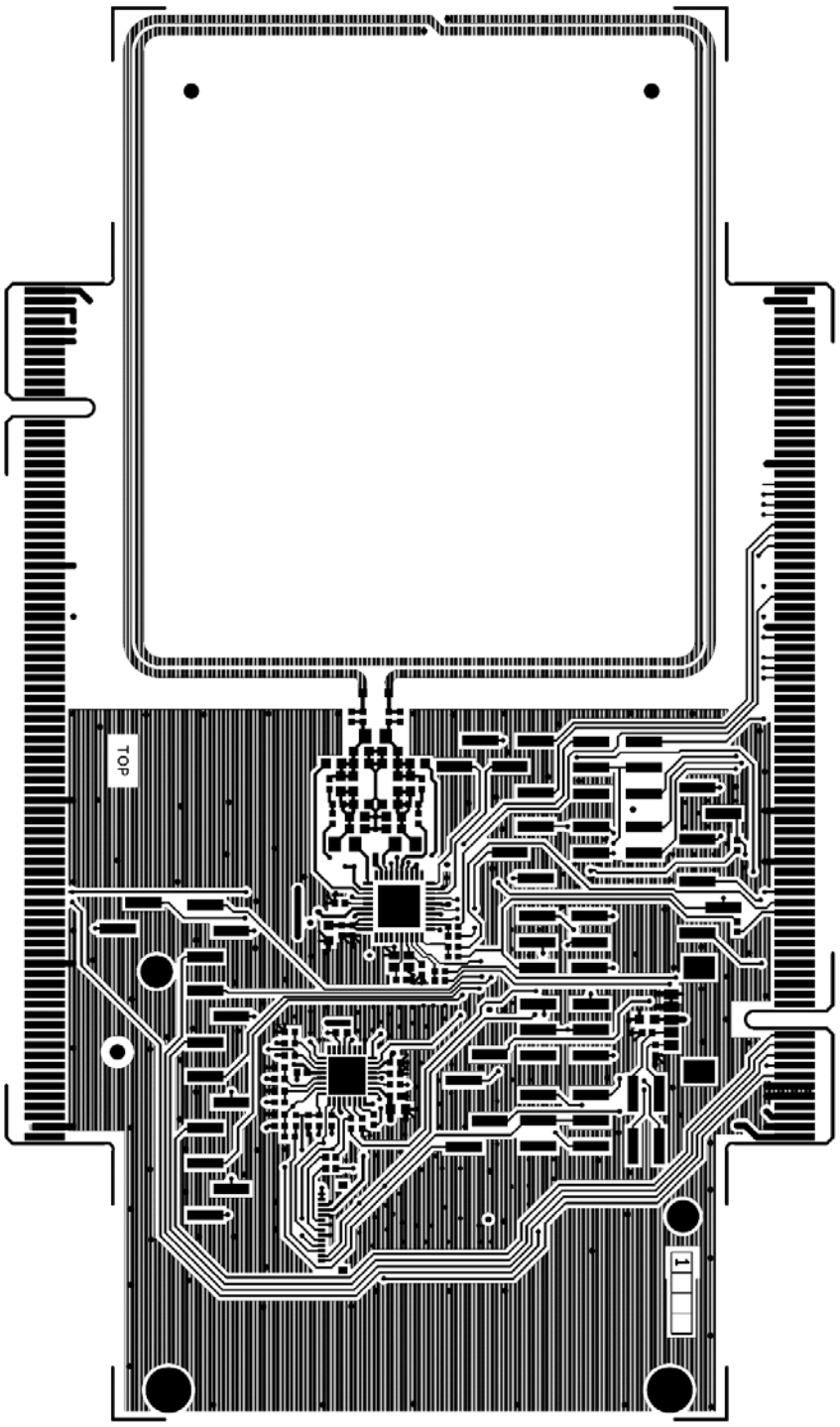


Fig 13. Layout TOP

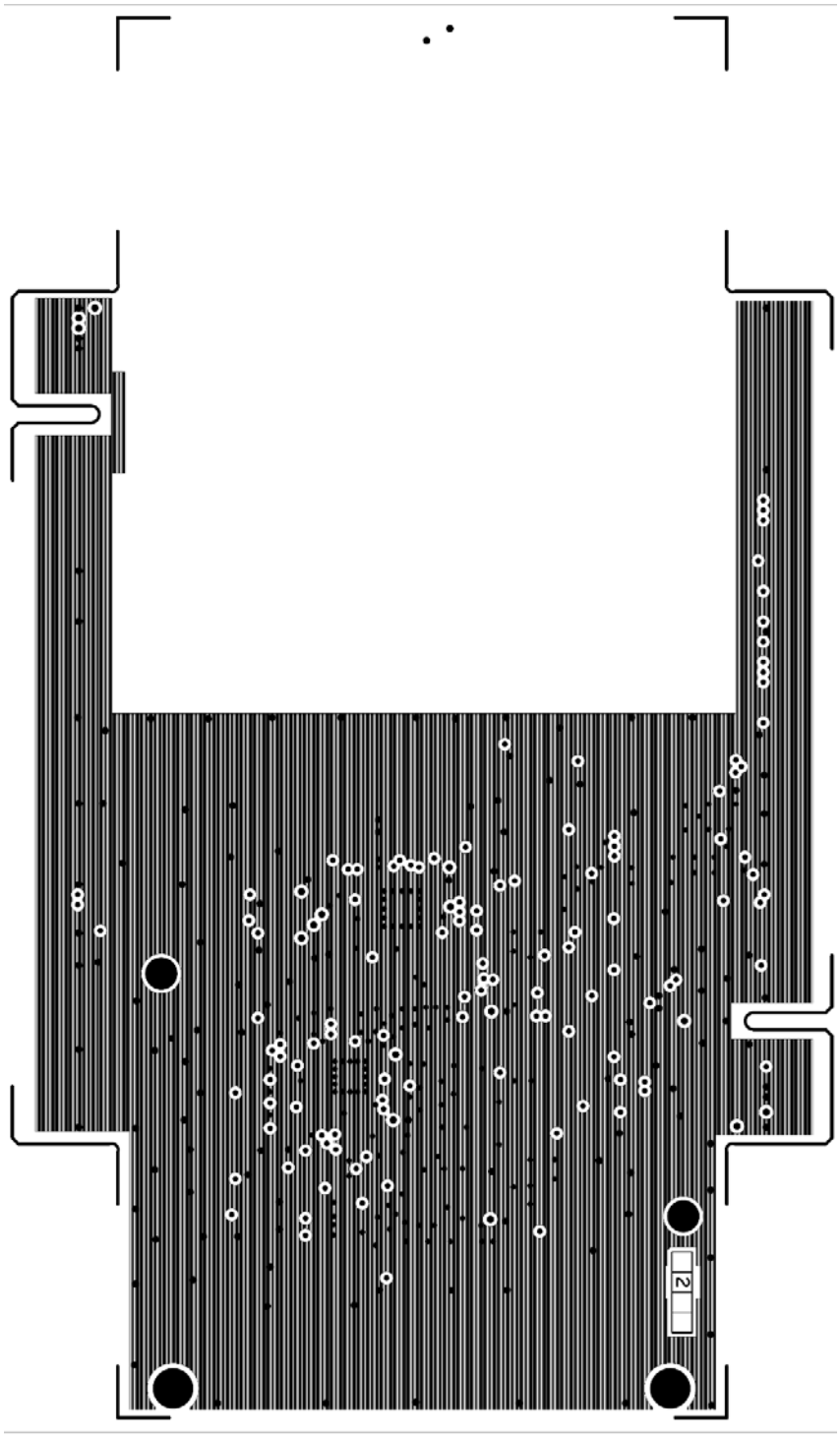


Fig 14. Layer in #1

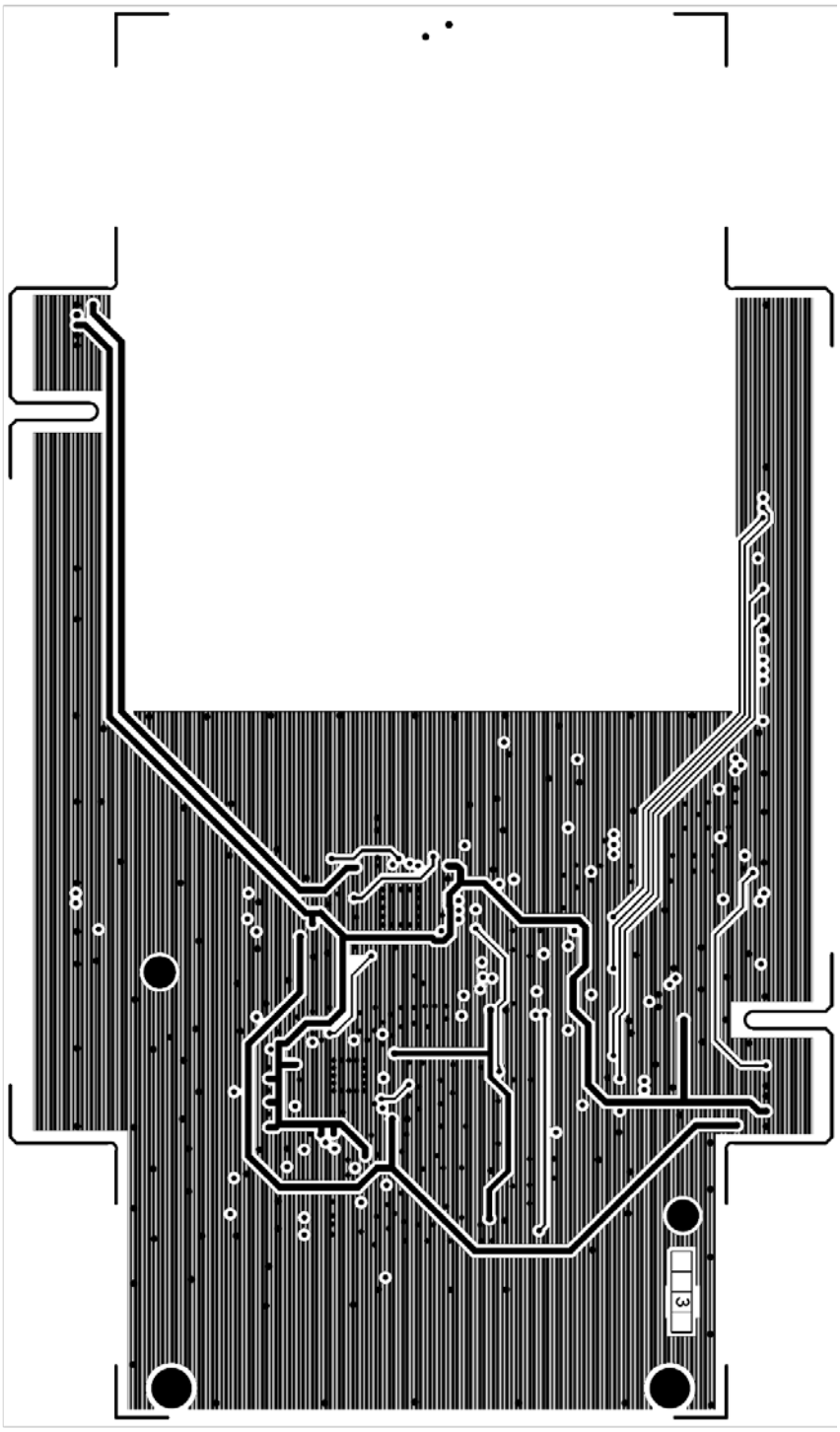


Fig 15. Layer in #2

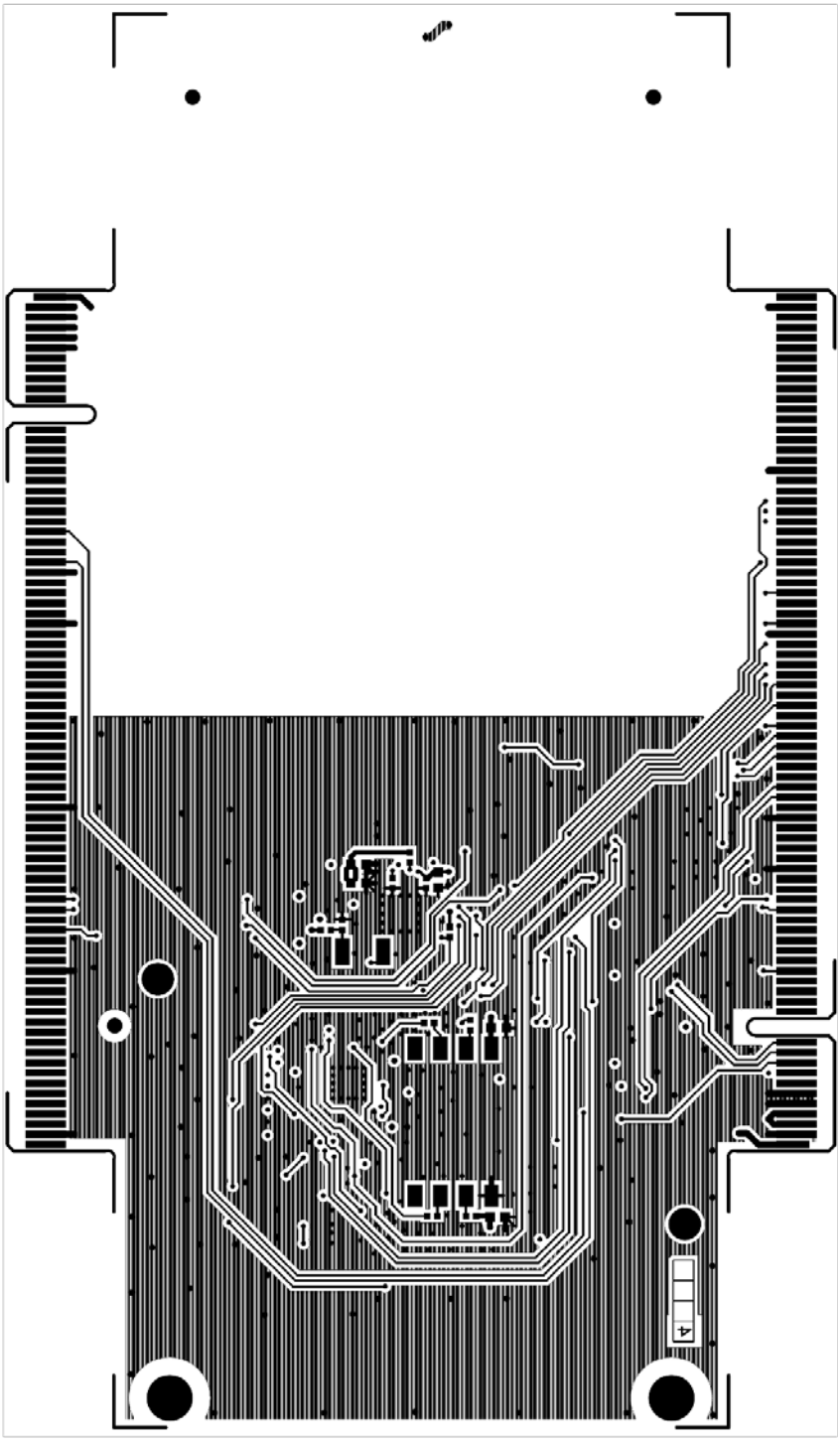


Fig 16. Layout Bottom

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Date of release: 3 March 2016
366410
Document identifier: AN11806