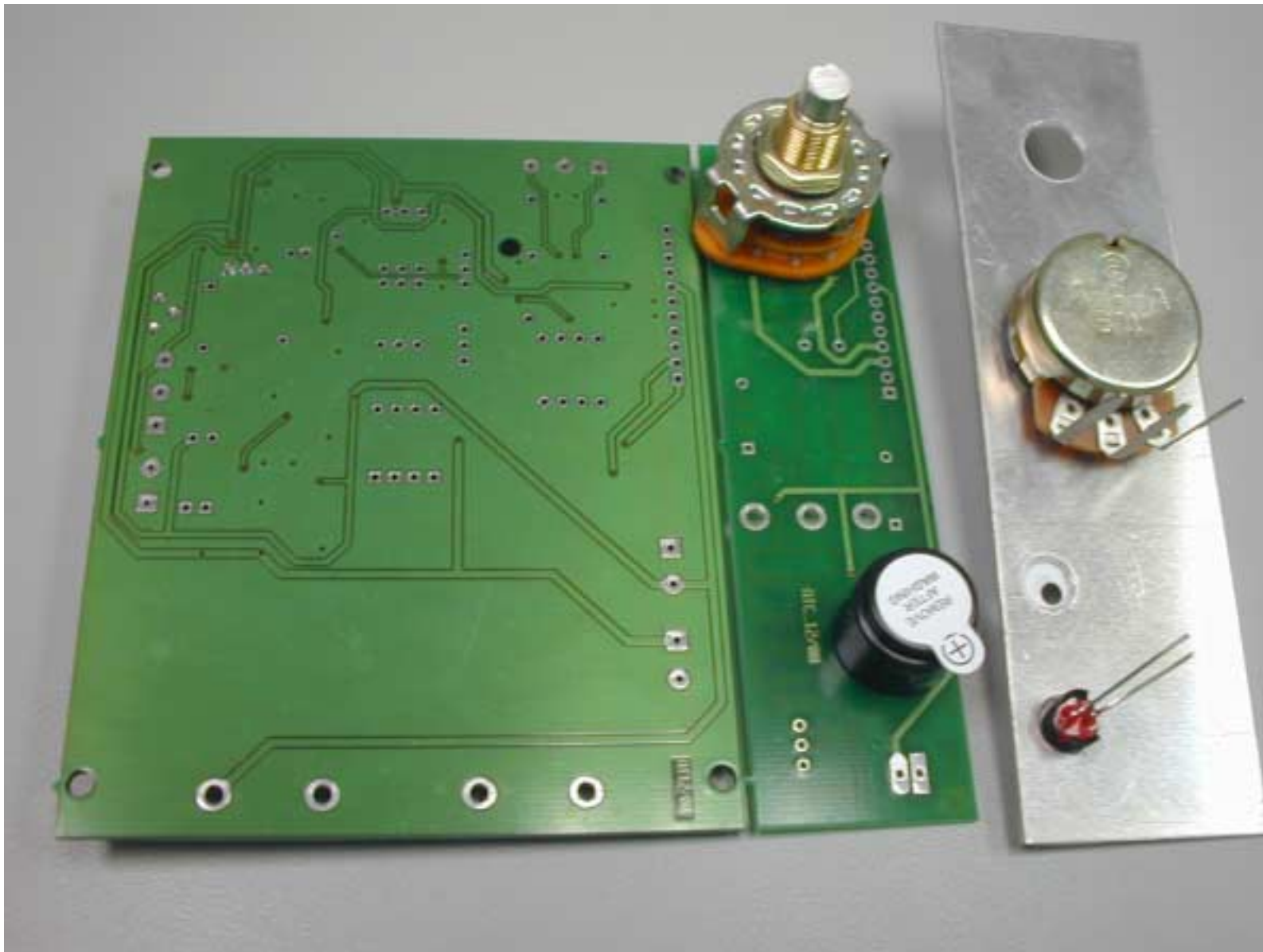
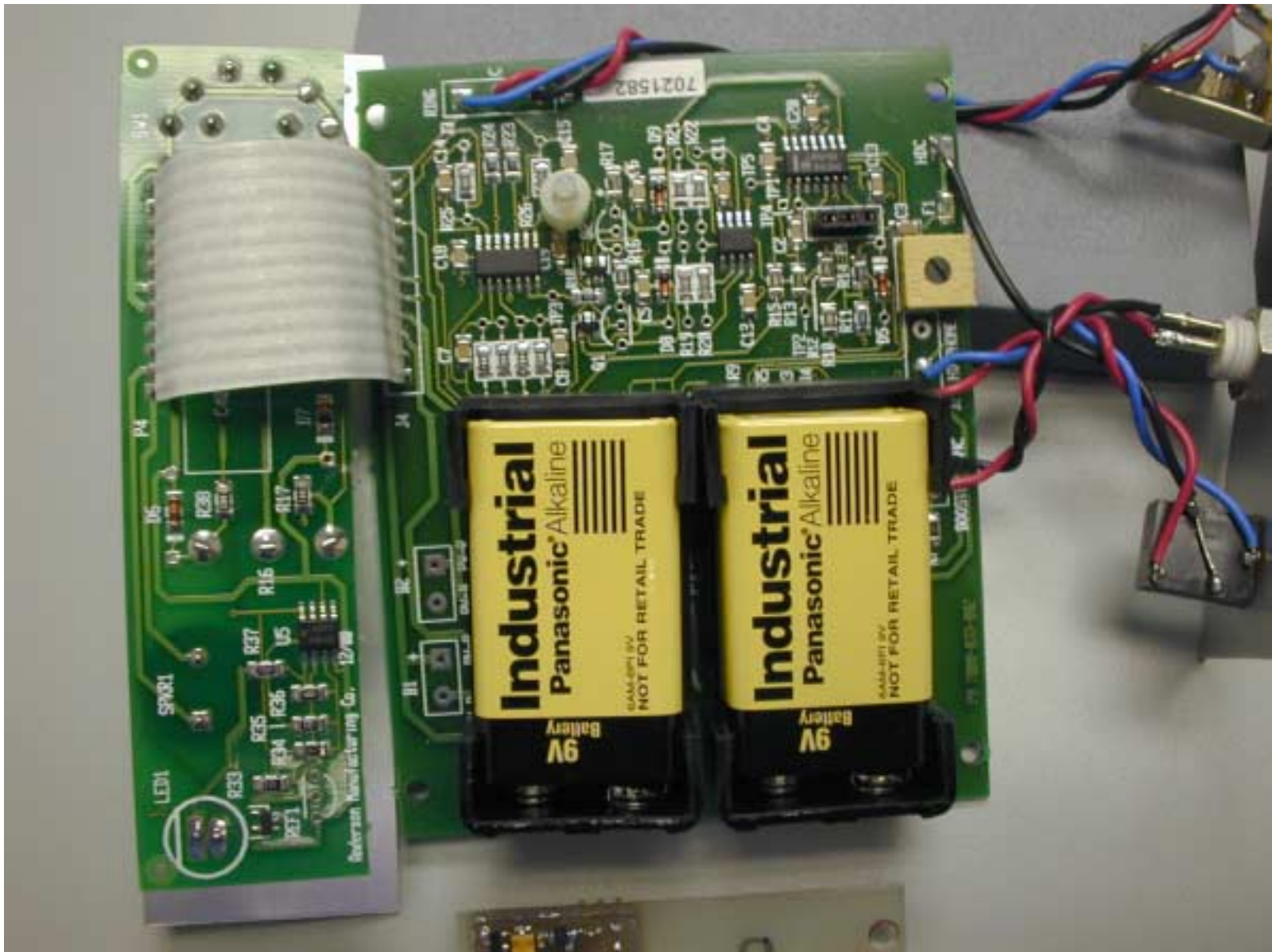




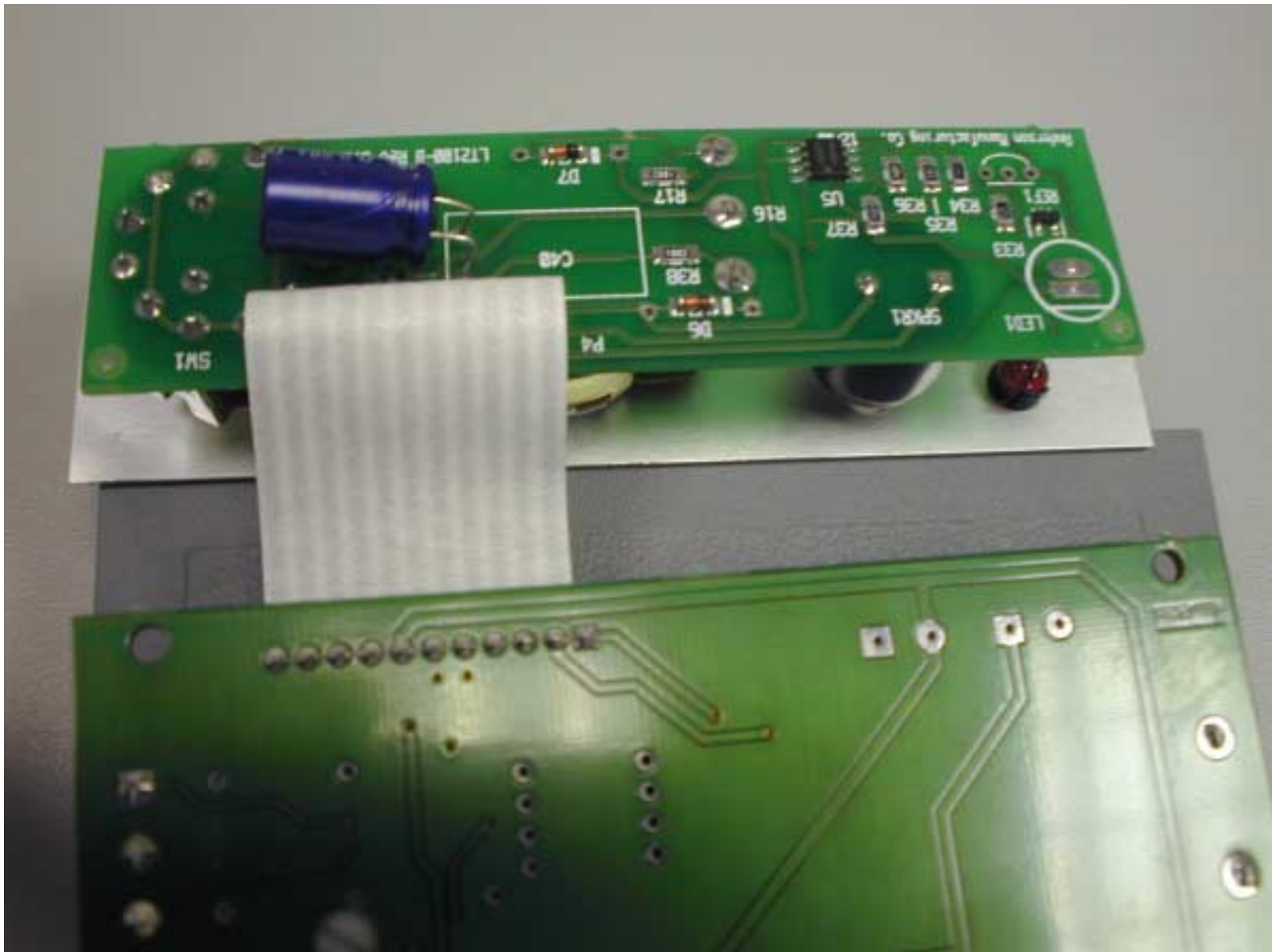


SPU Interface 2



SPU Interface 3

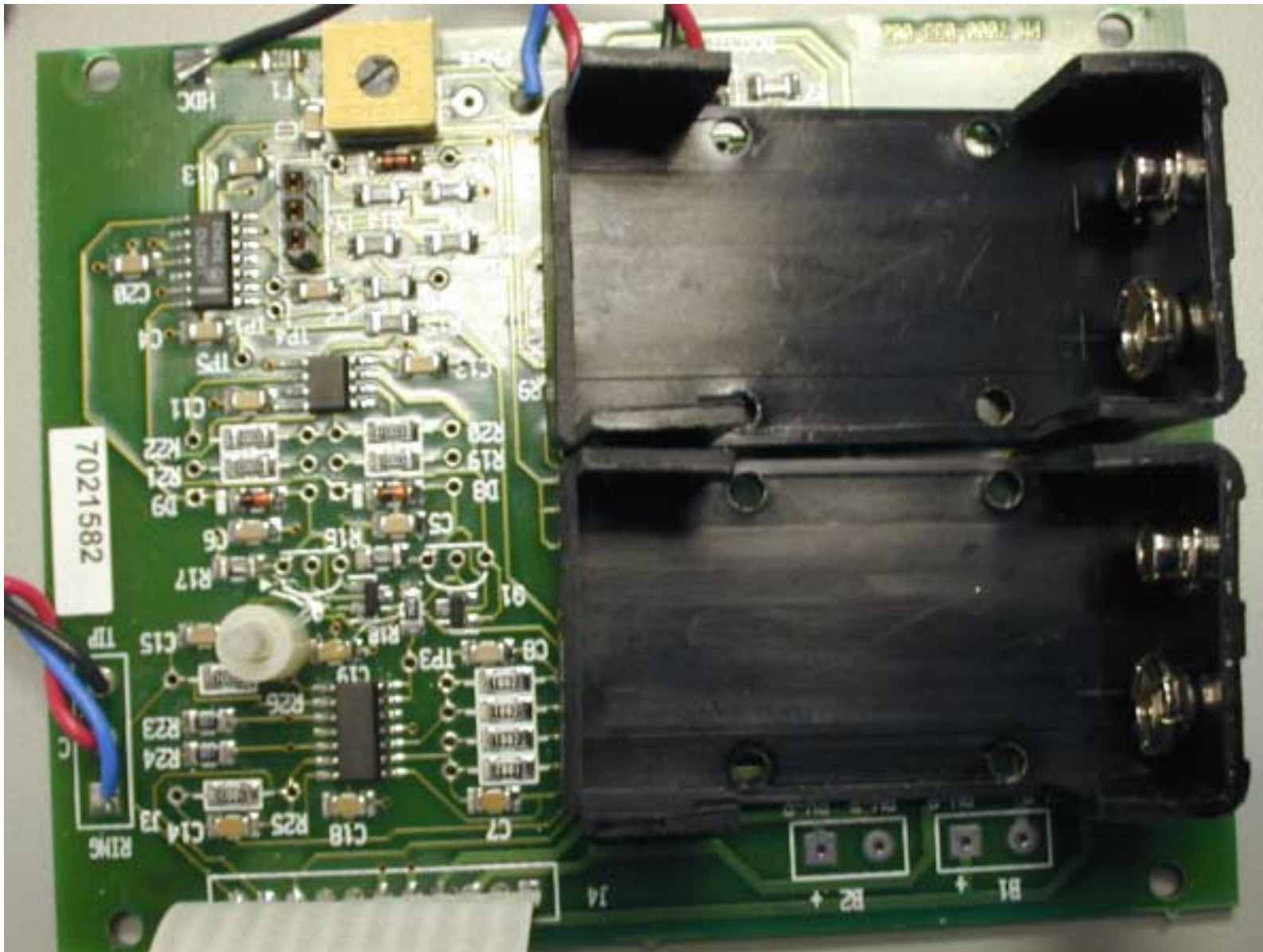




SPU interface 4

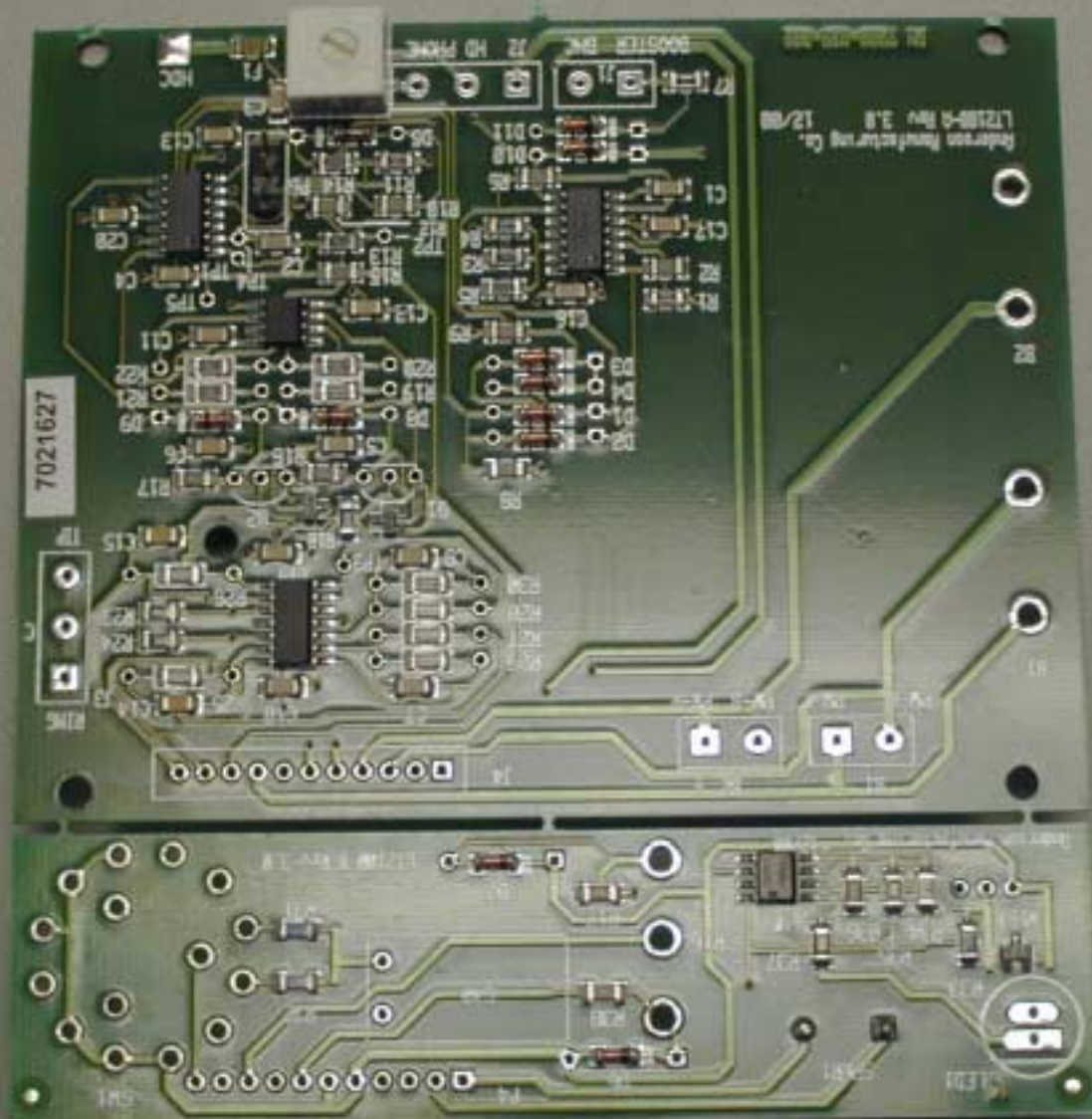


SPU Main

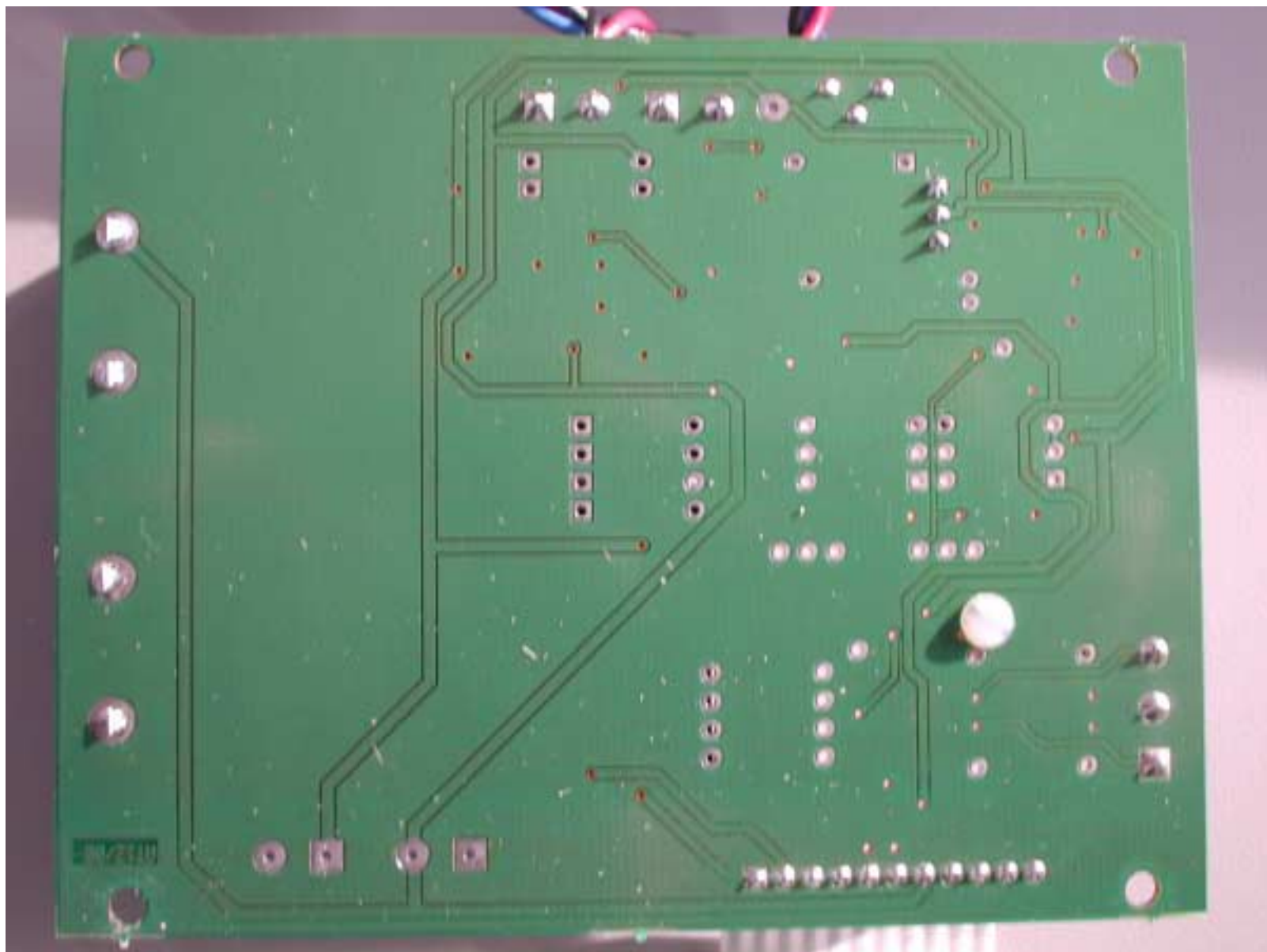


SPU Main 2





SPU Main 3



SPU Main bottom

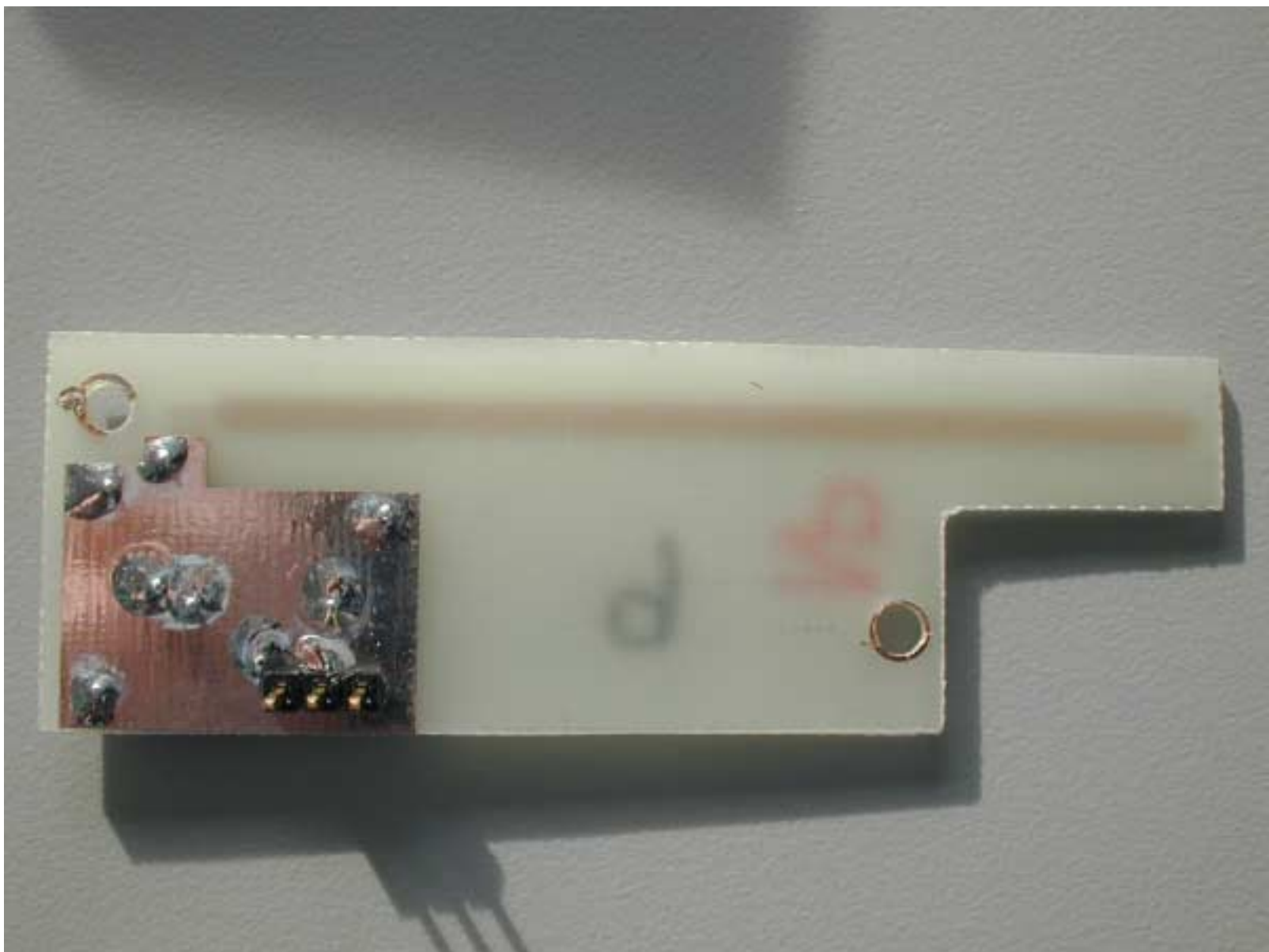




SPU Main with Transmitter



SPU transmitter



SPU XMTR bottom





SPU