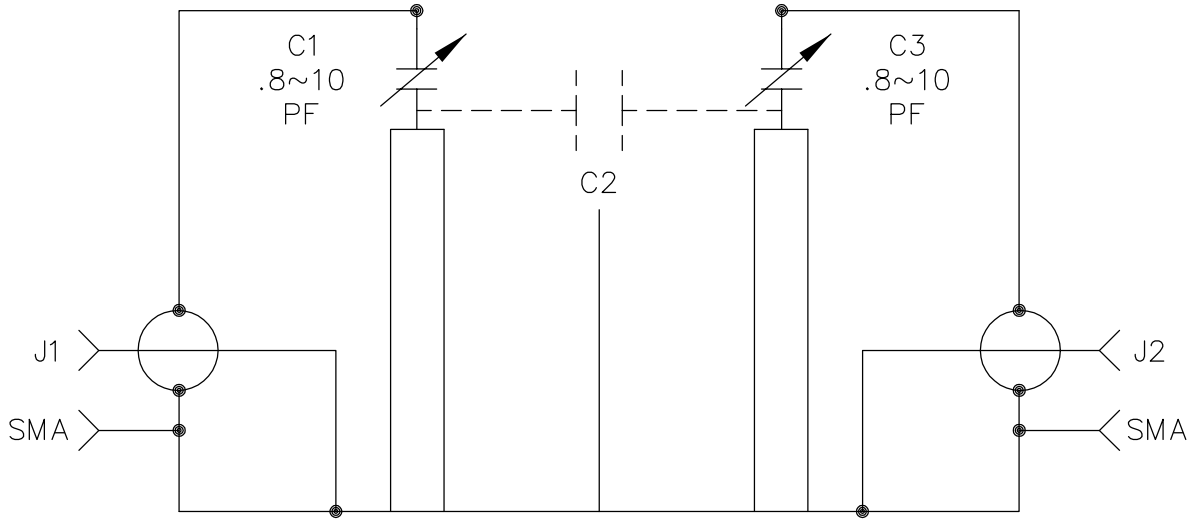

NOTE: C2 IS STRAY CAPACITANCE BETWEEN LINE SECTIONS.

REV	ECO	DATE	APV

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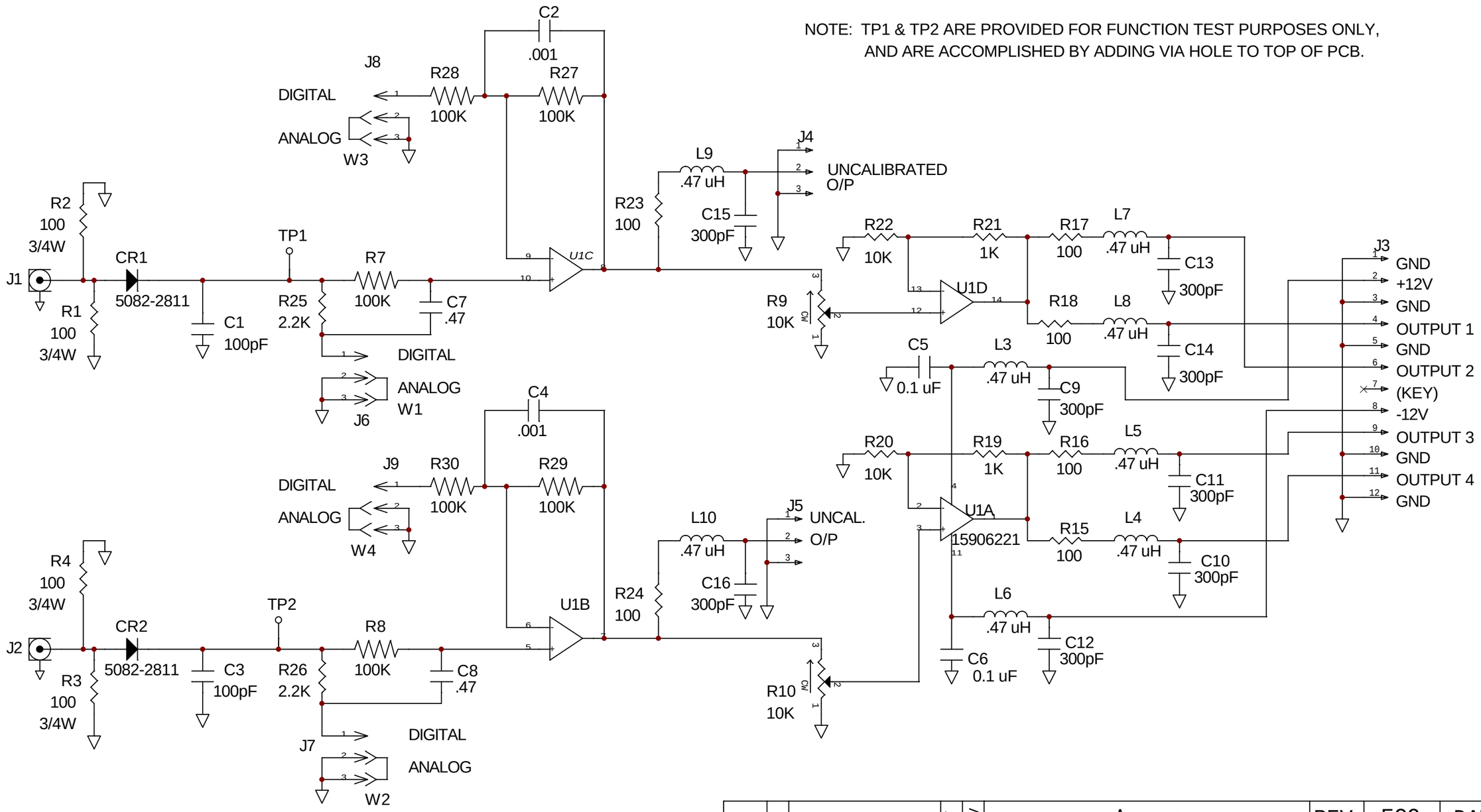
MATERIAL — — — —

FINISH — — — —

TITLE: SCHEMATIC — UHF FILTER

			DWG. NO.	REV
DWN	DD	9/13/83	1007-3101	0
CHK	RWZ	9/13/83		
REL	RWZ	7/20/90	A SCALE — —	SHEET 1 OF 1

NOTE: TP1 & TP2 ARE PROVIDED FOR FUNCTION TEST PURPOSES ONLY,
AND ARE ACCOMPLISHED BY ADDING VIA HOLE TO TOP OF PCB.



REV	ECO	DATE	APV
C0	20110722	5/16/03	LRT
B0	20092702	6/11/01	LRT

ADDED C2 & C4. JKF

REMOVED C2, C4, L1, L2, CR3, AND CR4. R25 AND R26 WERE 470K. R7 AND R8 WERE 2.2K. C7 AND C8 WERE .001. ADDED J8, J9, W3, W4, R27-R30. (PJK)

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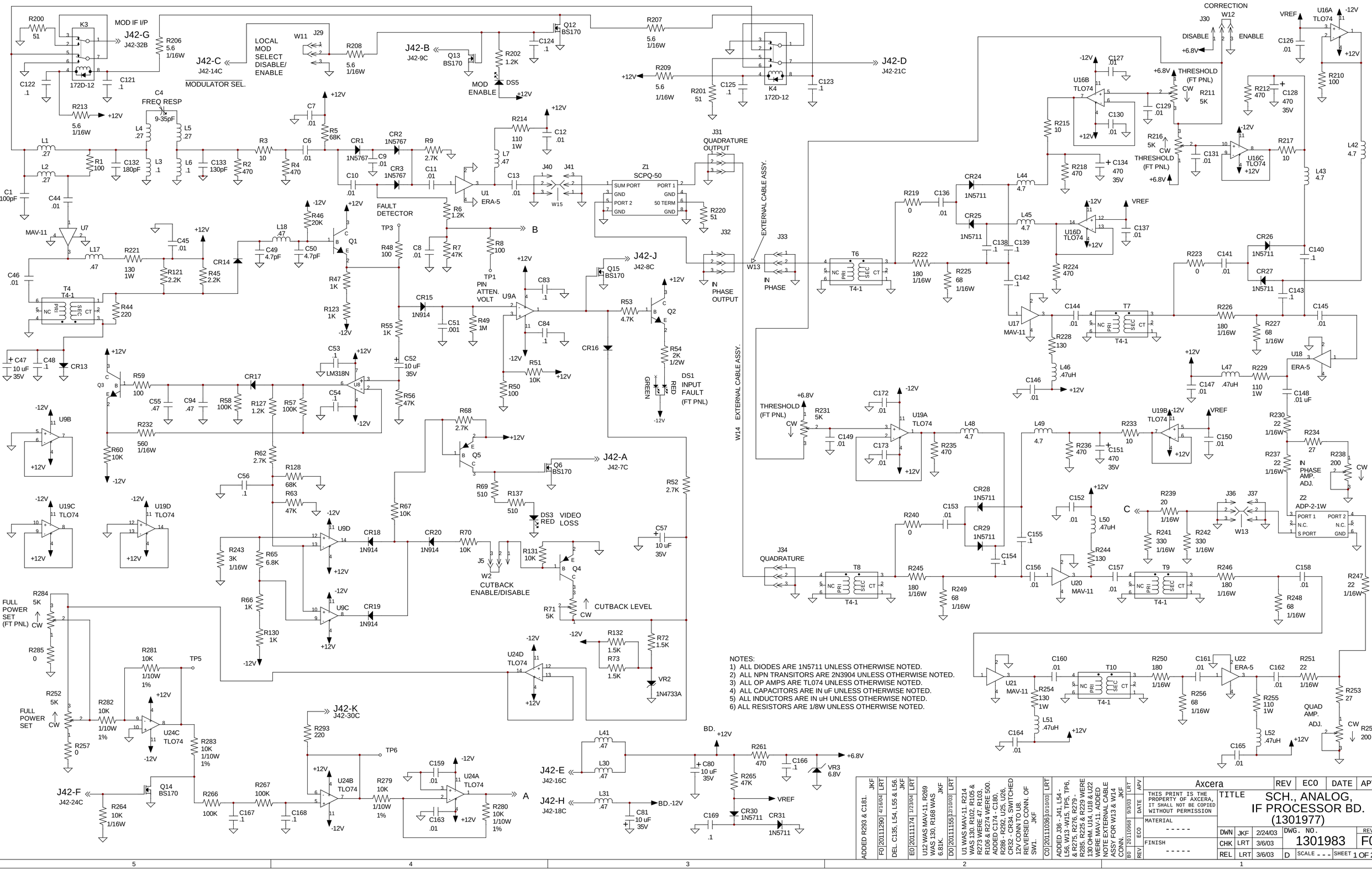
MATERIAL: - - - - -

FINISH: - - - - -

TITLE: SCH., DUAL PEAK DETECTOR, SMT (1159965)

			DWG. NO.	REV
DWN	PJK	2/23/00	1159976	C0
CHK	LRT	2/26/01		
REL	LRT	2/26/01	B	SCALE - - - SHEET 1 OF 1



NOTES:
1) ALL DIODES ARE 1N5711 UNLESS OTHERWISE NOTED.
2) ALL NPN TRANSITORS ARE 2N3904 UNLESS OTHERWISE NOTED.
3) ALL OP AMPS ARE TL074 UNLESS OTHERWISE NOTED.
4) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
5) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
6) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.

ADDED R293 & C181.	JKF		
FD | 20111290	4/16/04	LRT	
DEL. C135, L54, L55 & L56.		JKF	
ED | 20111174	1/23/04	LRT	
U12 WAS MAV-11, R269 WAS 130, R168 WAS 6.81K.		JKF	
DD | 20111155	12/10/03	LRT	
U1 WAS MAV-11, R214 WAS 130, R102, R105 & R273 WERE 47, R103, R106 & R274 WERE 500. ADDED C174 - C180, R286 - R292, U25, U26, CR32 - CR34, SWITCHED 12V CONN TO U8, REVERSED CONN. OF SW1.		JKF	
CD | 20111036	10/10/03	LRT	
ADDED J36 - J41, L54 - L56, W13 -W15, TP5, TP6, & R275, R276, R279 - R285, R225 & R229 WERE 130 OHM. U14, U18 & U22 WERE MAV-11. ADDED NOTE EXTERNAL CABLE ASSY FOR W13 & W14 CONN.		JKF	
BD | 20110968	9/3/03	LRT	
REV	ECO	DATE	APV

Axcera	REV	ECO	DATE	APV
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MATERIAL -----				
FINISH -----				

TITLE: SCH., ANALOG, IF PROCESSOR BD. (1301977)

DWN	JKF	2/24/03	
CHK	LRT	3/6/03	
REL	LRT	3/6/03	

DWG. NO. 1301983 REV F0

D SCALE --- SHEET 1 OF 2

Axcera	REV	ECO	DATE	APV

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TITLE SCH., ANALOG, IF PROCESSOR BD. (1301977)

MATERIAL -----

FINISH -----

DWN	JKF	2/24/03
CHK	LRT	3/6/03
REL	LRT	3/6/03

DWG. NO. 1301983 REV F0

D SCALE --- SHEET 2 OF 2

+7V
DS8
DS7
DS6
DS5
R1 1K 1/10W 1%
R3 1K 1/10W 1%
R5 1K 1/10W 1%
R7 1K 1/10W 1%
R9 1K 1/10W 1%
R11 1K 1/10W 1%
R13 1K 1/10W 1%
R15 1K 1/10W 1%
Q40 2N7002LT1
Q43 2N7002LT1
Q45 2N7002LT1
Q46 2N7002LT1
SPARE
V1
V2
V3
V4
V5
V6
V7
V8
S_POT_ENABLE
DATA BUS
PA_7
PA_6
PA_5
PA_4
PA_3
PA_2
PA_1
PA_0
+5V
C1 .1
ANALOG INPUTS
Ain_7
Ain_6
Ain_5
Ain_4
Ain_3
Ain_2
Ain_1
Ain_0
+5.0Vdc
L1 15906260SMT
R22 100
C8 .01
U1
1302044
PA3 PA4 PA5 PA6 PA7 ALE PC7 (A15) PC6 (A14) PC5 (A13) PC4 (A12) PC3 (A11) PC2 (A10) PC1 (A9) PC0 (A8) RD WR
PA2 PA1 PA0 Vcc GND (ADC7) PF7 (ADC6) PF6 (ADC5) PF5 (ADC4) PF4 (ADC3) PF3 (ADC2) PF2 (ADC1) PF1 (ADC0) PF0 AREF AGND AVCC
PEN PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7 PB0 PB1 PB2 PB3 PB4 PB5 PB6
PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0 XTAL1 XTAL2 GND Vcc RESET TOSC1 TOSC2 PB7
V9
V10
V11
V12
V13
Q39 2N7002LT1
Q41 2N7002LT1
Q42 2N7002LT1
Q44 2N7002LT1
R2 1K 1% 1/10W
R4 1K 1% 1/10W
R6 1K 1% 1/10W
R8 1K 1% 1/10W
R10 1K 1% 1/10W
R12 1K 1% 1/10W
R14 1K 1% 1/10W
R16 1K 1% 1/10W
DS1
DS2
DS3
DS4
+7V
R17 100
R18 100
R19 100
LCD_DATA_FLOW
LDC_E
LCD_RW
LCD_RS
UART1_TXD1
UART1_RXD1
AUTO_TEST_1
AUTO_TEST_2
R20 1M
Y1 3.6864 MHZ
C3 33 PF 50V
C5 33 PF 50V
C4 .1
C6 .1
+5V
R21 2.37K 1/10W 1%
R24 1K 1/10W 1%
R23 10K 1/10W 1%
PE_5
U2
WDS RST ST NMI PBRST Vcc GND IN
1095823
S1
MANUAL MICRO RESET
R25 100
MOD_STATION_ID_CONTROL
IF_PROCS_IF_POWER_CONTROL
UART1_RW
R26 100
R27 100
R28 100
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
PE_3
PE_4
PE_5
PE_6
PE_7
S_CLOCK
S_DATA
Q47 2N7002LT1
R29 1K 1/10W 1%
R30 1K 1/10W 1%
DS9
+7V
PROCESSOR STATUS
C9 .1
U5
IN1 OUT1 OUT2 IN2 CTRL2 CTRL3 GND VCC CTRL1 CTRL4 IN4 OUT4 OUT3 IN3
R31 10K 1/10W 1%
Q1 2N7002LT1
+5.0Vdc
PROGRAMMING ENABLED
DS10
GREEN
R32 1K 1/10W 1%
R33 1K 1/10W 1%
J4
PROGRAMMING PORT
U3
MC74HC138A
DIN_CS08
DIN_CS28
DIN_CS48
DIN_CS68
DIN_CS88
DIN_CSA8
DIN_CSC8
DIN_CSE8
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Vcc A0 A1 A2 CS1 CS2 CS3 GND
PE_5 PE_6 PE_7 PE_3 PE_4
C2 .1
U4
MC74HC138A
DOUT_CS10
DOUT_CS30
DOUT_CS50
DOUT_CS70
DOUT_CS90
DOUT_CSB0
DOUT_CSD0
DOUT_CSF0
PE_5 PE_6 PE_7 PE_4 PE_3
C7 .1
J3
120 OHM SCADA TERMINATION
OUT
IN
W1
UART1_TXD1
UART1_RXD1
UART1_RW
+5Vserial
C10 .1
R34 1K 1/10W 1%
R35 120
R36 1K 1/10W 1%
CR1 BAL99
NC
U6
2-61100-4472
SCADA_485_-
SCADA_485_+
U7
C1+ V+ C1- C2+ C2- V TR2OUT REC2IN VCC GND TR1OUT REC1IN REC1OUT TR1IN TR2IN REC2OUT
LT118ACSW
C12 .1
C13 .1
C14 .1
C15 .1
SCADA_232_A_OUT
SCADA_232_A_IN
SCADA_232_B_IN
SCADA_232_B_OUT
CR2 BAL99
CR3 BAL99
R41 1K 1/10W 1%
C11 .1
U8
2-61100-4472
R37 1K 1/10W 1%
R38 120
R39 1K 1/10W 1%
SYSTEM SERIAL -
SYSTEM SERIAL +
SW1
TRANSMITTER OPERATION SELECT
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
SYSTEM_VISUAL/AVERAGE_POWER
SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
TRANSMITTER OPERATION SELECT
BD04
J60
FRONT PANEL SWITCH BOARD
LCD_RS
LCD_RW
LDC_E
LCD_DATA_0
LCD_DATA_1
LCD_DATA_2
LCD_DATA_3
LCD_DATA_4
LCD_DATA_5
LCD_DATA_6
LCD_DATA_7
LCD_SWITCH_1
LCD_SWITCH_2
LCD_SWITCH_3
LCD_SWITCH_4
LCD_SWITCH_5
Key
SYSTEM_+12V_C3
FRONT PANEL LCD CONTRAST
CW
5K
R40
TP11
J44A
REAR BACKPLANE CONNECTOR
RMT_INTERLOCK_ISO_RETURN
SYSTEM_+12V_C3
SYSTEM_-12V_C2
SYSTEM_-12V_C1
SYSTEM_+12V_C6
SYSTEM_+12V_C5
SYSTEM_+12V_C4
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
RMT_AUX_I/O_1
RMT_RF_SYSTEM_INTERLOCK
RMT_OPERATE_COMMAND
RMT_STANDBY_COMMAND
RMT_POWER_RAISE
RMT_POWER_LOWER
RMT_SYSTEM_REFLECTED_POWER
RMT_SYSTEM_VISUAL/AVERAGE_POWER
RMT_SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
SYSTEM_VISUAL/AVERAGE_POWER
SYSTEM_AURAL_POWER
UC_PLL_LOCK_INDICATOR
UC_AFC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
UC_INTERLOCK
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
UC_EXTERNAL_REF_INDICATOR
913289
J44B
SYSTEM SERIAL -
SYSTEM_+12V_C3
SYSTEM_-12V_C2
SYSTEM_-12V_C1
SYSTEM_+12V_C6
SYSTEM_+12V_C5
SYSTEM_+12V_C4
SPARE_DIN_1
SPARE_DIN_2
SPARE_DIN_3
SPARE_DIN_4
SPARE_DIN_5
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SPARE_DOUT_1
SPARE_DOUT_2
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
AUTO_TEST_1
AUTO_TEST_2
SCADA_232_B_IN
SCADA_232_A_IN
SCADA_485_-
913289
J44C
SYSTEM SERIAL +
SYSTEM_+12V_C3
SYSTEM_-12V_C2
SYSTEM_-12V_C1
SYSTEM_+12V_C6
SYSTEM_+12V_C5
SYSTEM_+12V_C4
MOD_EXTERNAL_CW_PRESENT
MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
MOD_PLL_UNLOCKED
MOD_INTERLOCK
MOD_STATION_ID_CONTROL
IF_PROCS_ALC_AUTO_MANUAL_SW
IF_PROCS_MODULATION_PRESENT
IF_PROCS_INPUT_FAULT
IF_PROCS_SELECTED_IF_SOURCE
IF_PROCS_MUTE_COMMAND
IF_PROCS_ALC_VOLTAGE
IF_PROCS_INTERLOCK
IF_PROCS_BOARD_TYPE
IF_PROCS_IF_POWER_CONTROL
IF_PROCS_DLC_VOLTAGE
SCADA_232_B_OUT
SCADA_232_A_OUT
SCADA_485_+
913289
J61
POWER SUPPLY / POWER AMP
SYSTEM_-12V_C2
SYSTEM_+12V_C3
SYSTEM SERIAL +
SYSTEM SERIAL -
PA_INTERLOCK
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
UC_AGC_#1_VOLTAGE
PS_AC_OK
PS_ENABLE
PS_DC_OK
SYSTEM_+12V_C3
TP1
-12V
TP2
L2 15906260SMT
SYSTEM_-12V_C1
+7V
TP3
+5V
TP4
+5.0Vdc
TP5
+5Vserial
TP6
TP7
TP8
TP9
TP10
NET LABEL WAS RMT AUX I/O 2 FOR J44-12A & CR5 PIN 2 (PG 2) CONN. JKF
C0 20111235 3/3/04 JCM
ADDED C46 - C49, Q39 - Q47. R149 - R152, R162, R164, R166 & R167 WERE 20K. ALL +12V CHGD TO SYSTEM_+12V_C3. JKF
B0 20111032 10/2/03 REH
MATERIAL NUMBERS:
1302021 A/D, PIONEER, AMP CTRL
1302022 PCB, PIONEER, AMP CTRL
1302023 SCH, PIONEER, AMP CTRL
1302024 STENCIL FOR 1302022
Axcera
REV ECO DATE APV
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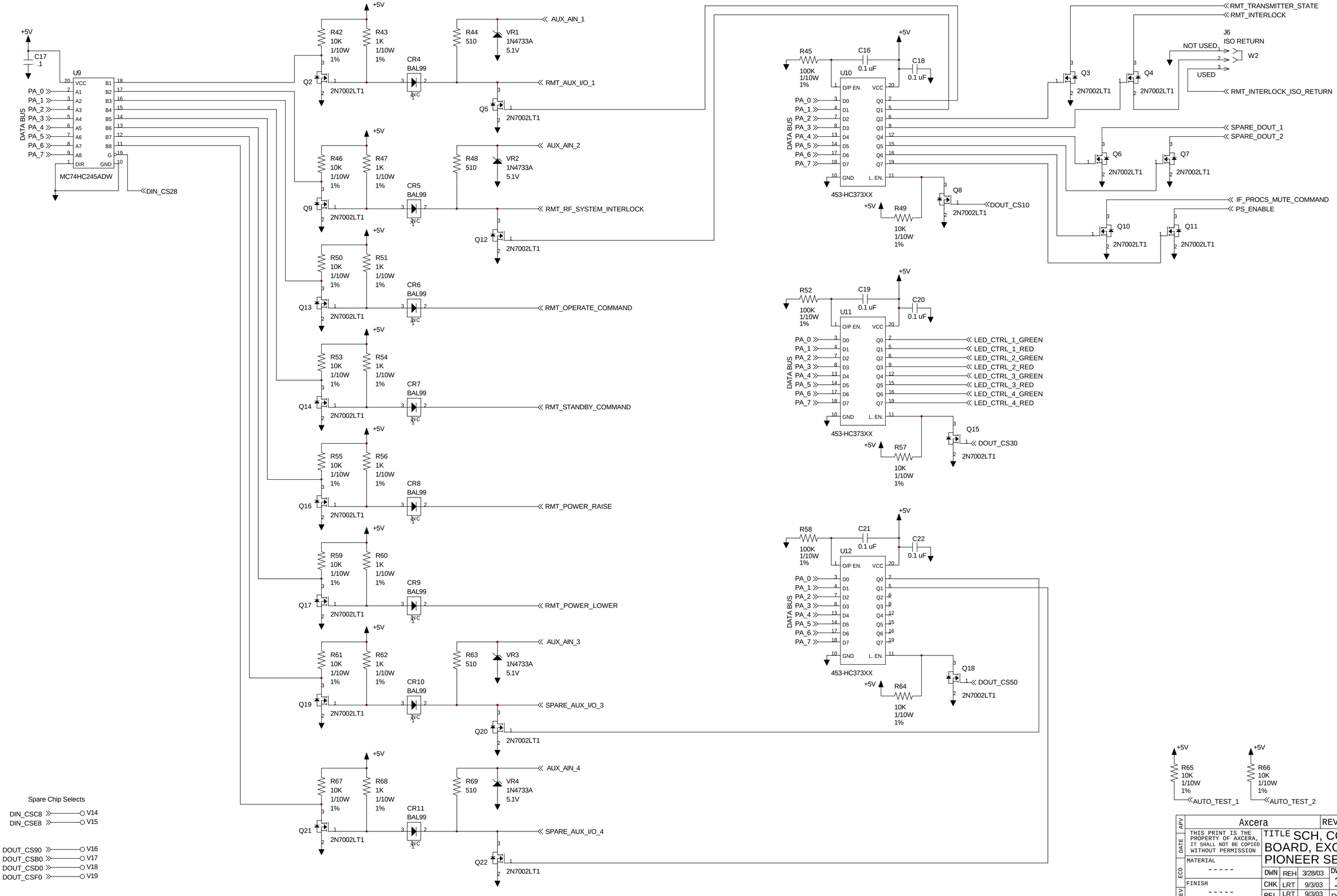
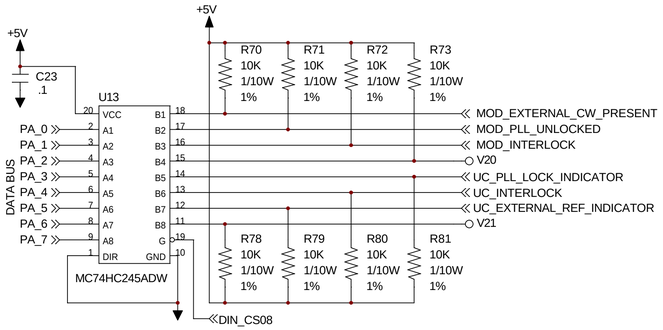
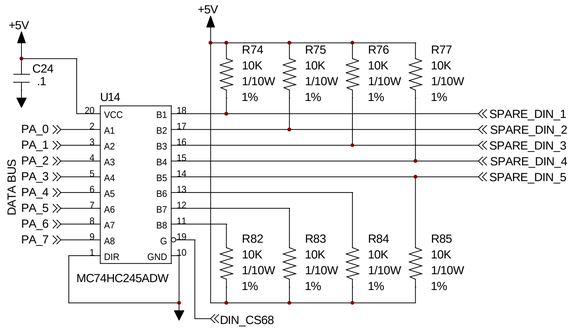
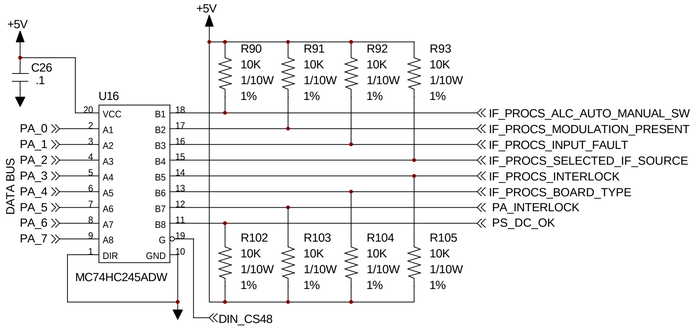
MATERIAL -----
FINISH -----
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWN REH 3/28/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1302023
REV C0
D
SCALE - - -
SHEET 1 OF 5

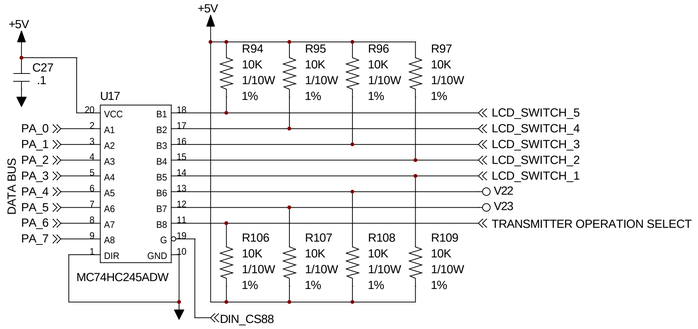


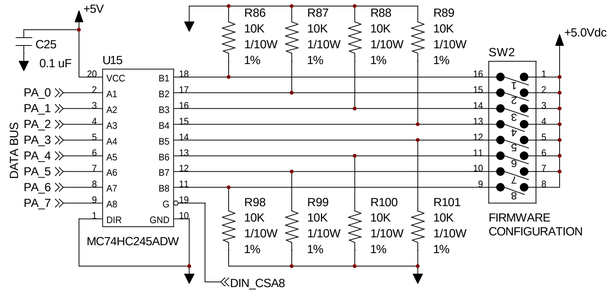
APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL -----	DWN	REH	3/28/03	DWG. NO. 1302023 REV C0
REV	FINISH -----	CHK	LRT	9/3/03	
		REL	LRT	9/3/03	D SCALE - - - SHEET 2 OF 5



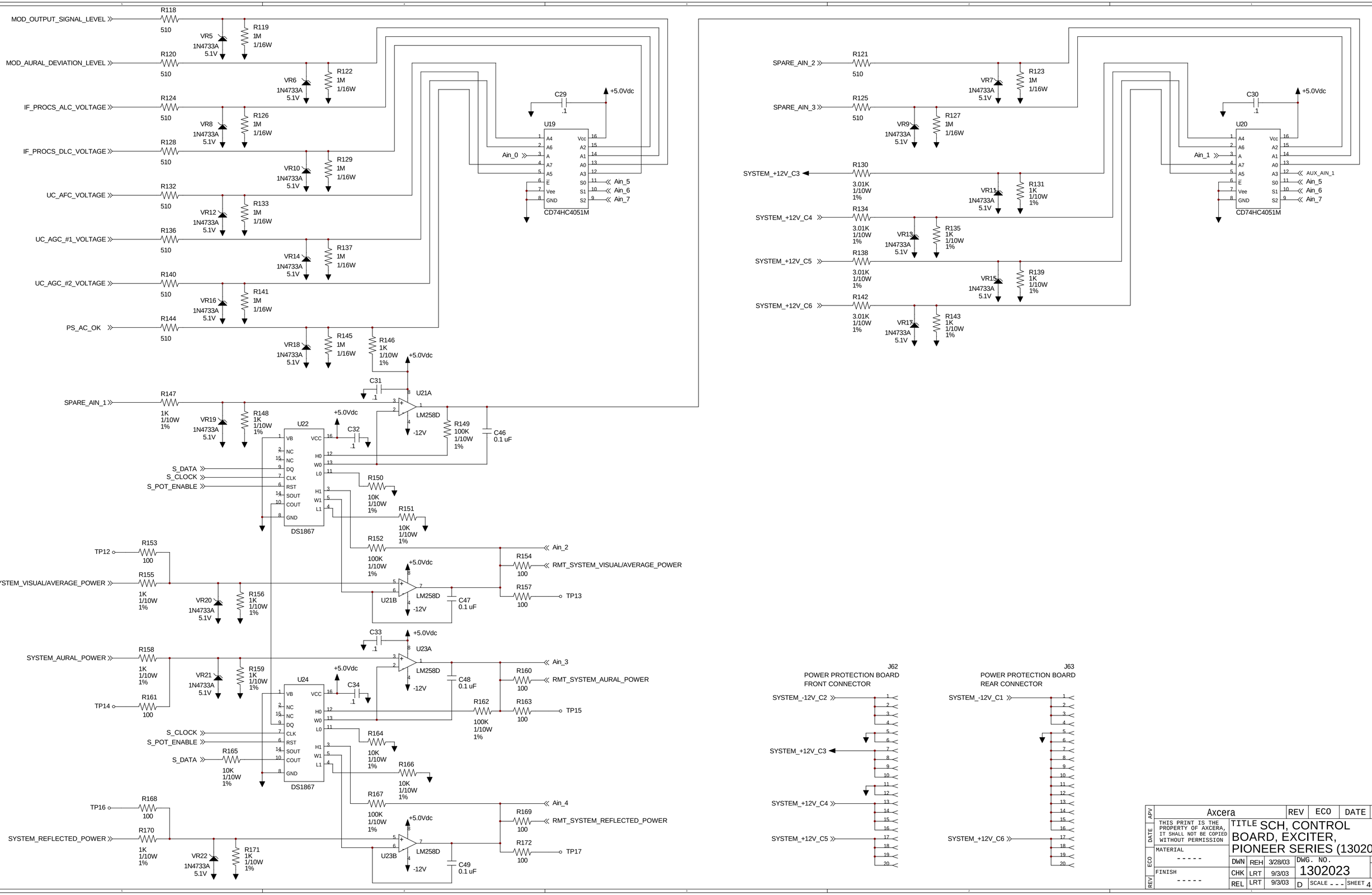






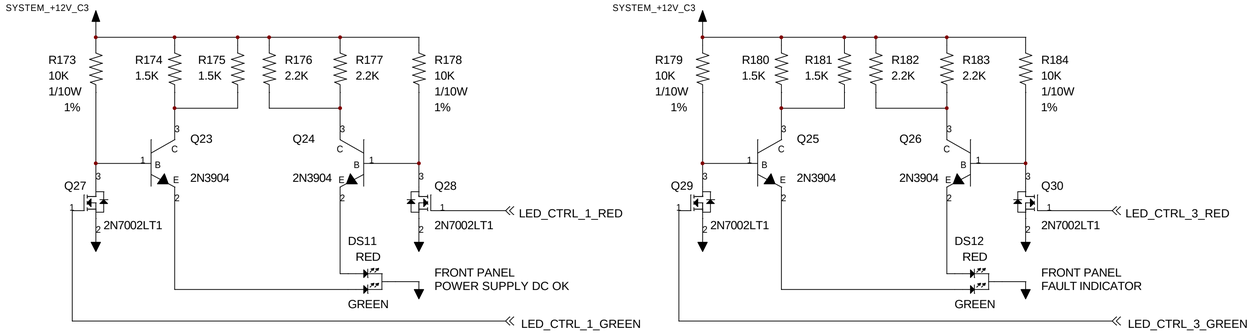


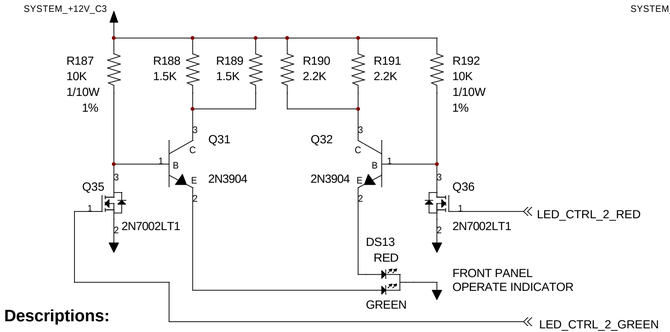
APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023	REV C0	
REV	FINISH -----	CHK LRT 9/3/03			
		REL LRT 9/3/03	D	SCALE - - -	SHEET 3 OF 5

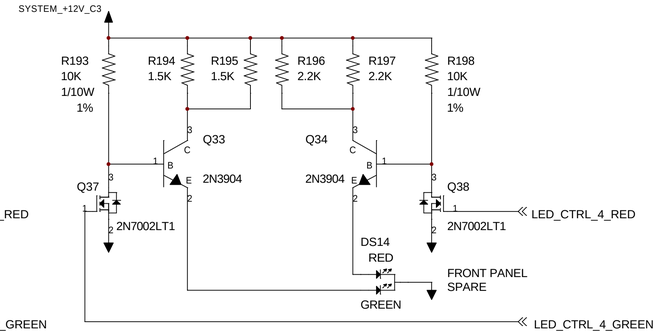

MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
IF_PROCS_ALC_VOLTAGE
IF_PROCS_DLC_VOLTAGE
UC_AFC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
PS_AC_OK
SPARE_AIN_1
R118 510
R119 1M 1/16W
R120 510
R122 1M 1/16W
R124 510
R126 1M 1/16W
R128 510
R129 1M 1/16W
R132 510
R133 1M 1/16W
R136 510
R137 1M 1/16W
R140 510
R141 1M 1/16W
R144 510
R145 1M 1/16W
R146 1K 1/10W 1%
R147 1K 1/10W 1%
R148 1K 1/10W 1%
VR5 1N4733A 5.1V
VR6 1N4733A 5.1V
VR8 1N4733A 5.1V
VR10 1N4733A 5.1V
VR12 1N4733A 5.1V
VR14 1N4733A 5.1V
VR16 1N4733A 5.1V
VR18 1N4733A 5.1V
VR19 1N4733A 5.1V
C29 .1
+5.0Vdc
U19
CD74HC4051M
Ain_0
Ain_5
Ain_6
Ain_7
C31 .1
U21A
LM258D
-12V
R149 100K 1/10W 1%
C46 0.1 uF
U22
DS1867
S_DATA
S_CLOCK
S_POT_ENABLE
C32 .1
R150 10K 1/10W 1%
R151 10K 1/10W 1%
R152 100K 1/10W 1%
TP12
TP13
TP14
TP15
TP16
TP17
R153 100
R154 100
R155 1K 1/10W 1%
R156 1K 1/10W 1%
R157 100
SYSTEM_VISUAL/AVERAGE_POWER
RMT_SYSTEM_VISUAL/AVERAGE_POWER
VR20 1N4733A 5.1V
U21B
C47 0.1 uF
Ain_2
C33 .1
U23A
C48 0.1 uF
SYSTEM_AURAL_POWER
R158 1K 1/10W 1%
R159 1K 1/10W 1%
R160 100
R161 100
R162 100K 1/10W 1%
R163 100
RMT_SYSTEM_AURAL_POWER
VR21 1N4733A 5.1V
U24
C34 .1
Ain_3
R164 10K 1/10W 1%
R165 10K 1/10W 1%
R166 10K 1/10W 1%
R167 100K 1/10W 1%
R168 100
R169 100
R170 1K 1/10W 1%
R171 1K 1/10W 1%
R172 100
SYSTEM_REFLECTED_POWER
RMT_SYSTEM_REFLECTED_POWER
VR22 1N4733A 5.1V
U23B
C49 0.1 uF
Ain_4
SPARE_AIN_2
SPARE_AIN_3
R121 510
R123 1M 1/16W
R125 510
R127 1M 1/16W
VR7 1N4733A 5.1V
VR9 1N4733A 5.1V
C30 .1
U20
AUX_AIN_1
Ain_1
SYSTEM_+12V_C3
SYSTEM_+12V_C4
SYSTEM_+12V_C5
SYSTEM_+12V_C6
R130 3.01K 1/10W 1%
R131 1K 1/10W 1%
R134 3.01K 1/10W 1%
R135 1K 1/10W 1%
R138 3.01K 1/10W 1%
R139 1K 1/10W 1%
R142 3.01K 1/10W 1%
R143 1K 1/10W 1%
VR11 1N4733A 5.1V
VR13 1N4733A 5.1V
VR15 1N4733A 5.1V
VR17 1N4733A 5.1V
J62
POWER PROTECTION BOARD
FRONT CONNECTOR
J63
POWER PROTECTION BOARD
REAR CONNECTOR
SYSTEM_-12V_C2
SYSTEM_-12V_C1
Axcera
REV
ECO
DATE
APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
MATERIAL
FINISH
DWN REH 3/28/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1302023
REV C0
D
SCALE - - -
SHEET 4 OF 5

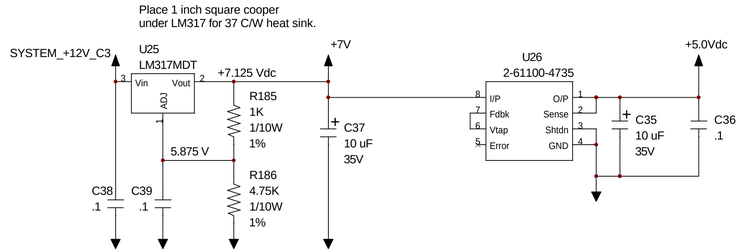
LAST USED REF.

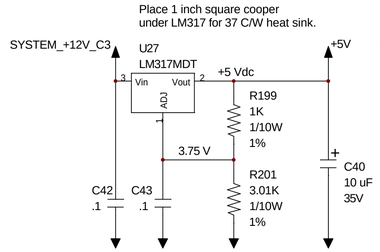
R202
C49
Q47
DS14
U28
VR22
J63
TP17
V23
SW2
CR11
W2
Y1
L2
S1

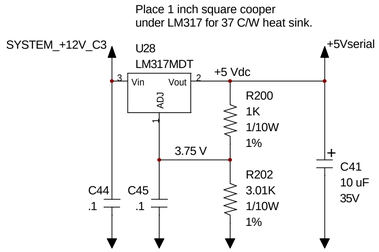












Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N= 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

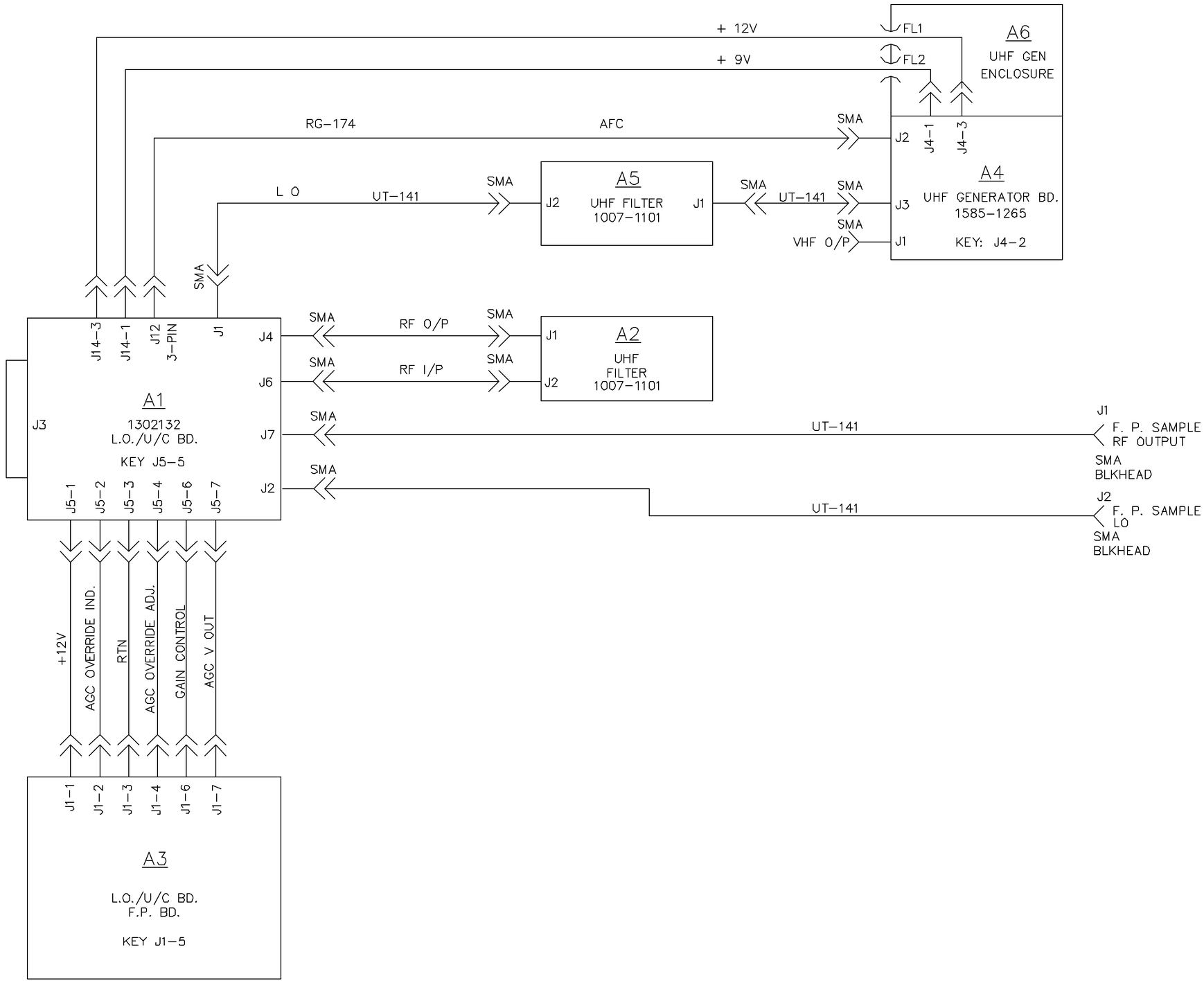
Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C.
They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023	REV C0	
REV	FINISH -----	CHK LRT 9/3/03			
		REL LRT 9/3/03	D	SCALE ---	SHEET 5 OF 5



NOTES:

1) ALL WIRES 22AWG UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV

Axcera

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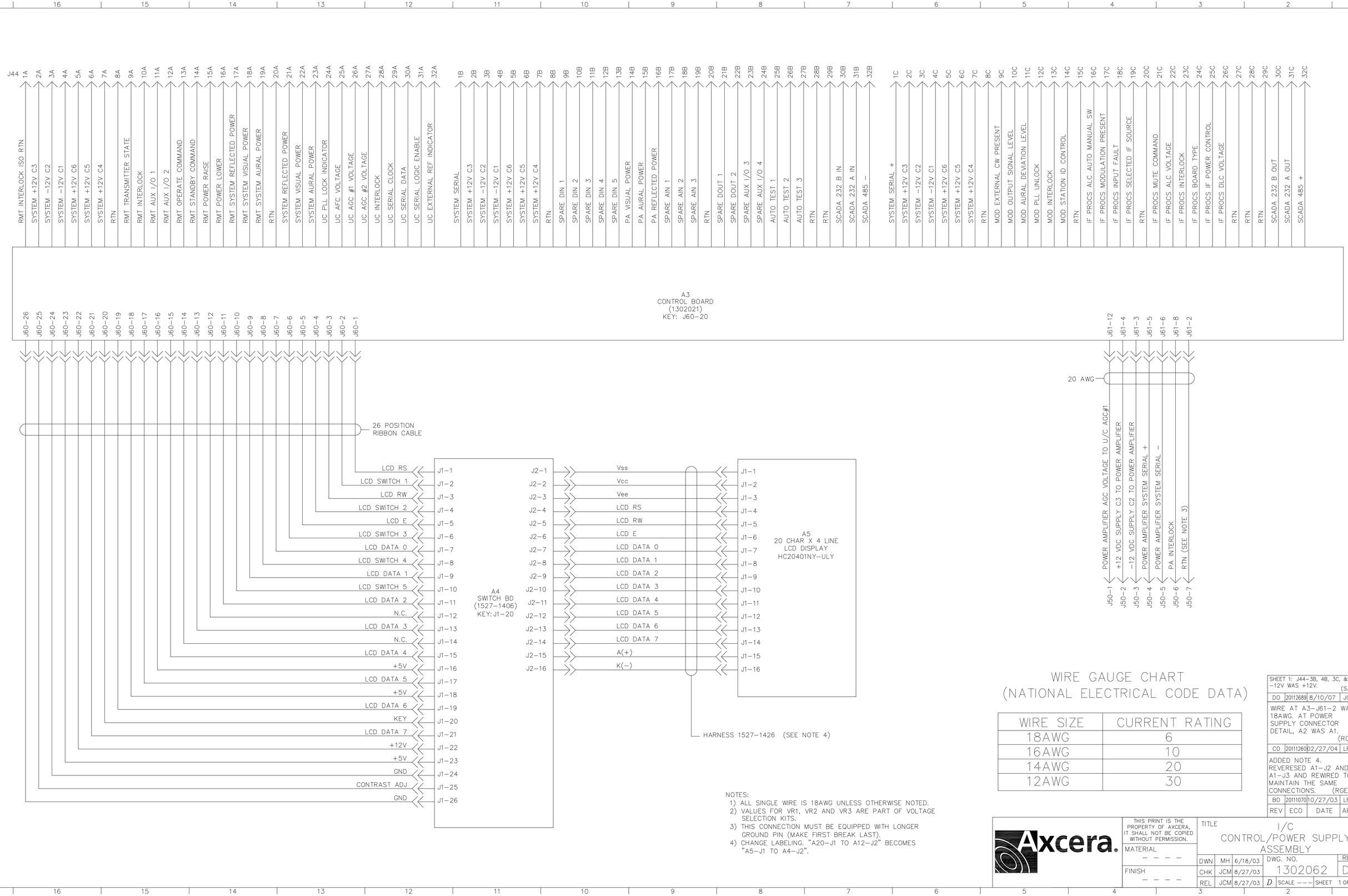
MATERIAL — — — —

FINISH — — — —

TITLE: I/C, L.O./ U/C ASSY, UHF LOW PHASE NOISE

DWN	MH	6/11/03	DWG. NO. 1302060	REV A0
CHK	LRT	6/12/03		
REL	LRT	6/12/03	C SCALE ---	SHEET 1 OF 1



WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

NOTES:
1) ALL SINGLE WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2) VALUES FOR VR1, VR2 AND VR3 ARE PART OF VOLTAGE SELECTION KITS.
3) THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN (MAKE FIRST BREAK LAST).
4) CHANGE LABELING. "A20–J1 TO A12–J2" BECOMES "A5–J1 TO A4–J2".

REV	ECO	DATE	APV
D0	20112689	8/10/07	JCM

SHEET 1: J44–3B, 4B, 3C, & 4C, –12V WAS +12V. (SAK)

REV	ECO	DATE	APV
C0	20111260	02/27/04	LRT

WIRE AT A3–J61–2 WAS 18AWG. AT POWER SUPPLY CONNECTOR DETAIL, A2 WAS A1. (RGE)

REV	ECO	DATE	APV
B0	20111070	10/27/03	LRT

ADDED NOTE 4. REVERESED A1–J2 AND A1–J3 AND REWIRED TO MAINTAIN THE SAME CONNECTIONS. (RGE)

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MATERIAL – – – –

FINISH – – – –

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	DWG. NO. 1302062 REV D0
CHK	JCM	8/27/03	
REL	JCM	8/27/03	D SCALE – – – SHEET 1 OF 2

A3
CONTROL BOARD
1302021

J62-1 J62-2 J62-3 J62-4 J62-5 J62-6 J62-7 J62-8 J62-9 J62-10 J62-11 J62-12 J62-13 J62-14 J62-15 J62-16 J62-17 J62-18 J62-19 J62-20

-12VDC (REM)
-12VDC (REM)
-12VDC (REM)
-12VDC (REM)
RTN
RTN
+12VDC (SYS CTRLR/AMP CTRLR/SPARE SLOT)
+12VDC (SYS CTRLR/AMP CTRLR/SPARE SLOT)
+12VDC (SYS CTRLR/AMP CTRLR/SPARE SLOT)
+12VDC (SYS CTRLR/AMP CTRLR/SPARE SLOT)
RTN
RTN
+12VDC (MOD.IF)
+12VDC (MOD.IF)
+12VDC (MOD.IF)
+12VDC (U/C)
+12VDC (U/C)
+12VDC (U/C)
+12VDC (U/C)

J63-1 J63-2 J63-3 J63-4 J63-5 J63-6 J63-7 J63-8 J63-9 J63-10 J63-11 J63-12 J63-13 J63-14 J63-15 J63-16 J63-17 J63-18 J63-19 J63-20

-12VDC (SYS)
-12VDC (SYS)
-12VDC (SYS)
-12VDC (SYS)
RTN
RTN
RTN
RTN
RTN
RTN
RTN
RTN
RTN
RTN
RTN
+12VDC (REM)
+12VDC (REM)
+12VDC (REM)
+12VDC (REM)

J61-16 J61-13 J61-14 J61-7 J61-15 J61-1

PS DC OK
PS DC OK RTN
PS AC OK
PS AC OK RTN
PS ENABLE
PS ENABLE RTN

22AWG

A1
POWER PROTECTION
BOARD
(1302837)

J1-4 J1-3 J1-2 J1-1 V1-6 V1-7

A2
600W SWITCHING
POWER SUPPLY

J1-1 J1-2 J1-3 J1-4 J1-5

16AWG

LINE#1
EARTH GROUND
LINE#2 (220VAC) OR NEUTRAL (110VAC)
AC LINE#1 (FAN)
AC LINE#2 (FAN)

J50-10 J50-8 J50-9 J50-11 J50-12

SEE NOTE 2
ON SHEET 1

J2 J3 J4 J5 J6 J7

VR3 VR2 VR1

16AWG

RTN (±12VDC)
+12VDC
-12VDC

16AWG

CHASSIS GND

V1-(-)1 V1-(-)2 V1-(+)1 V1-(+)2 V2-(-) V2-(+) V3-(-) V3-(+) V2/V3-9 V2/V3-10 V2/V3-1 V2/V3-4 V1-1 V1-4

22AWG

AC I/P-L AC I/P-N AC I/P-G

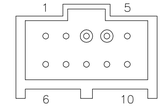
AC LINE#1
AC LINE#2
EARTH GND

+32VDC → J50-A

RTN (+32VDC) → J50-B

12AWG

A2-J1
(BELOW AC INPUT)



POWER SUPPLY FRONT VIEW

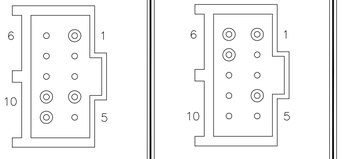
A2-V2/V3

A2-V2-(+)
A2-V2-(-)
A2-V3-(+)
A2-V3-(-)

A2-V1

A2-V1-(+)1 A2-V1-(+)2

A2-V1-(-)1 A2-V1-(-)2



POWER SUPPLY REAR VIEW

REV	ECO	DATE	APV

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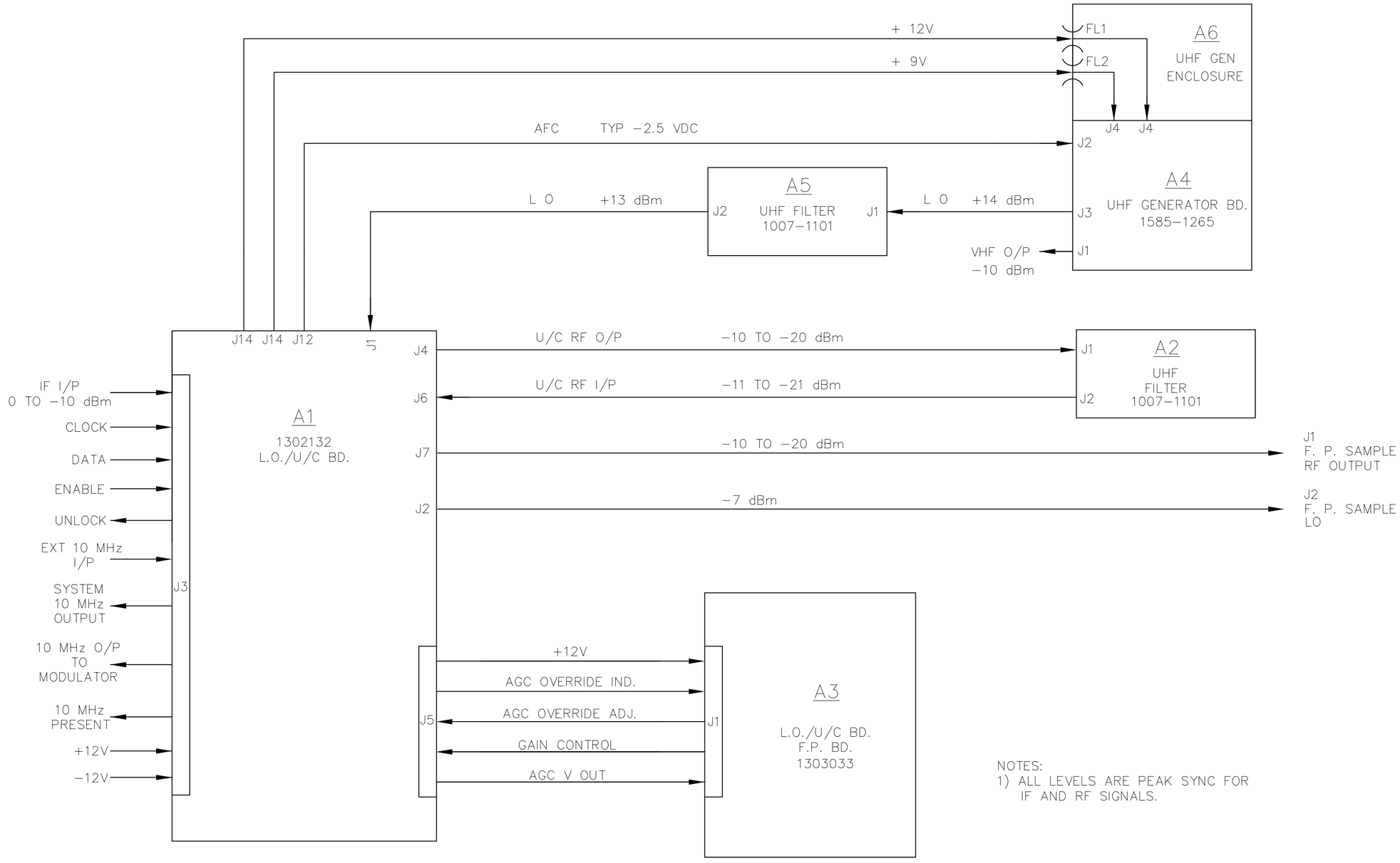
MATERIAL — — — —

FINISH — — — —

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

			DWG. NO.	REV
DWN	MH	6/18/03	1302062	D0
CHK	JCM	8/27/03		
REL	JCM	8/27/03	D SCALE — — —	SHEET 2 OF 2



NOTES:
1) ALL LEVELS ARE PEAK SYNC FOR IF AND RF SIGNALS.

REV	ECO	DATE	APV

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MATERIAL — — — —

FINISH — — — —

TITLE: B/D, L.O./ U/C ASSY, UHF LOW PHASE NOISE

DWN	RGE	1/9/04	DWG. NO. 1302107	REV A0
CHK	LRT	01/09/04		
REL	LRT	01/09/04	C SCALE — — —	SHEET 1 OF 1

LAST USED REF.

C89
CR13
DS2
J14 + J43
K1
L16
Q8
R111
T2
TP7
U14
W3
Z1

NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

C35 WAS .01, R42 & R44 WERE 47, R20 & R21 WERE NOT USED, R18 WAS 0. JKF

C0	20111040	10/20/03	LRT

R42 WAS 220, R109 & R110 WERE 2K, R49 WAS 10K, C38 WAS 4.7, ADDED R112. PINS U4-2 & -3 TO GND. PIN U4-1 NO CONN. DEL. C36 & C45. JKF

B0	20111055		

APV	Axcera	REV	ECO	DATE	APV

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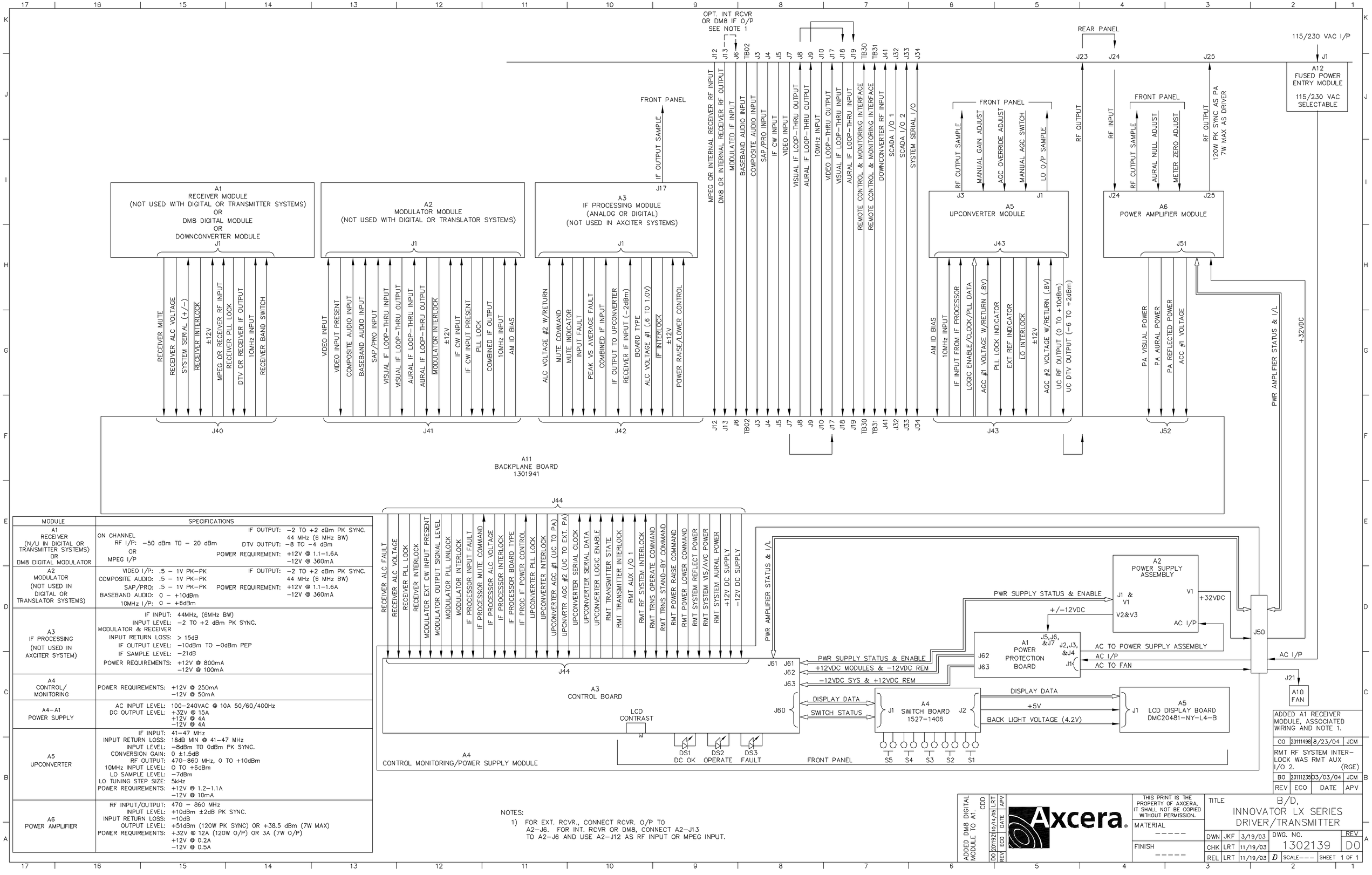
MATERIAL: -----

FINISH: -----

TITLE: SCH., L.O./ UPCONVERTER BD., UHF, LPN. (1302132)

DWN	JKF	3/25/03	DWG. NO. 1302134 REV C0
CHK	LRT	9/3/03	
REL	LRT	9/3/03	D SCALE - - - SHEET 1 OF 1



MODULE	SPECIFICATIONS
A1 RECEIVER (N/U IN DIGITAL OR TRANSMITTER SYSTEMS) OR DM8 DIGITAL MODULATOR	ON CHANNEL RF I/P: −50 dBm TO − 20 dBm OR MPEG I/P IF OUTPUT: −2 TO +2 dBm PK SYNC. 44 MHz (6 MHz BW) DTV OUTPUT: −8 TO −4 dBm POWER REQUIREMENT: +12V @ 1.1−1.6A −12V @ 360mA
A2 MODULATOR (NOT USED IN DIGITAL OR TRANSLATOR SYSTEMS)	VIDEO I/P: .5 − 1V PK−PK COMPOSITE AUDIO: .5 − 1V PK−PK SAP/PRO: .5 − 1V PK−PK BASEBAND AUDIO: 0 − +10dBm 10MHz I/P: 0 − +6dBm IF OUTPUT: −2 TO +2 dBm PK SYNC. 44 MHz (6 MHz BW) POWER REQUIREMENT: +12V @ 1.1−1.6A −12V @ 360mA
A3 IF PROCESSING (NOT USED IN AXCITER SYSTEM)	IF INPUT: 44MHz, (6MHz BW) INPUT LEVEL: −2 TO +2 dBm PK SYNC. MODULATOR & RECEIVER INPUT RETURN LOSS: > 15dB IF OUTPUT LEVEL: −10dBm TO −0dBm PEP IF SAMPLE LEVEL: −21dB POWER REQUIREMENTS: +12V @ 800mA −12V @ 100mA
A4 CONTROL/ MONITORING	POWER REQUIREMENTS: +12V @ 250mA −12V @ 50mA
A4−A1 POWER SUPPLY	AC INPUT LEVEL: 100−240VAC @ 10A 50/60/400Hz DC OUTPUT LEVEL: +32V @ 15A +12V @ 4A −12V @ 4A
A5 UPCONVERTER	IF INPUT: 41−47 MHz INPUT RETURN LOSS: 18dB MIN @ 41−47 MHz INPUT LEVEL: −8dBm TO 0dBm PK SYNC. CONVERSION GAIN: 0 ±1.5dB RF OUTPUT: 470−860 MHz, 0 TO +10dBm 10MHz INPUT LEVEL: 0 TO +6dBm LO SAMPLE LEVEL: −7dBm LO TUNING STEP SIZE: 5kHz POWER REQUIREMENTS: +12V @ 1.2−1.1A −12V @ 10mA
A6 POWER AMPLIFIER	RF INPUT/OUTPUT: 470 − 860 MHz INPUT LEVEL: +10dBm ±2dB PK SYNC. INPUT RETURN LOSS: −10dB OUTPUT LEVEL: +51dBm (120W PK SYNC) OR +38.5 dBm (7W MAX) POWER REQUIREMENTS: +32V @ 12A (120W O/P) OR 3A (7W O/P) +12V @ 0.2A −12V @ 0.5A

NOTES:

1) FOR EXT. RCVR., CONNECT RCVR. O/P TO A2−J6. FOR INT. RCVR OR DM8, CONNECT A2−J13 TO A2−J6 AND USE A2−J12 AS RF INPUT OR MPEG INPUT.

REV	ECO	DATE	APV
CO	20111498	8/23/04	JCM

ADDED A1 RECEIVER MODULE, ASSOCIATED WIRING AND NOTE 1.

REV	ECO	DATE	APV
B0	20111235	03/03/04	JCM

RMT RF SYSTEM INTER−LOCK WAS RMT AUX I/O 2. (RGE)

REV	ECO	DATE	APV
D0	20111921	10/14/03	LRT

ADDED DM8 DIGITAL MODULE TO A1. CDD

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MATERIAL −−−−−

FINISH −−−−−

TITLE B/D, INNOVATOR LX SERIES DRIVER/TRANSMITTER

DWN	JKF	3/19/03	
CHK	LRT	11/19/03	
REL	LRT	11/19/03	

DWG. NO. 1302139 REV D0

D SCALE−−− SHEET 1 OF 1

LAST USED REF.

C64
CR4
R28
L24
J6
Q8
U4
RC4

J3
EXTERNAL I/P

U3
1084607

C14 100 pF
R10 100 1/10W 1%
L3 22 nH
C16 100 pF
L4 22 nH
R13 10 1/10W 1%
Q4 FP2189
L5 1.8 nH
L6 3.3 nH
L7 4.7 nH
C17 100 pF
C18 100 pF
L8 7.5 nH
L9 5.6 nH
L10 4.3 nH
C19 2 pF
C20 1 pF
L21 22 nH
C21 1.5 pF
C22 1.8 pF
C23 1.8 pF
C24 0.4 pF
C25 2.2 pF
C26 1.2 pF
C27 1.8 pF
C28 3.9 pF
L22 22 nH
C29 3.3 pF
C30 2.7 pF
R27 100 1/10W 1%
C62 100 pF
C63 100 pF
R28 100 1/10W 1%
L24 22 nH
C61 100 pF
C64 100 pF
L23 22 nH
R11 100 3/4W
R12 100 3/4W
U2
1084607
J4
EXTERNAL O/P
R14 100 3/4W
R15 100 3/4W
C32 100 pF
L14 7.5 nH
L15 5.6 nH
L16 4.3 nH
C33 2 pF
C34 1 pF
L17 22 nH
L12 3.3 nH
C35 1.5 pF
C36 1.8 pF
L13 4.7 nH
C37 1.8 pF
C38 0.4 pF
C31 100 pF
C39 2.2 pF
C40 1.2 pF
C41 1.8 pF
C42 3.9 pF
C43 3.3 pF
C44 2.7 pF
R16 10 1/10W 1%
Q5 FP2189
L11 1.8 nH
L18 22 nH
C45 100 pF
C46 .001
C49 .01
R17 100 1/10W 1%
C47 100 pF
C48 .001
C50 .01
RC3 47 - 100pF
RC4 100pF - 47
R18 47
Q6 2N3906
R19 47K 1/16W
C54 .01
R20 470
Q7 2N3906
C56 .01
C55 .01
R22 1 1/4W
R23 47K 1/16W
C57 4.7
Q8 2N3906
R24 1.21K 1/10W 1%
R25 61.9 1/10W 1%
C59 4.7
J6 -12V
L19 FERRITE BEAD
C60 10uF 50V
L20 FERRITE BEAD
+8.25V
C52 4.7
R21 255
CR4 LL4448
R26 1.5K
CR3 LL4448
U4 LM317T
O IN ADJ
C58 10 35V
C51 .01
C53 220 35V
J5 +12V

C25, C26, C39 & C40 WERE 0.2pF. C27, C28, C41 & C42 WERE 0.9pF. C29 & C43 WERE 1.8pF. C30 & C44 WERE NOT USED. C17, C19, C31 & C33 WERE 1pF. C20 & C34 WERE 0.8pF. C22 & C36 WERE 1.5pF. C23 & C37 WERE 4.7pF. L3, L18, L22 & L24 WERE 27nH. L8, L9, L14 & L15 WERE 1.8nH.L7, L13, L6 & L12 WERE 4.3nH. L4, L17, L21 & L23 WERE 33nH. L5 & L11 WERE 1.6nH. L10 & L16 WERE 3.9nH. R21 WAS 220. R24 WAS 3.9K. R25 WAS 130.
JKF

	REV	ECO	DATE	APV
	B0	20111098	11/3/03	DU

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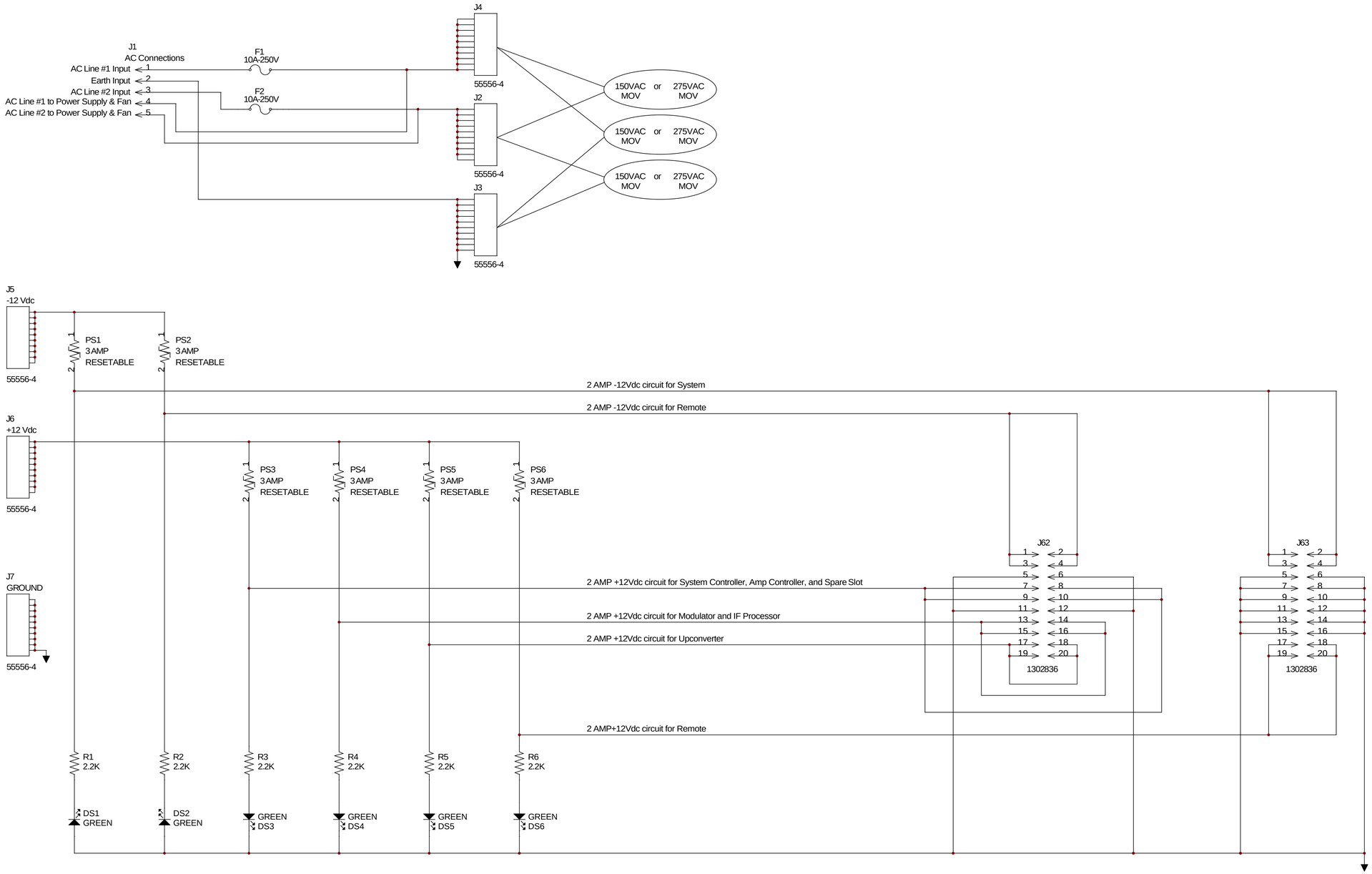
TITLE: SCH., 1 WATT UHF AMPLIFIER (1302761)

MATERIAL: -----

FINISH: -----

			DWG. NO.	REV
DWN	JKF	5/12/03	1302762	B0
CHK	LRT	9/3/03		
REL	LRT	9/3/03	SCALE ---	SHEET 1 OF 1

D



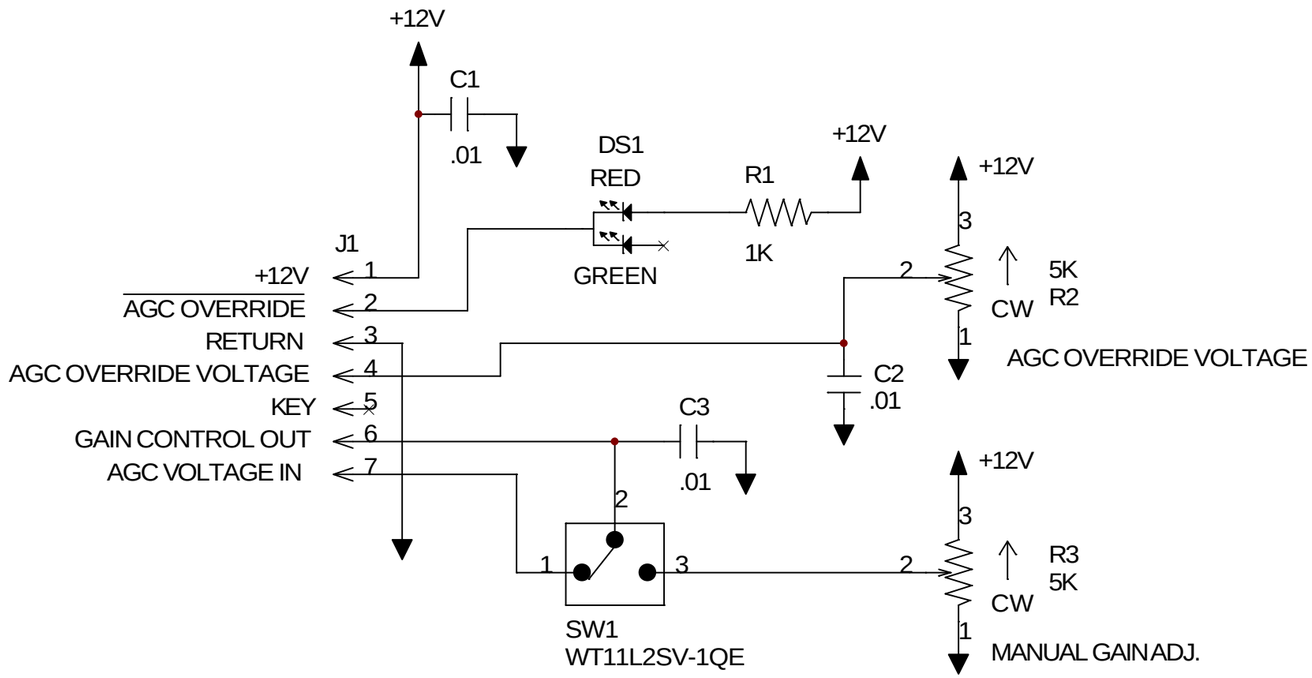
Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.065 inch minimum shall be used to connections to J62 and J63.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

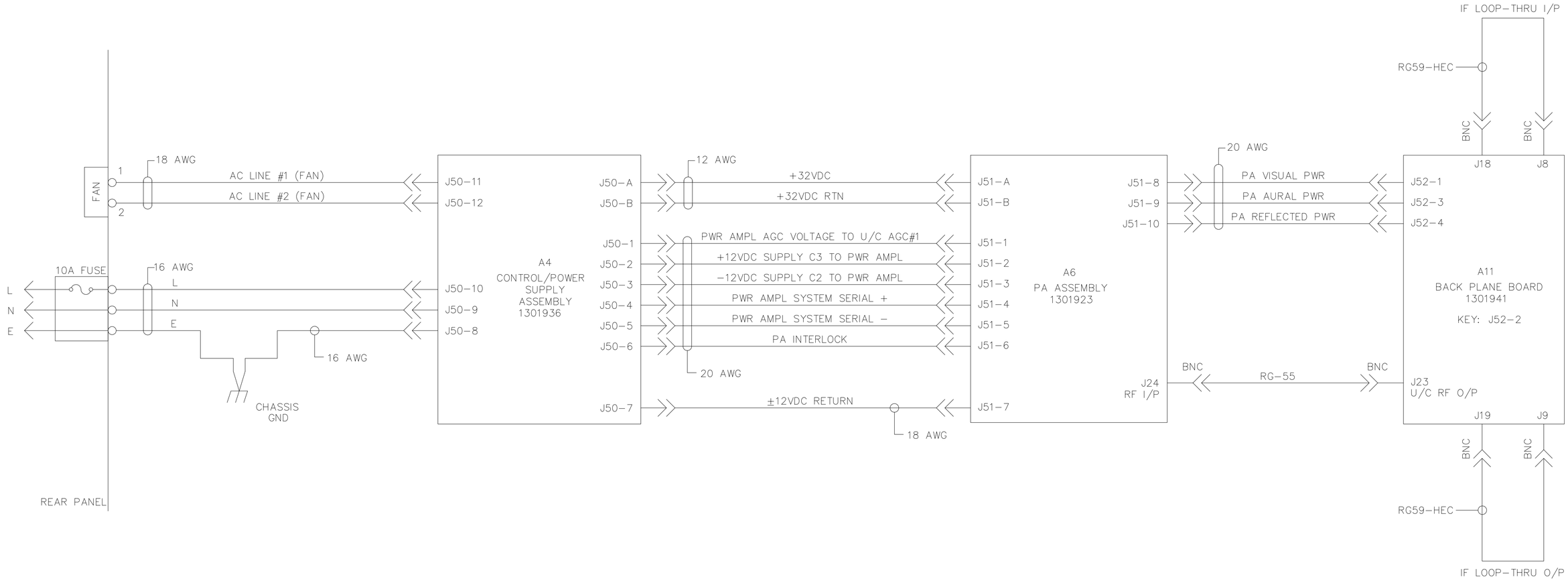
Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, PWR PROTECT (1302837)			
ECO	MATERIAL -----	DWN REH 5/29/03	DWG. NO. 1302839		REV AO
	FINISH -----	CHK REH 5/29/03			
REV		REL REH 5/29/03	D	SCALE - - -	SHEET 1 OF 1



APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., FRONT PANEL LED DISPLAY BOARD (1303033)		
ECO	MATERIAL -----	DWN	JKF	7/24/03	DWG. NO. 1303035 / REV A0
REV	FINISH -----	CHK	LRT	7/25/03	
		REL	LRT	7/25/03	B / SCALE - - - / SHEET 1 OF 1



REV	ECO	DATE	APV
B0	20111072	10/23/03	JCM

ADDED COAX CONNECTIONS AT A11. (RGE)

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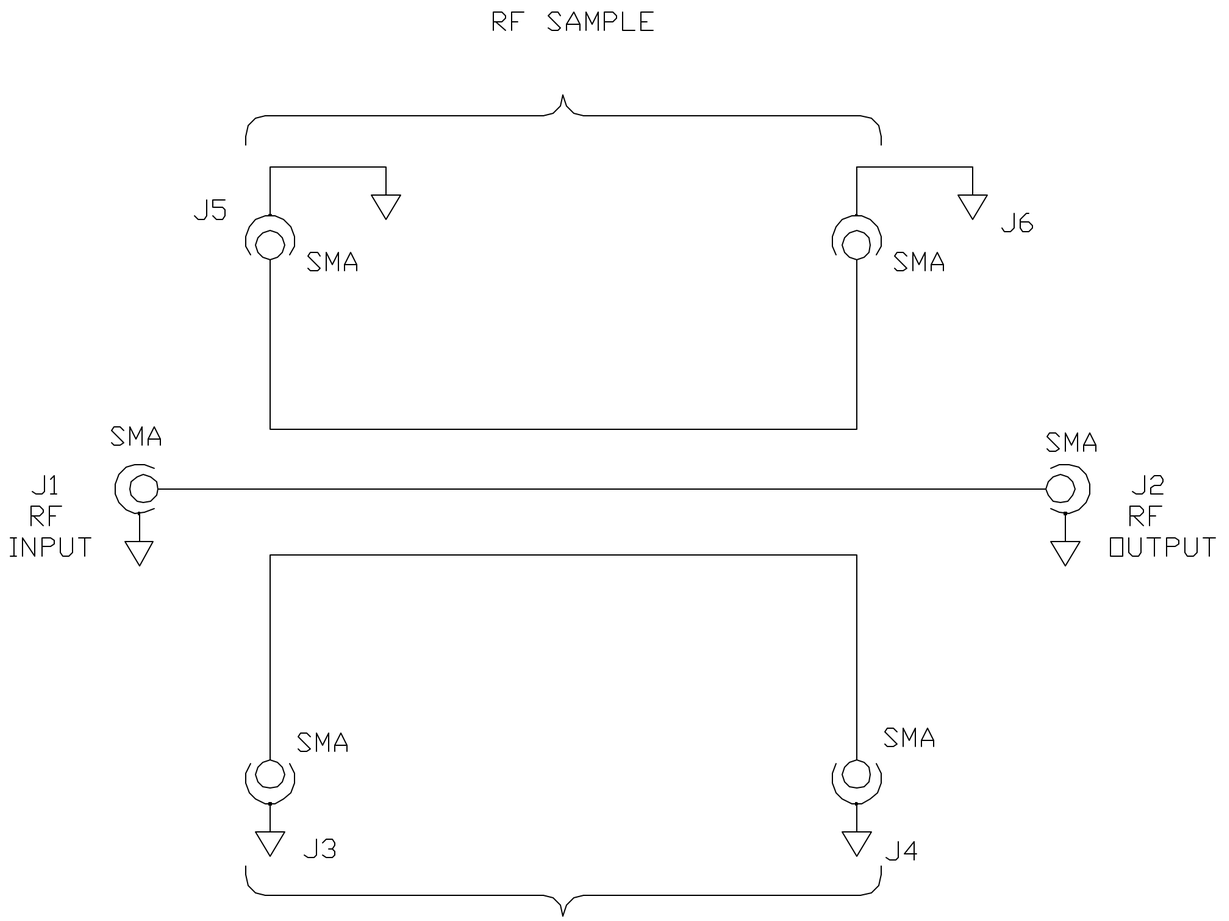
MATERIAL: ------

FINISH: ------

TITLE: I/C, CHASSIS ASSEMBLY PIONEER SERIES

DWN	MH	7/29/03	DWG. NO. 1303108
CHK	JCM	8/27/03	REV B0
REL	JCM	8/27/03	D SCALE --- SHEET 1 OF 1



REV	ECO	DATE	APV

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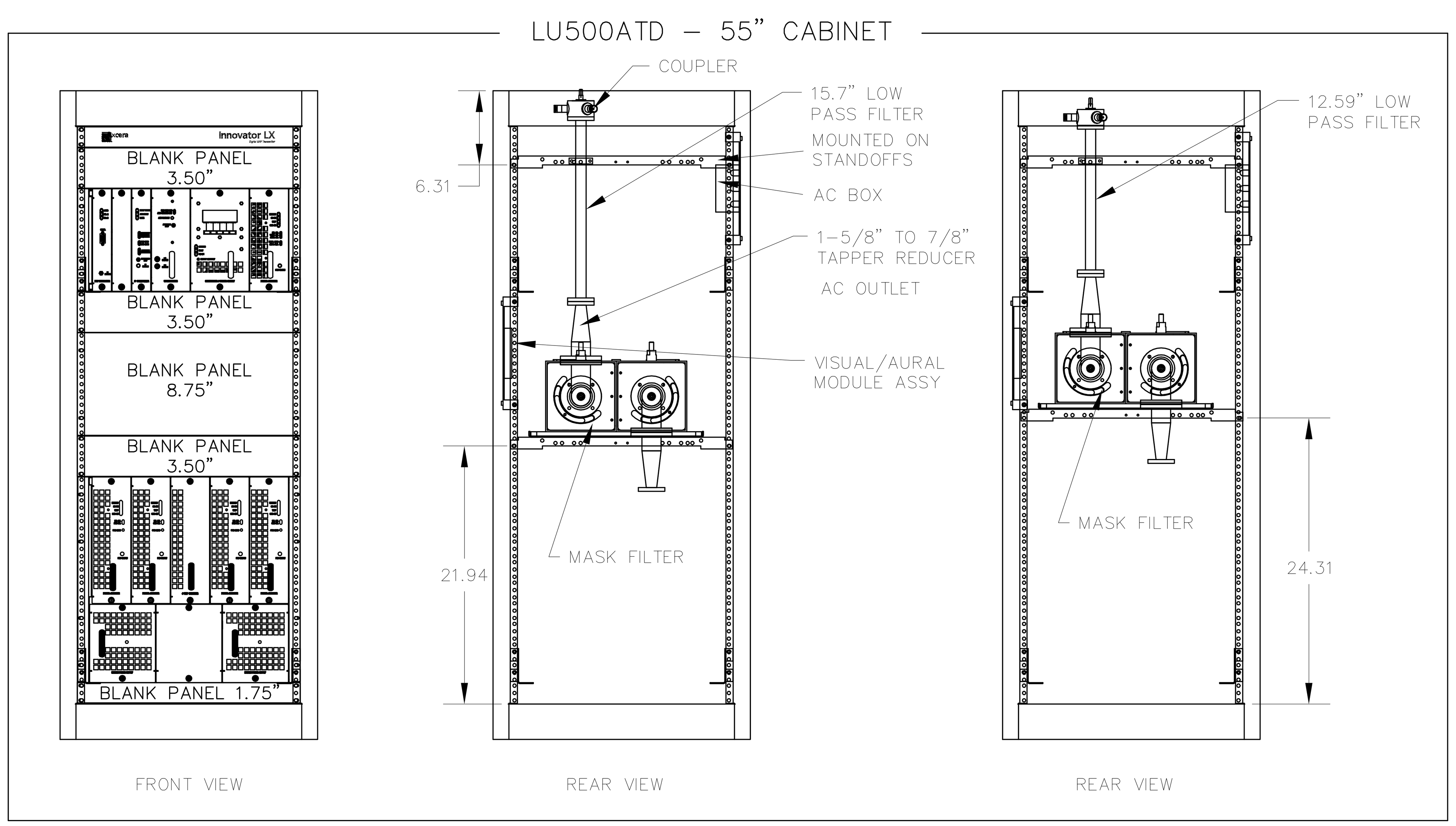
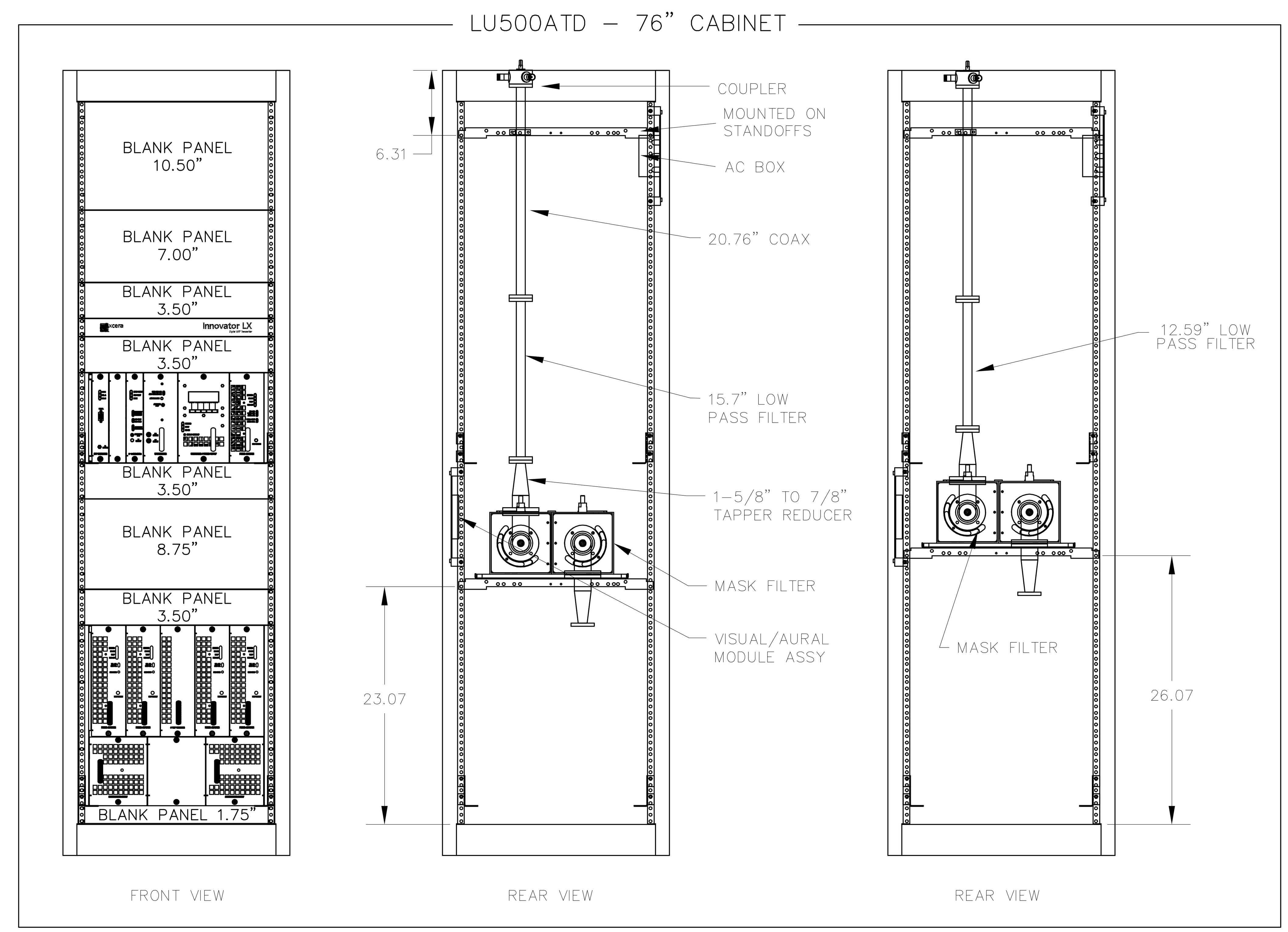
MATERIAL — — — —

FINISH — — — —

TITLE
SCHEMATIC
DIRECTIONAL COUPLER
BOARD

DWN	MH	8/11/03	DWG. NO. 1303152	REV A0
CHK	JCM	8/25/03		
REL	JCM	8/25/03	B SCALE — — —	SHEET 1 OF 1





REV	ECO	DATE	APV	DESCRIPTION
H0	2011257	4/25/07	LRT	CHANGE LU125-500ATD TO LU500ATD DELETED LU50ATD LAYOUTS AND DT1C TRAY. ADDED DM8 SLED. (JEC)
G0	2011557	10/20/04	LRT	CHANGE LU500ATD – 76" CAB TO LU125-500 RT
F0	2011494	8/24/04	LRT	CHANGED HYBRID COMBINER RT
E0	2011262	2/24/04	GJN	ADD 1000ATD (SAK)
D0	2011232	2/3/04	RT	ON 76" CABINET: TITLE PLATE AND TRAY RACKING RECONFIGURED. DELETED LOWER AC BOXES. (SAK)
C0	2011186	1/12/04	RT	CHG 69 CAB TO 76 RT
B	2011169	12/15/03	RT	ADDED 1.75 BLANK UNDER AMP. COMBINED BOTTOM AC. RT
A	2011143	11/20/03	RT	NEW RELEASE

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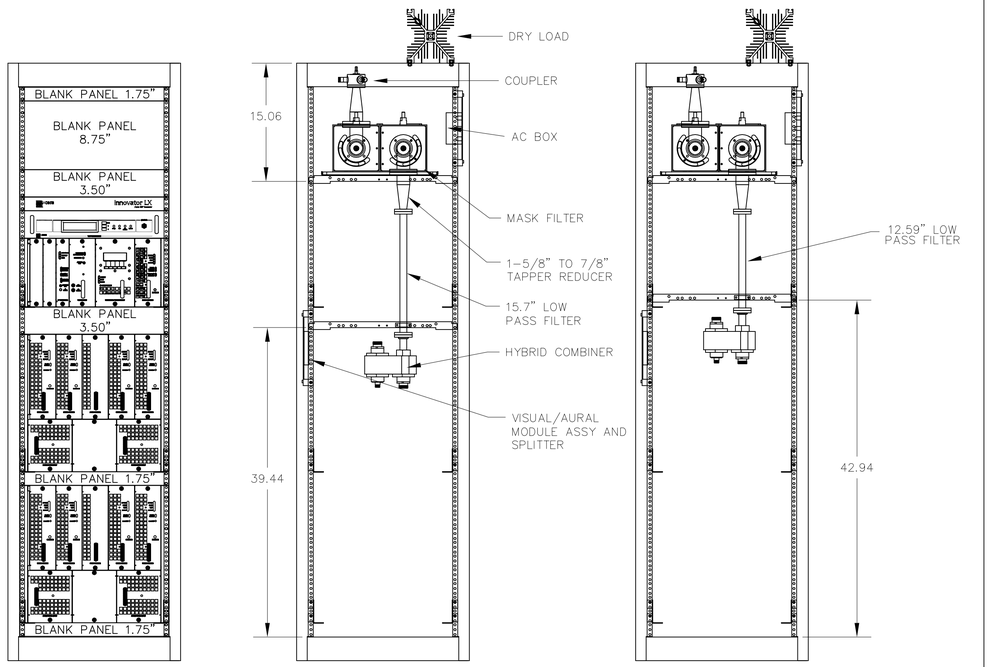
MATERIAL ----	TITLE	RACKING PLAN INN. DIGITAL LX 500W–1000W TYPICAL CONFIGURATION		
	DWN	RT	11/20/03	DWG. NO. 1303596 — REV H0
FINISH ----	CHK	RT	11/20/03	
	REL	RT	11/20/03	D — SCALE — SHEET 1 OF 2

LU1000ATD – 76" CABINET



REV	ECO	DATE	APV

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MATERIAL ----

FINISH ----

TITLE RACKING PLAN
INN. DIGITAL LX 500W–1000W
TYPICAL CONFIGURATION

DWN	RT	11/20/03	DWG. NO. 1303596	REV H0
CHK	RT	11/20/03		
REL	RT	11/20/03	D SCALE	SHEET 2 OF 2

NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

Serial Address

MC74VHC245DT

(See note on sheet 3)

CD74HC4051M

U4 1302044

2-61100-4472

1095823

MANUAL MICRO RESET

453-HC373XX

MC74VHC245DT

LT1076-ND

PROGRAMMING ENABLED

ENABLED

DC OK

TEMP

MOD OK

FIRMWARE CONFIGURATION

MOD OK LED NOTE:

LED is red and blinking if a fault is present

1 blink means Amp Current fault
2 blinks means Temperature fault
3 blinks means +32V supply over voltage
4 blinks means +32V supply under voltage
5 blinks means Reflected Power fault
6 blinks means +12V or -12V fault

MATERIAL NUMBERS:
1303682 A/D, INNOVATOR LX, AMP CTRL
1303683 SCH, INNOVATOR LX, AMP CTRL
1303696 PCB, INNOVATOR LX, AMP CTRL
1303697 STENCIL FOR 1303696
1303698 FIRMWARE, INNOVATOR LX, AMP CTRL

PAGE 2 , B-4 AREA, R214 WAS 100 OHMS. CR

H0	20112473	4/13/07	TB
R61 WAS 1.21K. R118 WAS 220. ADDED C112 & R214. DEL C78. Q16 & R114 CHANGED TO NOT USED.			JKF
G0	20112306	10/23/06	LRT
R66 WAS 1.47K. R78 WAS 1.21K. U10B PIN 5 SIGNAL NAME WAS 2.257V.			CR
F0	20111898	2/28/06	LRT
ADDED C110 & C111. ADDED NOT USED R211 & R212.			JKF
E0	20111812	7/6/05	LRT
C43, C45, C47, C59, C61 & C63 WERE 1800pF. J6 & J9 WERE STRAIGHT.			JKF
D0	20111601	5/19/05	LRT
C6, C8, C11, C12, C15, C18 - C22, C25 - C28, C43, C45, C47, C59, C61 & C63 WERE .01uF. C44, C46, C48, C60, C62, C64, C94, C98, C102 & C107 WERE .1uF.			JKF
C0	20111538	10/11/04	REH
PG 1) ADD R206 FROM U1.19 TO U1.20 ADD R207 FROM U8.19 TO U8.20. ADD R208 FROM U2.2 TO GROUND. PG 2) REMOVE C55, C56,C57. CHANGE E15 THRU E20 TO TB15 THRU TB20 (NEW P/N 1304505). PG 3). REMOVE CR22, CR23, CR25, CR27, CR32, CR34. CHANGE R126, R139, R153 FROM 2.2K TO 0 OHMS. ADD R209 FROM U22A.2 TO GROUND. ADD R210 BETWEEN U22A.1 AND U22A.2.			(CR)
B0	20111421	6/15/04	REH

REV	ECO	DATE	APV
Axcera			

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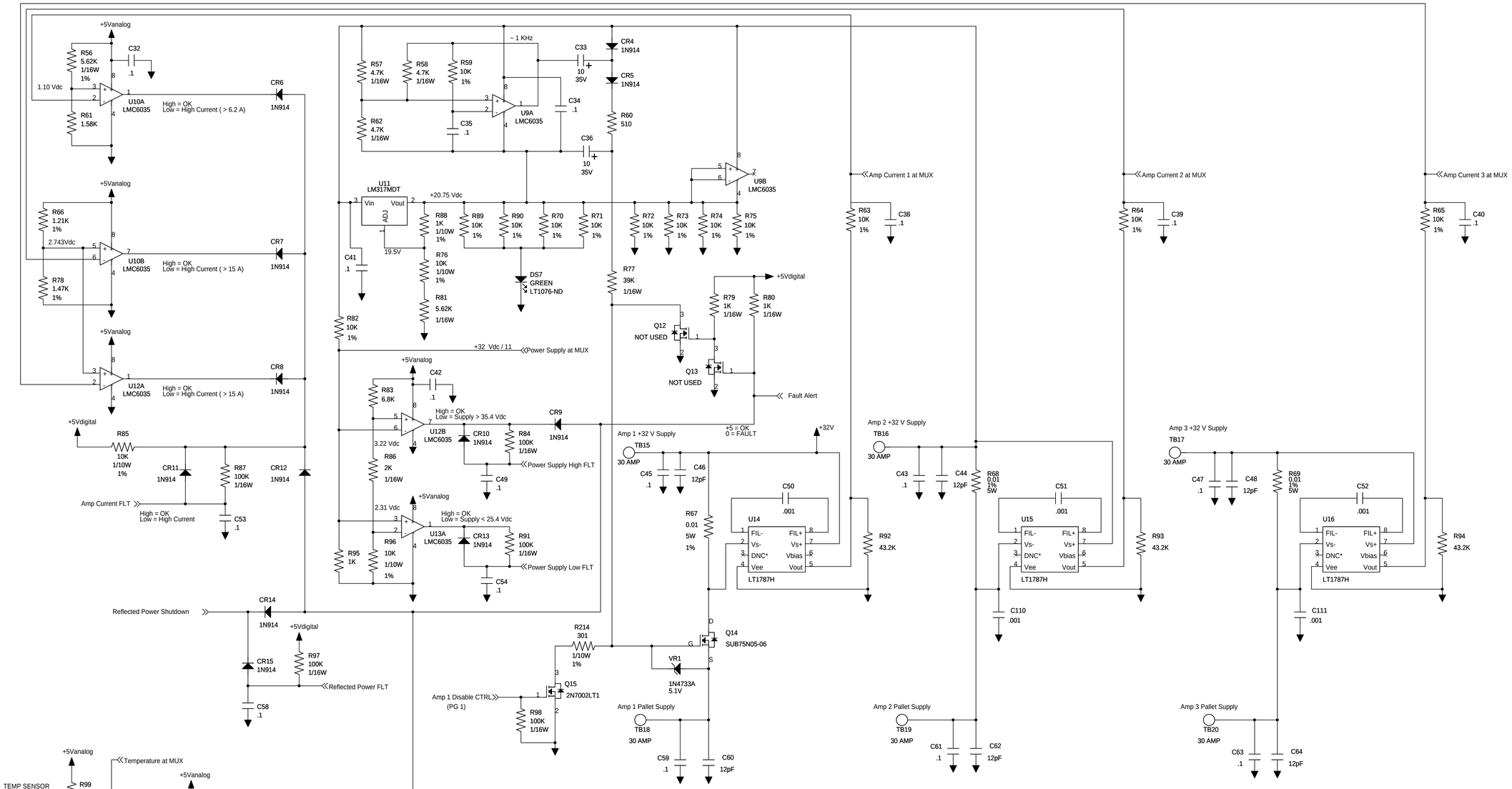
MATERIAL -----

FINISH -----

TITLE SCH., AMP. CONTROL, INNOVATOR LX (1303682)

DWN	REH	12/16/03	DWG. NO. 1303683 REV H0
CHK	REH	12/16/03	
REL	REH	12/16/03	D SCALE --- SHEET 1 OF 3



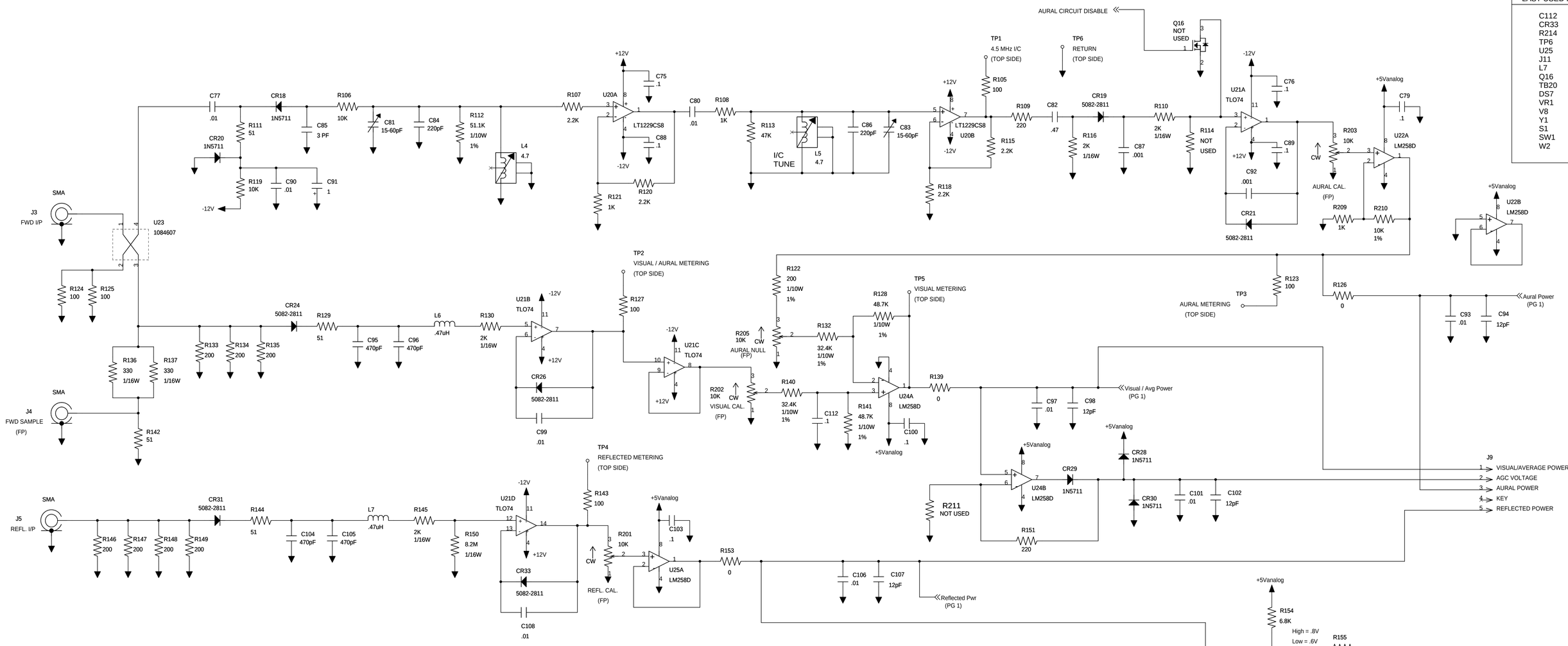
NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.

APV	Axcera		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., AMP. CONTROL, INNOVATOR LX (1303682)			
ECO	MATERIAL -----	DWN	REH	12/16/03	DWG. NO. 1303683	REV H0
REV	FINISH -----	CHK	REH	12/16/03		
		REL	REH	12/16/03	D	SCALE --- SHEET 2 OF 3

LAST USED REF.

C112
CR33
R214
TP6
U25
J11
L7
Q16
TB20
DS7
VR1
V8
Y1
S1
SW1
W2



Circuit Description

Page 1:
Upper center of page one is U4 which is the controller. This in-circuit Atmel microcontroller is operated at 3.6864 MHz. Programming of this device is performed through J2. U4 selects the desired analog channel of U3 through the settings of PA0 - PA2. PA3 of U4 is a processor operating LED that can be flashed to show continued operation.
PF1 is used to monitor the +12 Vdc supply to the board. PF4 is the selected channel of analog switch U3. PF3 and other select microcontroller pins are connected to a via for future access.

U2 is our standard serial to RS-485 driver IC. U5 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). U5 momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper left corner U1 is used to determine where the amplifier control board is located. The eight inputs come from amp connector J8 and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U6 below U1 is used to control two of the four board's status LEDs and three other circuits that are not allowed to change state during a microcontroller reset. A FET is turned on to shut current away from the LED to turn it off. U8 below U6 is used to enable different features within software. Actual use is TBD.

Page 2:

In the lower right corner are voltage regulator circuits. U17 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60C max and Tj = 125C max. 0.26 amps can be obtained from U17 if the mounting pad is 0.5 sqr. inches. The controller will not need this much current.

U18 and U19 are low drop-out voltage regulators with a tolerance greater than or equal to 1%. 100 mA is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U9 and U11. U11 is used to generate a regulated voltage that is about 5 Volts less than the +32 Volt supply. When the +32 Volt supply is enabled, the circuitry around U9A is used to provide gate voltage to Q14 that is 5 volts greater than the source pin of this FET. The gate of Q14 can be turned off by any one of a few different circuits. These circuits are wired through Q12 and Q13. At this time these transistors are not installed but they may be installed to increase the shut-down time on a detected fault. Without Q12 and Q13 installed, Q14 is only turned off by the microcontroller through Q16.

U10A is used to detect high current in amplifier #1. At 1.10 Vdc, the current to amplifier #1 should be about 6.20 Amps. U10B and U12A are used to detect a high current condition in amplifier stages #2 or #3. With a 2.74 Vdc reference, high current shut down should be about 15 Amps.

U12B is used to detect high power supply voltage. U13A is used to indicate that the power supply voltage is less than 26 volts.

U25B on page 3 is used to detect high reflected power. U13B determines if the power supply temperature gets too hot.

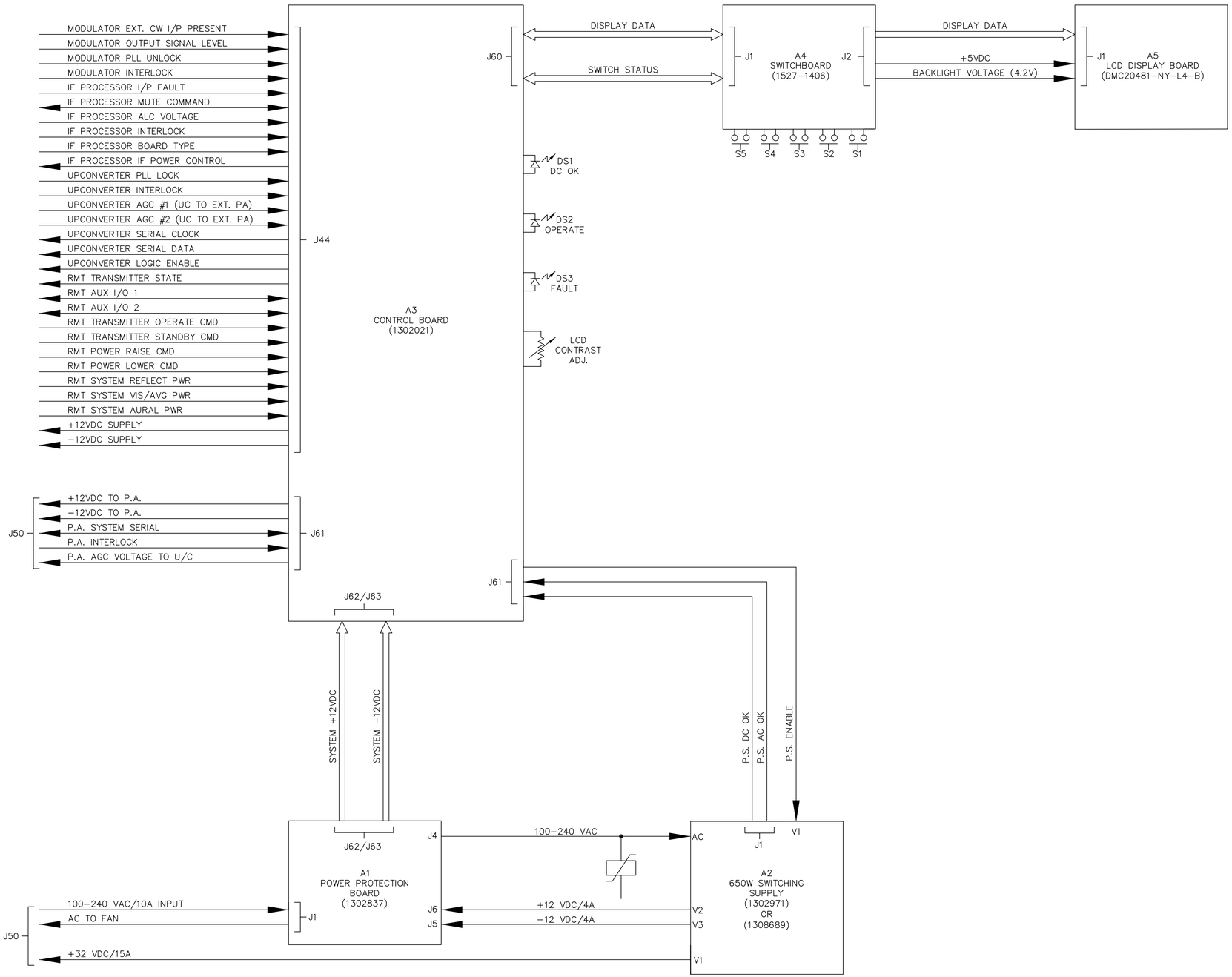
Current Monitoring Sections - A 0.01 ohm 1% 5 Watt thru-hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across this resistor is amplified for current monitoring by U14, U15, or U16. The Linear Technology LT1787HVCS8 precision high side current sense amplifier accepts a maximum voltage of 60 Vdc. The 43.2 Kohm resistor from Pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacture internal matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of -200ppm/C but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements.

Page 3:

RF power detector circuits. Q16 is used by the microcontroller to disable the aural circuit of a digital transmitter or in external amplifiers where the amplifier is not to monitor visual power.

The Visual or Forward power circuit is calibrated and presented on the input of U24B pin 5. If this module has the highest detected forward power in a multi-amplifier system, it will have the highest forward power signal. This signal level into U24B pin 5 will be used to set the AGC output voltage of J9-2. If another amplifier has a higher forward power, the level into U24B pin 6 will be higher than pin5 and this amplifiers output signal will not be used to set the voltage level of J9-2.

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., AMP. CONTROL, INNOVATOR LX (1303682)		
ECO	MATERIAL -----	DWN REH 12/16/03	DWG. NO. 1303683	REV H0	
REV	FINISH -----	CHK REH 12/16/03			
		REL REH 12/16/03	D	SCALE ---	SHEET 3 OF 3



REV	ECO	DATE	APV

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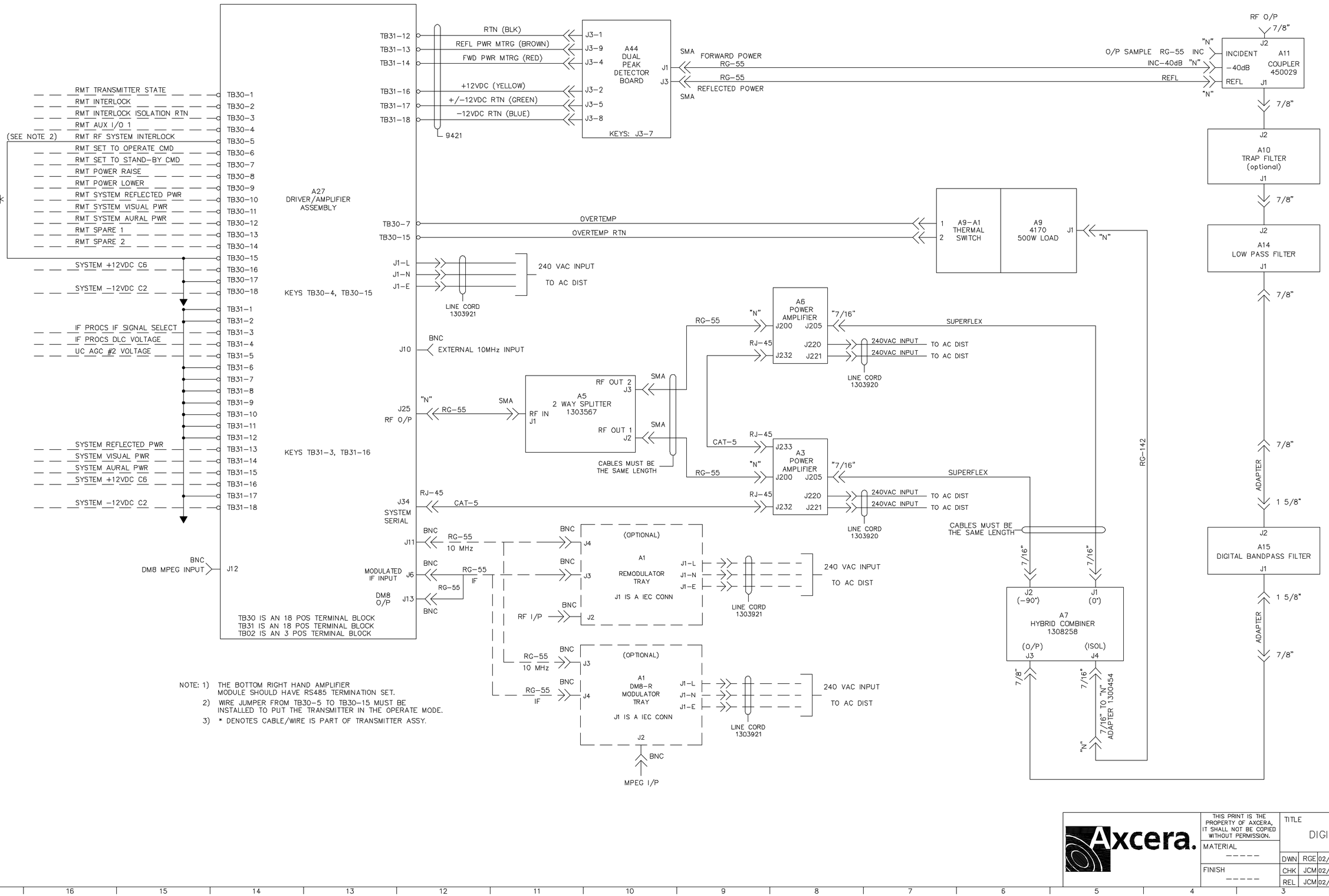
MATERIAL

FINISH

TITLE
B/D,
CONTROL/POWER SUPPLY
ASSEMBLY, INNOVATOR LX

			DWG. NO.	REV.
DWN	RGE	1/28/04	1303889	A0
CHK	JCM	2/2/04		
REL	JCM	2/2/04	D SCALE ---	SHEET 1 OF 1



NOTE: 1) THE BOTTOM RIGHT HAND AMPLIFIER MODULE SHOULD HAVE RS485 TERMINATION SET.

2) WIRE JUMPER FROM TB30-5 TO TB30-15 MUST BE INSTALLED TO PUT THE TRANSMITTER IN THE OPERATE MODE.

3) * DENOTES CABLE/WIRE IS PART OF TRANSMITTER ASSY.

A44 WAS VISUAL/AURAL METERING BOARD. A27-TB31-14 WAS VISUAL POWER MTRG (RED). DELETED A27-TB31-15, AURAL PWR MTRG (ORNG). A24 WAS DTIC MODULATOR. ADDED A27-J12. DELETED A27-J7, J17, J4, J3, TB02-1, TB02-2, & TB02-3. ADDED CONNETION AT A27-J6 TO A27-J13. (SAK)

REV	ECO	DATE	APV
D0	20112639	6/26/07	LRT
ADDED "RF IN" AND "RF OUT" TO A5 CHANGED KEYS ON A2: WAS TB30-1, TB30-18, TB31-2, TB31-17. CHANGED HYBRID			RT
C0	20111494	8/17/04	LRT
A44 WAS A4, A11 WAS A13. CHANGED TO MATCH HARNESS BOARD.			RT.
B0	20111262	3/1/04	LRT

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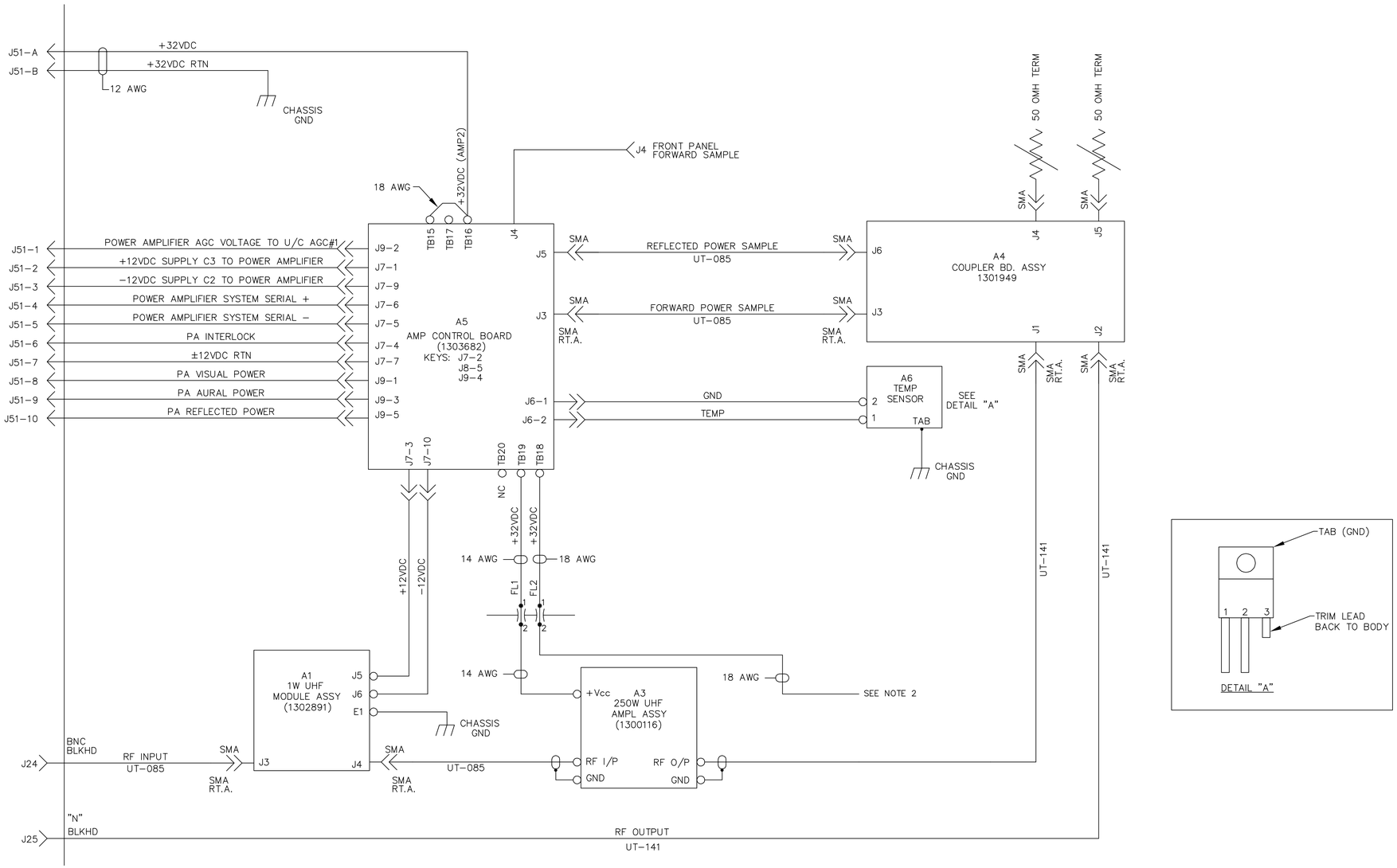
MATERIAL ------

FINISH ------

TITLE
I/C
DIGITAL LX SERIES, 1KW
TRANSMITTER

DWN	RGE	02/11/04	DWG. NO. 1303941 REV D0
CHK	JCM	02/11/04	
REL	JCM	02/11/04	D SCALE --- SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 20AWG UNLESS OTHERWISE NOTED.
2. THIS WIRE IS NOT USED ON THIS ASSEMBLY. COVER THE END WITH HEAT SHRINKABLE TUBING AND TIE BACK IN THE HARNESS.

REV	ECO	DATE	APV
A4 WAS 1227–1316. ADDED COAX FROM A4–J6 TO A5–J5. ADDED 50 OHM TERMINATIONS AT A4. (SAK)			
CO	201112047	3/1/06	LRT
DELETED 50 OHM TERMINATION AT A5–J5. (RGE)			
BO	201117660	5/05/05	LRT

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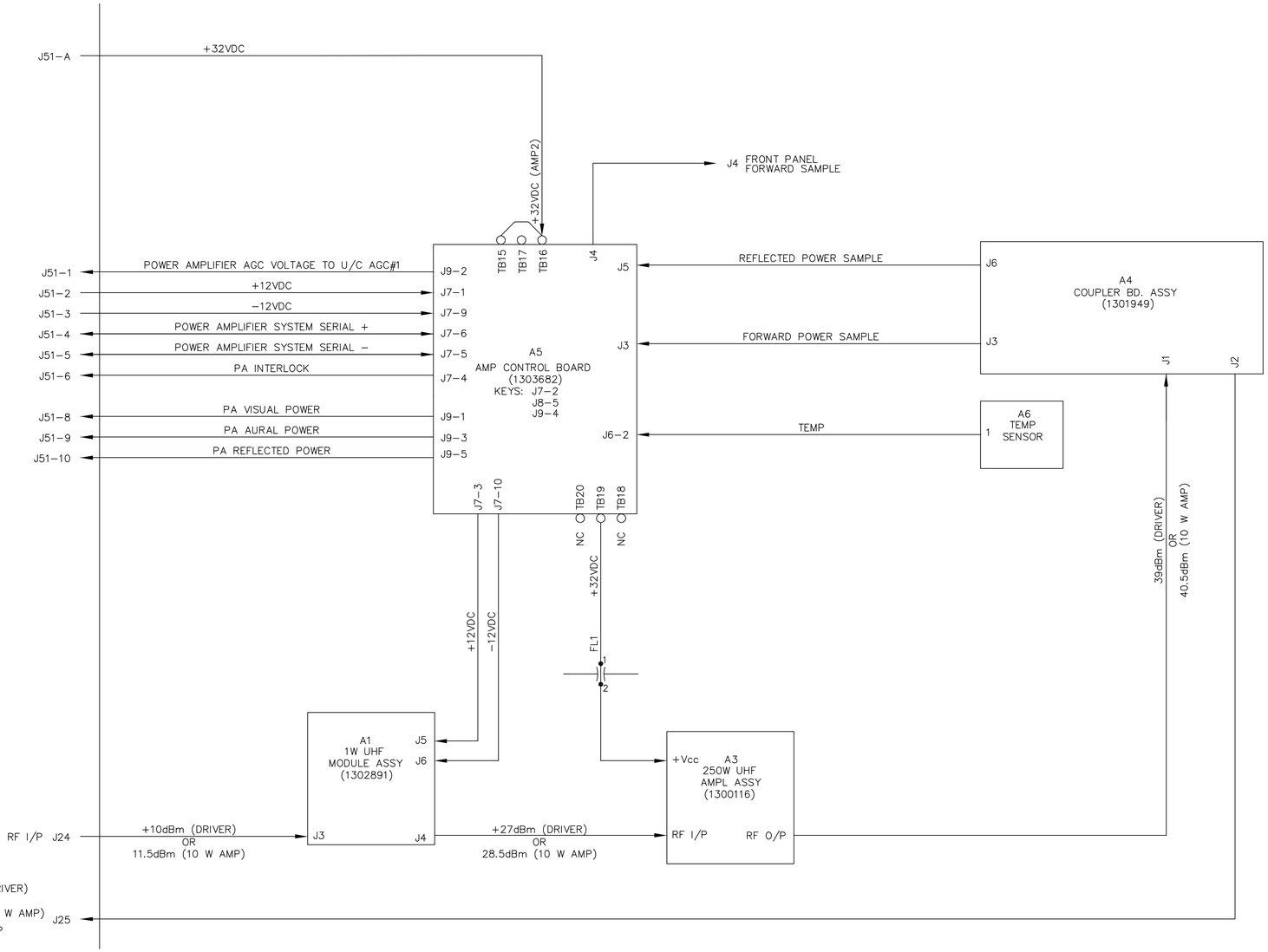
MATERIAL ––––––

FINISH ––––––

TITLE
I/C,
PA ASSEMBLY, 2KW DRIVER/
10 W PA, LX SERIES

DWN	RGE	11/17/04	DWG. NO. 1305137 REV C0
CHK	LRT	11/18/04	
REL	LRT	11/18/04	D SCALE ––– SHEET 1 OF 1



NOTE:
1. ALL POWER LEVELS ARE PK–SYNC +10% AURAL. FOR DTV LEVELS, SUBTRACT 3dBm.

A4 WAS 1227–1316.
ADDED REFLECTED SAMPLE FROM A4–J6 TO A5–J5.
ADDED AMPLIFIER POWER LEVELS. (SAK)

REV	ECO	DATE	APV
B0	20112047	3/1/06	LRT

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MATERIAL
–––––

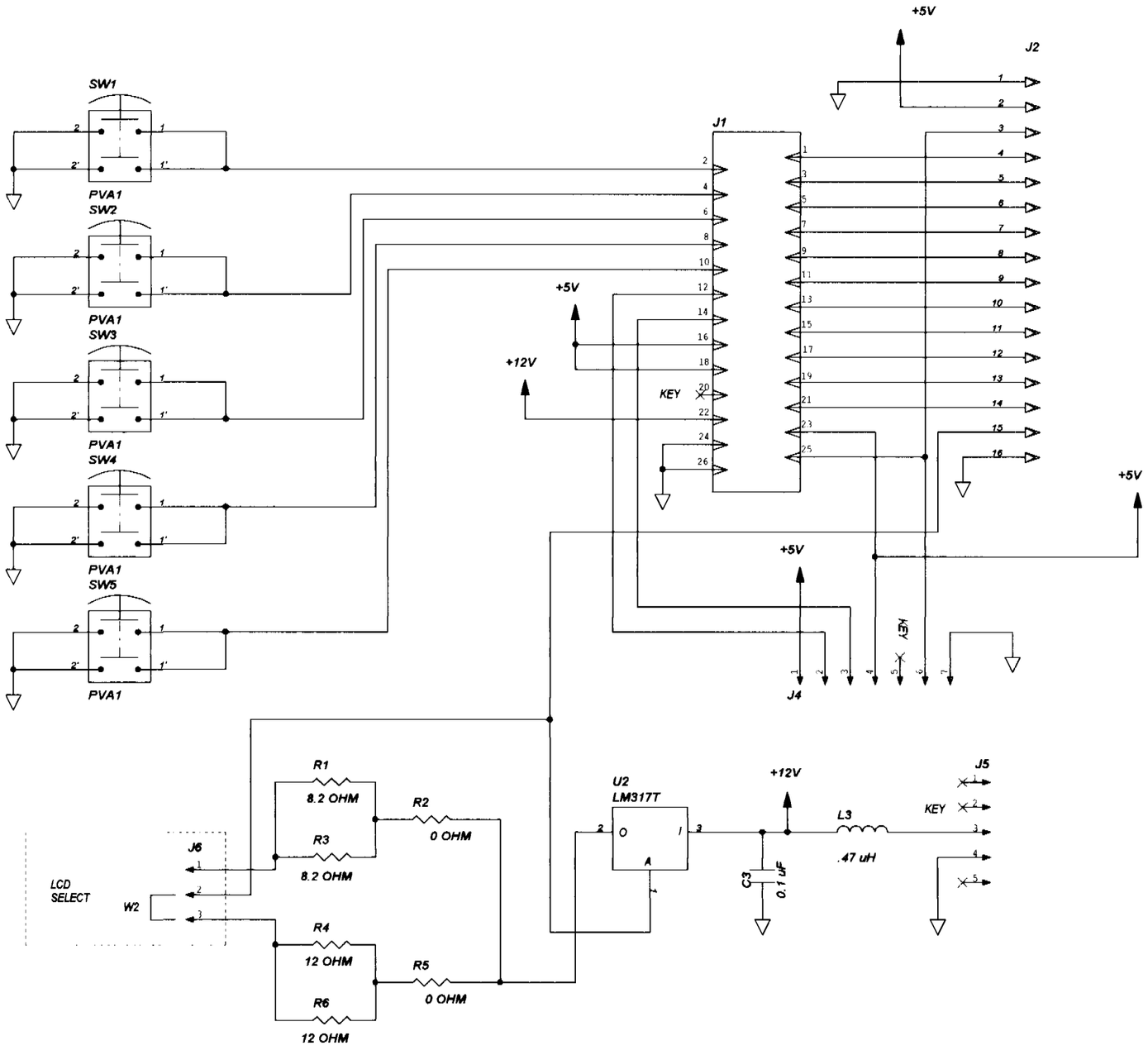
FINISH
–––––

TITLE
B/D
PA ASSEMBLY, 2KW DRIVER/ 10 W PA, LX SERIES

DWN	RGE	11/17/04	
CHK	LRT	11/18/04	
REL	LRT	11/18/04	

DWG. NO. 1305138 REV B0

D SCALE ––– SHEET 1 OF 1



DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3. JKF

REV	ECN	DATE	APV
3	8603	11/7/96	RAS
AT J2 W2 WAS W1. (TMY)			
2	8424	9/29/96	JCM
SWITCHED PINS 1 & 2 OF U2. (TMY)			
1	8368	8/27/96	RAS

ITS CORPORATION

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MATERIAL ---

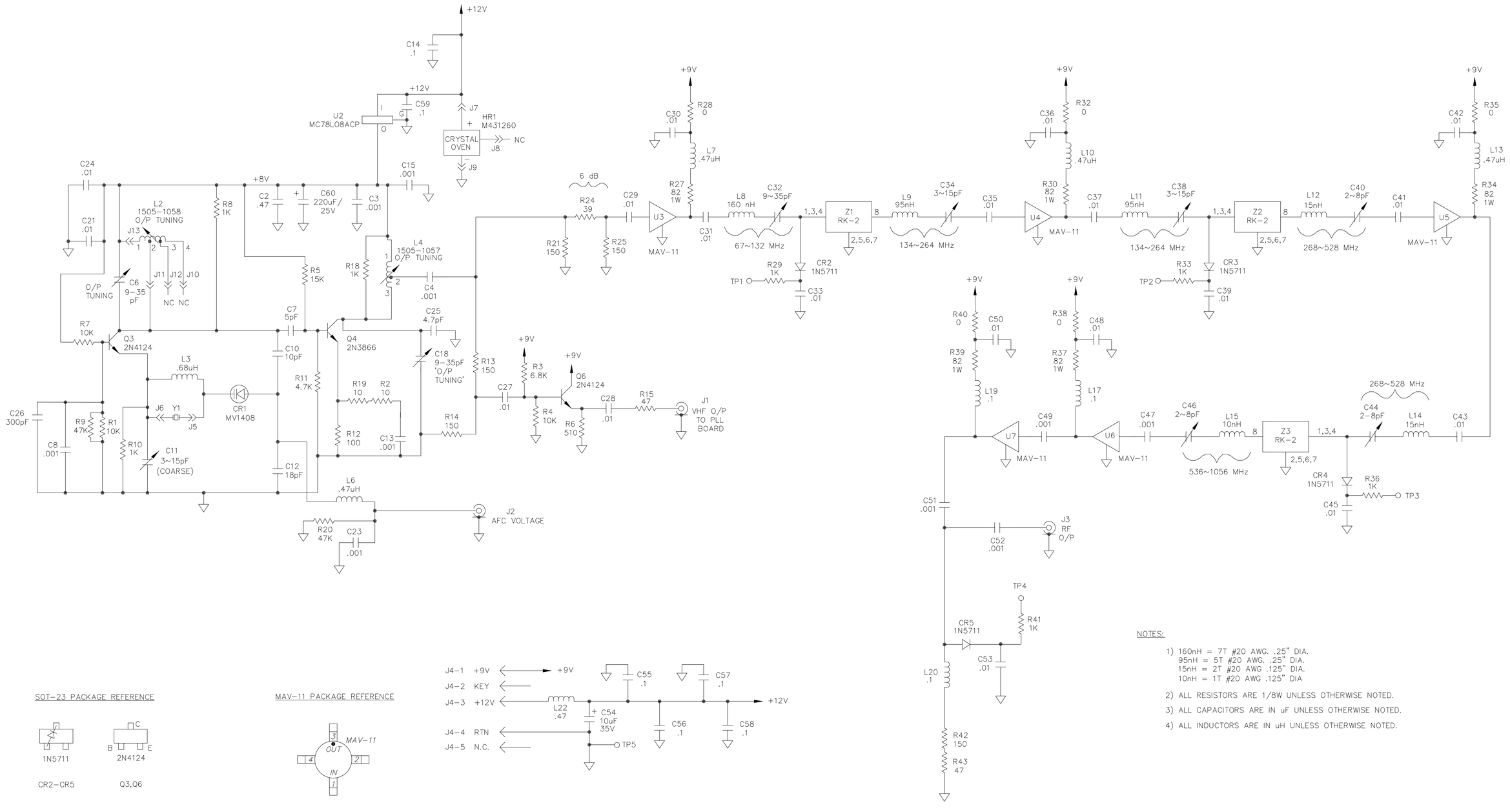
FINISH ---

TITLE SCHEMATIC SWITCH BOARD (1527-1406)

DWN	DLM	6/3/96	
CHK	RAS	6/14/96	
REL	RAS	6/14/96	

DWG. NO. 1527-3406 REV 3

B SCALE --- SHEET 1 OF 1



NOTES:

1) 160nH = 7T #20 AWG. .25" DIA.
   95nH = 5T #20 AWG. .25" DIA.
   15nH = 2T #20 AWG .125" DIA.
   10nH = 1T #20 AWG .125" DIA
2) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
3) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
4) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
2	9386	6/20/98	DWB
1	9312	1/30/98	DWB

ADDED C60 & C54
WAS 47uF/20V.
(RFB)

R28,32,35,38, & 40 WAS 27ohm. R27, 30,34,37, & 39 WAS 100ohm 1W. ADDED +9V TO BD. AT J1– 1 LOCATION. ALL +9V WAS +12V. JKF

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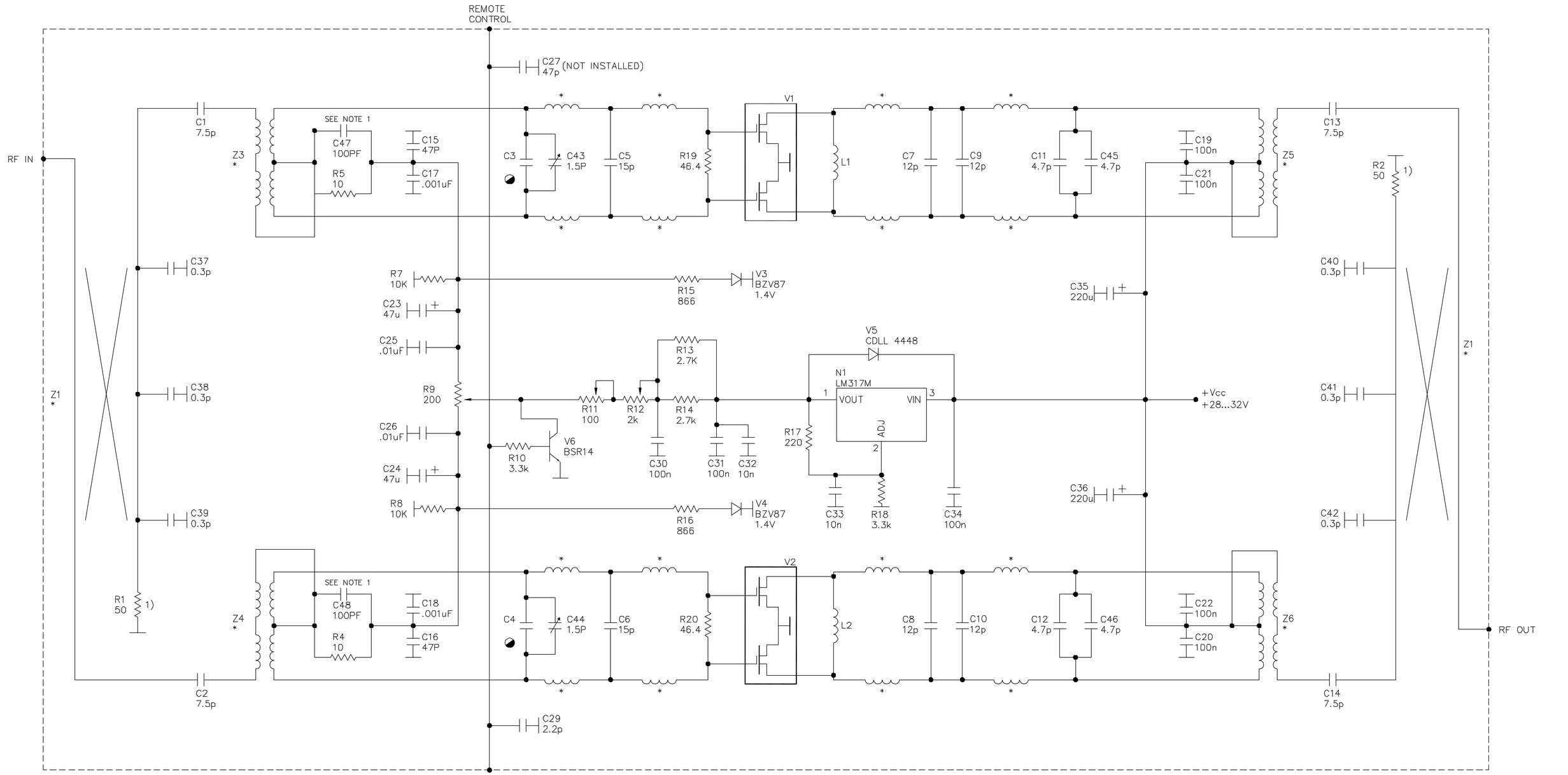
MATERIAL – – – –

FINISH – – – –

TITLE: SCHEMATIC – UHF GENERATOR BOARD (1585–1265)

DWN	JKF	12/8/97	DWG. NO. 1585–3265 REV 2
CHK	DWB	12/22/97	
REL	DWB	12/22/97	D SCALE – – SHEET 1 OF 1



* PRINTED COMPONENT

FACTORY SET VALUE

PC BOARD LAYOUT SEE 51-5379-309-00 (2)

NOTE:

1) C47 IS LOCATED IN THE R3 POSITION ON THE PCB.
   C48 IS LOCATED IN THE R6 POSITION ON THE PCB.

REV	ECO	DATE	APV
DELETED PTF10159 P/N FROM LDMOS. ADDED C23,C24 & C27. CDD/CR			
C0	20110221	5/17/02	RE
R15 AND R16 WERE 680 OHMS. PWN			
B0	20100316	04/02/02	LRT

REV	ECO	DATE	APV
ADDED NOTE 1. JKF			
G0	20112235	11/13/07	LRT
R15 & R16 WERE 820 OHM. JKF			
F0	20111398	5/1/06	LRT
R9 WAS 50. RGE			
E0	20110785	5/14/03	LRT
CHANGE R3 FROM A 2.2 OHM RESISTOR TO C47, SM., CAP., 100PF, 500WVDC. CHANGE R6 FROM A 2.2 OHM RESISTOR TO C48, SM., CAP., 100PF, 500WVDC. CHANGE R4 FROM A 2.2 OHM RESISTOR TO 1590600OSMT, SM., RES., 10 OHM 5% 1/8W. CHANGE R5 FROM A 2.2 OHM RESISTOR TO 1590600OSMT, SM., RES., 10 OHM 5% 1/8W. CHANGE C17 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1590616OSMT, SM., CAP., .001 UF, 50 WVDC. CHANGE C18 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1590616OSMT, SM., CAP., .001 UF, 50 WVDC. ADD C23, 1501246, SM. CAP, 47MF, 50V, LOW ESR. C24. ADD C24, 1501246, SM. CAP, 47MF, 50V, LOW ESR. ADD C25, 1590616ISMT, SM., CAP., .01 UF, 50 WVDC. ADD C26, 1590616ISMT, SM., CAP., .01 UF, 50 WVDC. PWN			
D0	20110444	09/18/02	RJ

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MATERIAL

FINISH

Axcera

TITLE AMPLIFIER MODULE

DWN	PWN	04/01/02	DWG. NO.		REV
CHK	LRT	04/03/02	51-5379-309-00 WSP		G0
REL	LRT	04/03/02	D	SCALE	SHEET 1 OF 1