8. OPERATIONAL DESCRIPTION - MODEL Axcera-5543A

8.1 General Description

The 5543A transmitter is a complete 8-watt solid-state, digital frequency agile transmitter. It operates at a nominal output power of 8 watts (average). This transmitter can be used, as a back-up transmitter should a main transmitter fail and become inoperable.

Functionally, it is comprised of a QAM modulator (Comstream CM720M) tray, a frequency generator tray, and upconverter/amplifier tray. The modulator receives a 28 Mbit/sec, serial bit stream, consisting of multiplexed MPEG-2 transport streams, translates the signal to a Quadrature Amplitude Modulated (QAM) format, converts the digital information to analog and modulates the signal to IF (44MHz).

The modulator tray's IF output is then routed to the upconverter/amplifier tray for IF signal processing, upconversion to the BRS/EBS band, and then amplification. The frequency generator tray generates the variable second conversion local oscillator signal, which is fed to the upconverter/amplifier tray, using a number of highly stable VCXO's. The VCXO's are microprocessor selectable and controlled by an automatic frequency control (AFC) voltage in a PLL configuration. The upconverter/amplifier tray utilizes ALC/AGC circuitry for automatic level control of the IF signal and automatic gain control of the output signal. The upconverter/amplifier tray also employs Feed Forward distortion cancellation to insure error free signal transmission. All three trays are 19-inch rack mount assemblies and can be supplied with or without a cabinet. The unit is supplied complete with cables and cabinet slides.

8.2 Technical Specifications

Type of Emission 6M00D7W

Frequency Range..... 2572 to 2614 MHz

Output Power Rating.....8 watts average

8.3 Performance Specifications

Operating Frequency Range..... 2572 MHz to 2614 MHz

RF output - Nominal:
- Power .....8 watts average
- Impedance .....50 ohms
- Connector ..... Type N

Modulation..... QAM, MPEG-2 Transport Stream
Phase Noise ..... < or = 110 dBc (single sideband measurement)
Frequency Response ..... ± 0.5 dB
Group Delay .....40 nsec peak-peak (Measured with 1 MHz delay aperture)
Gain Linearity (AM-AM [2]) ..... 0.2 dB /dB
Phase Linearity (AM-PM [2]) ..... 1°/dB
IF Input Frequency .....41-47 MHz or 32-40 MHz
IF Input Impedance .....75 or 50 Ohms (specify)
IF Input Level .....+25 to +35 dBmV (-23 to –13 dBm) average
Frequency Stability [3] .....± 500 Hz (standard)
w/Precise Frequency Option.....± 1 Hz (optional)

<u>Electrical Requirements</u>

Power Line Voltage ..... 110 volts, 60 Hz
220 volts, 50/60 Hz
Power Consumption ..... 1245 watts

<u>Environmental</u>

Maximum Altitude .....12,000 feet
Operational Temperature Range.....0°C to +45°C

Mechanical

Dimensions:

Width	19 inches
Depth	21 inches
Height	15.75 inches
Weight	130 lbs

[2] Specified at 6dB above digital average power.
[3] When interfaced with 5060 10 MHz system reference or GPS precise reference.

8.4. System Overview

The 5543A transmitter is made up of the trays listed in Table 8-1.

Table 8-1. 5543A Major Trays and Assemblies

MAJOR ASSEMBLY DESIGNATOR	TRAY / ASSEMBLY NAME
A1	QAM Modulator Tray
A2	Frequency Generator Tray
A3	Upconverter/Amplifier Tray

8.4.1 QAM Modulator Tray

The CM720M modulator tray generates a 64 QAM digital IF output which is used to drive the upconverter/amplifier tray. External, multiplexed 28 MBPS data is applied to the rear of the modulator tray. The digital data is received using an IC chip set known as TAXI® (Transparent Asynchronous Transmitter/Receiver Interface) on the Digital Data Input Card. TAXI is a registered trademark of Advanced Micro Devices (AMD).

The TAXI receiver operates in 10 bits-per-byte mode (8 data bits, 1 even parity bit, 1 active low-frame sync bit). The TAXI receiver reference clock (5 MHz) is fed to the modulator.

The digital bit stream of data from the Digital Data Card is fed to the Quadrature Amplitude Modulator (QAM) digital modulator on the Modulator Card. The data/clock signal is continuously monitored for the following:

1. Clock out of spec (more/less than 100 ppm of spec)
2. Loss of clock
3. Parity errors
4. Frame sync errors
5. Sync acquisition errors
6. TAXI decoding violations

The system is normally frequency locked to the input clock. If the input clock is not present, the system switches over to internal timing to preserve the output spectrum. When the system clock returns, the system will detect the presence of the clock and return to normal operation.

The outptut power of the modulator, which is monitored continuously, is adjustable form -27 dBm to -5 dBm.

The front panel of the CM720M modulator contains a seven-segment LED display, a LCD display, two LED fault indicators, control keys, and a numerical keypad to monitor and control the operating status of the tray. Also included on the front panel are IF and RF output test ports (refer to *Chapter 3: Front Panel Operation* of the Installation and Operation Manual, included in Exhibit II of this report, for a complete description of front panel operation).

The CM720M power supply is auto-ranging for AC inputs from 90 to 264 VAC and 47 to 63 Hz.

8.4.2 Frequency Generator Tray

The Frequency Generator Tray generates a variable frequency (960 to 1080 MHz) local oscillator (LO) signal that is fed to an upconverter within the Upconverter/Amplifier tray.

The 4 Channel VCXO Board (1527-1405) contains four independent VCXO circuits, which generate a highly stable frequency reference signal ranging from 127.250 to 129.500 MHz. Each oscillator, along with its associated components, form a Butler Common Base Oscillator Circuit. The output tank circuits are adjusted for maximum output level. Each oven is mounted in an oven set at 60°C for increased stability. On board variable capacitors provide coarse frequency adjustment while an AFC voltage, derived from an external PLL circuit described below, provides automatic frequency adjustment. The AFC voltage is looped through the board (J2 to J3) in order to be distributed to additional 4 Channel VCXO Boards. The output of each of the oscillators are buffered to summing resistors then to two amplifier/buffers which combine the signals into a single output at J1.

The outputs of the 4 Channel VCXO Boards are fed to the inputs of the VHF/Combiner Buffer Board (1527-1407), which is designed to combine independent RF inputs. Only one RF input is present at any given time. The selected channel oscillator signal is amplified and buffered to two outputs. The first output is fed to a front panel sample port (J5). The second output (J10) is fed to the input of the Broadband X4 Multiplier Board (1527-1404).

The input to the Broadband X4 Multiplier Board is amplified and fed to a broadband doubler IC. The doubler output is amplified and fed to a filter, which attenuates the input signal and all harmonics except the desired second harmonic. The filter output is amplified and fed to a second broadband doubler. The output of the second broadband doubler is fed to a filter designed to pass only the 4th harmonic of the input signal. The output of the board is fed to a Broadband UHF Filter (2005-1053) then to the PLL Board (1527-1402).

The PLL Board establishes a phase locked loop for the selected VCXO. An external 5 or 10 MHz reference, selected using an on board jumper (W1), is applied to the board at J1 and divided down to 1 MHz using a fixed divider IC. The VCXO signal is applied to the board at jack J2. The signal is amplified and split into two separate signals. The first is divided by a prescaler IC then sent to a programmable divider IC that compares the signal to the 5 or 10 MHz reference, producing two output phase signals. These output phase signals are fed to a comparator, which generates a proportional error (AFC) voltage. This AFC voltage is then fed to the appropriate VCXO on the corresponding 4 Channel Oscillator Board. The programmable divider may be programmed externally by the Frequency Generator Control Board (1527-1401) or by on board manual DIP switches. The second output of the splitter is the main output of the board and is fed to a Broadband UHF Filter (2005-1103) then to the UHF I/P X4 Multiplier Board (1128-206). The input to the UHF I/P X4 Multiplier Board is amplified and fed to a broadband doubler IC. The doubler output is amplified and fed to a filter, which attenuates the input signal and all harmonics except the desired second harmonic of the input signal. The filter output is amplified and fed to a second discrete component broadband doubler. The output of the second broadband doubler is fed to a filter designed to pass only the 4th harmonic of the input signal. The UHF I/P X4 Multiplier Board output signal is at the first conversion L.O. frequency for the selected channel. This first conversion L.O. signal is directed to the L.O. Amplifier Module (1557-1213), which amplifies the L. O. signal approximately 10 dB using a VNA-25 MMIC. The module output is filtered by a Filter Assembly (1128-1102) then fed to the rear panel L. O. output jack (J4).

The Frequency Generator Control Board utilizes a Motorola MC68HC70B16 microprocessor and software developed by ITS Corporation to monitor and control the operation of the tray. On board IC's and FET's receive commands from the microprocessor and selectively gate the VCXO's on or off. Under actual operation, only one VCXO is gated on at any given time. On board IC's provide status commands from the VCXO's to the microprocessor, which tell the microprocessor how many VCXO's are installed and whether each VCXO is gated on or off.

This board also provides for RS-485 data communications links between the tray and Supervisory Control and Data Acquisition (SCADA) and an Automatic Backup System (ABS).

Input commands are entered through the front panel soft-keys, and are passed to the microprocessor. Parallel data from the microprocessor is fed to output jack J10 then to a front panel 4 line X 20 character LCD display providing easy viewing indication of current tray status (operate/standby), selected channel (A1, B1 ect.), status of channel oscillators (available/unavailable) and faults (PLL unlock/transmitter fault/SCADA communications fault/ABS communications fault). In automatic mode, the microprocessor runs through a continuous loop checking for faults detected by the ABS system and automatically switches to the appropriate channel.

Tray power is supplied by a +12V/21 amp Switching Power Supply (SPL250-1012).

8.4.3 Upconverter/Amplifier Tray

The input to the Upconverter/Amplifier tray is a QAM digital IF (44MHz) signal. This digital QAM IF input signal is applied to the IF input jack (J2) on the rear of the tray. The IF input signal, referred to as the first IF signal (IF_1), is fed to the IF Input Equalizer Board (1555-1219). This board contains a transformer coupled input for impedance matching of the IF input signal (75Ω to 50Ω), a SAW filter, two sections of group delay equalization circuitry to compensate for group delay created by external filters, and three notch filters to adjust the response of the first IF_1 signal. The output of the IF Input Equalizer Board is fed to the ALC/AGC Board (1555-1216).

The signal enters the ALC/AGC Board at J1, and after a 6 dB pad, a IF band-pass filter, and a second 6 dB pad, is adjusted in level by the PIN Diode Attenuator/ALC circuitry. This circuitry takes a peak-detected sample of the IF signal and generates an ALC voltage, which biases a PIN Diode Attenuator. The ALC circuitry senses any change in the IF level and automatically adjust the loss of the PIN attenuator to compensate, thereby maintaining a constant IF output level regardless of minor changes in the input signal.

Next, the IF_1 signal is fed to a loop through at J2 to a series of three boards. The first, the Linearity Corrector Board (1555-1220) pre-distorts the IF_1 signal to compensate for compression in later stages of the system. The second board, the IF Phase Corrector Board (1555-1244), corrects for any phase error, which may be introduced by the amplifiers later in the system.

The phase and linearity corrected signal then enters the third board in the loop, the Peak Vs. Average Detector Board (1555-1254). On this board the signal is transformer coupled and buffered to peak and average detector circuits. The peak and average detector output signals are connected to a comparator which compares both signals and should the average signal approach the peak signal, indicating a loss in the QAM input signal, will send a fault

signal to the ALC/AGC Board. The main signal path consist of a 4 dB pad and MAV-11 amplifier which exits the board at J4 and reenters the ALC/AGC Board loop in at J7.

After an IF filter identical to that used on the main input of the board (J1), the IF_1 signal is applied to a splitter. One output of the splitter is fed to the ALC/AGC circuitry, which generates both the ALC voltage and the AGC reference voltage. The second output of the splitter is fed to an AGC PIN Diode Attenuator, which functions in the same manner as the ALC PIN Diode Attenuator. The AGC circuitry uses a DC level generated externally to control the output power level.

There are three possible AGC bias voltage inputs. The first two, Inner Loop 1 and Inner Loop 2 (J6-7 and 5), are generated from peak detected samples of the 3 Stage Driver Amplifier (A10-A1) and the 50 Watt Output Amplifier (A10-A3) respectively. Inner Loop 1 AGC bias voltage insures AGC operation in the event of a 50-Watt Amplifier fault. The third AGC bias voltage input, Outer Loop (J6-2), is used only if an external final amplifier tray is connected to the system. If both the Inner Loop and Outer Loop inputs are used, the signal that is largest in level controls the AGC circuit.

The AGC circuit can be bypassed by placing jumper W2 into the manual position (pins 1 and 2). When the AGC is disabled, the loss through the AGC PIN attenuator is adjusted by Manual Gain potentiometer R105, which then directly controls the output in a manual fashion. The AGC Pin Diode Attenuator output is fed to an amplifier then to three notch filters, which adjust the frequency response of the signal. The signal is then amplified once again and fed to the output of the board (J8), which is connected to the IF input of the first double balanced mixer (ZFM-15-SMA).

A UHF LO (local oscillator) signal, referred to as the first conversion local oscillator signal (LO_1) is generated on the UHF Generator Board (1512-1101). This Board uses a voltage controlled crystal oscillator circuit and x8 multiplier, consisting of three x2 broadband doublers (2^3 = x8), to produce the LO_1 signal (583 MHz). The oscillator circuit is a modified Colpitts design and the crystal is mounted in an oven set at 60° C and operates at 1/8 of the first conversion local oscillator frequency. The voltage controlled crystal oscillator circuit within the UHF Generator Board is controlled by the VHF Generator Control Board (1555-1214), which locks the LO_1 signal to a precise external 10 MHz reference, which is applied to the rear of the tray at jack J3. The PLL circuit on the VHF Generator Control Board divides a sample of the VCXO frequency and compares it to the divided down reference frequency (50 KHz) also generated on the VHF Generator Control Board. The difference between the phase of the reference frequency and the divided down VCXO frequency sample causes the PLL IC to create an error output voltage called the Automatic Frequency Control (AFC) voltage, which is used to bias a variable capacitor in the VCXO circuit. A sample of the first conversion local oscillator signal is available at the front panel jack J16. The output signal of the UHF Generator Board is fed through a UHF filter (1007-1101) then to the LO input of the double balanced mixer which mixes the first conversion local oscillator signal and the first IF signal generating an output consisting of the sum (LO_1 + IF_1), difference (LO_1 - IF_1), first IF and first conversion LO frequency signals.

This signal is passed through a 4 Pole UHF Filter (2005-1047) which passes only the difference signal referred to as the second IF (IF_2). This IF_2 signal, at a frequency of 539 MHz, is applied to the IF input of a second double balanced mixer (A13).

A second conversion LO signal (LO_2), from the Frequency generator tray, enters the tray at rear panel jack J5 and is fed to the Local Oscillator Amplifier Module (1557-1213). This amplifier module amplifies the signal to a sufficient level to drive the LO input of the second double balanced mixer (A13) which mixes the second conversion LO signal and the second IF signal producing an output consisting of the sum (LO_2 + IF_2), difference (LO_2 - IF_2), second IF and second conversion LO frequency signals. This signal is amplified by a Local Oscillator Amplifier and applied to a Three Stage Broadband Filter (1107-1101), which passes only the sum frequency signal (LO_2 + IF_2). The RF output signal of the filter is fed to a circulator then to the input of a Three Stage Amplifier Module (1516-1108).

The Three Stage Amplifier Module consists of three cascaded GaAs FET amplifiers (FLL-101 driving a FLL-351 driving a FLL200) with an overall gain of 36 dB. The output of the Three Stage Amplifier (J2) is connected to a circulator (A10-A2) then to the input (J2) of the Feed Forward Cancellation Module (1555-1232) which generates the correction signal that will later be coupled with the RF output signal to cancel the distortion created in the 50-Watt Amplifier (1512-1107).

The main output of this module is fed to the 50-Watt Amplifier Module (1512-1107) input. The signal enters the module at J1 and is amplified by GaAs FET Q101 (FLL200IB-3). Then the signal is split four ways by three Wilkinson in phase couplers and amplified by GaAs FET amplifiers Q201, Q301, Q401, and Q501 (all FLL200IB-3's). The signal is then combined by three Wilkinson in phase couplers and fed to the output of the module at jack J2. The output is fed to a Circulator Kit (A50), then to the RF input of the Feed Forward Correction Module (1555-1248 or 1555-1250) where it will be coupled with the correction signal.

The DC biasing of each FET within the module is controlled and filtered by the corresponding daughter boards (D1, D2, D3, D4, and D5), which are soldered directly to the motherboard. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

A 20 dB micro-strip coupler located within the 50-Watt Amplifier Module provides a uncorrected (distorted) sample of the RF signal. This uncorrected signal is fed to the signal plus distortion signal input (J1) of the Feed Forward Cancellation Module where it is shifted in phase (180°) and coupled with the undistorted input signal from the 3 Stage Driver Amplifier (A10-A1). Combining these two signals, the undistorted input signal, and the distorted, phase shifted (180°) RF output signal, cancels the information carrying component of the signal, leaving only the distortion of the RF output of the 50 Watt Amplifier Module at the output (J4).

This correction signal is shifted 180° in phase and fed to the input of a Three Stage Amplifier Module (A10-A2) where it is amplified to a sufficient level to cancel the distortion created by the 50 Watt Amplifier Module. The amplified correction signal at the output of this module (J2) and the RF output of the 50 Watt Amplifier Module are applied to the inputs of the Feed Forward Correction Module (1555-1231) where the signals are coupled together, effectively canceling the distortion in the output signal. The main output of the module (J5) is connected to the RF output jack (J10) on the rear of the tray. A sample of the RF output signal is taken using an internal micro-strip coupler. This sample provides a forward power sample of the RF output. A reflective power sample is provided by a circulator, (A50). Both samples are sent to the Dual Peak Detector Board (1512-1147), which detects each sample and produces a forward and reflected metering voltage, which drives the tray's front panel meter.

The Seven Section Bias Board (1555-1213) supplies the amplifier modules with both +10 VDC (operating voltage) and -5 VDC (bias voltage).

The Transmitter Control Board (1527-1215) provides the capability to control and monitor the operating status of the transmitter. The board is designed to protect the transmitter in the event of the following faults: over temperature, loss or reduction in output power and loss of the -5 VDC GaAs FET bias voltage. The Transmitter Control Board is interfaced with the SCADA (Supervisory Control and Data Acquisition) Board (1555-1215), which provides the capability to remotely control and monitor the transmitter status with a computer terminal via the Connector Assembly Board (1555-1237 or 1555-1238) jacks J16 and J17 at the rear of the tray.

The transmitter may be configured for either a 115 VAC/60 Hz or 230 VAC/50 Hz source. The AC source enters the tray at jack J1. The AC source passes through a line filter and is distributed to a terminal block (TB1). Varistors VR1, VR2, VR3 and VR4 provide transient and over voltage protection to the transmitter. The rear panel circuit breaker applies AC voltage to the input of the toroid transformer.

The toroid transformer provides (2) 15 VAC secondary windings. The first winding is sent to a full wave bridge rectifier which supplies a positive 18 VDC to several positive voltage regulators located on the DC Power Supply Board. The second winding is applied to the +12 VDC Power Supply Board which powers the 12 VDC cooling fan. The second winding is also applied to a full wave bridge rectifier circuit on the DC Power Supply Board whose output is sent to several negative voltage regulators. Two +12 VDC switching supplies (SPL250-1012) rated at 21 amperes are used to supply the GaAs FET amplifier modules with power.

System Operation

When the transmitter is placed in the "operate" mode, as set by the menu screen located on the front panel of the Upconverter/Amplifier assembly, the amplifier stage's power supply is enabled, the operate indicator on the front panel is lit and the DC OK on the front of the power supply should also be green.

When the transmitter is in standby, the amplifier stage's power supply is disabled, the operate indicator on the front panel and the DC OK on the power supply will be extinguished.

If the transmitter does not switch to "Operate" when the operate menu is switched to Operate, check that all faults are cleared.

The transmitter can be controlled by the presence of input signal. If the input signal to the transmitter is lost, the transmitter will automatically cutback and the input fault indicator will light. When the input signal returns, the transmitter will automatically return to full power and the input fault indicator will be extinguished.

8.5.1 Principles of Operation

Operating Modes

This transmitter is either operating or in standby mode. The sections below discuss the characteristics of each of these modes.

Operate Mode

Operate mode is the normal mode for the transmitter when it is providing RF power output. To provide RF power to the output, the transmitter will not be in mute. Mute is a special case of the operate mode where the power supply is enabled but there is no RF output power from the transmitter. This condition is the result of a fault condition that causes the firmware to hold the module in a mute state.

Operate Mode with Mute Condition

The transmitter will remain in the operate mode but will be placed in mute when the following fault conditions exists in the transmitter.

- The Upconverter is unlocked

Entering Operate Mode

Entering the operate mode can be initiated a few different ways by the transmitter Control/Monitoring board. A list of the actions that cause the operate mode to be entered is given below:

- A low on the Remote Transmitter Operate line.
- User selects "OPR" using switches and menus of the front panel.
- Receipt of an "Operate CMD" over the serial interface.

There are several fault or interlock conditions that may exist in the transmitter that will prevent the transmitter from entering the operate mode. These conditions are:

- Power Amplifier heat sink temperature greater than 78°C.
- Transmitter is muted due to conditions listed above.
- Power Amplifier Interlock is high indicating that the amplifier is not installed.

Standby Mode

The standby mode in the transmitter indicates that the output amplifier of the transmitter is disabled.

Entering Standby Mode

Similar to the operate mode, the standby mode is entered using various means. These are:

- A low on the Remote Transmitter Stand-By line.

Depressing the "STB" key on selected front panel menus.

- Receipt of a "Standby CMD" over the serial interface.

Operating Frequency

The Power detectors in the transmitter have been calibrated at their frequency of use. The detectors for System RF monitoring are also calibrated at the desired frequency of use.