7. PARTS LIST/TUNE-UP INFO

7.1 Parts List

The transmitter, can be subdivided as follows:

QAM Modulator Tray
Frequency Generator Tray
Upconverter/Amplifier Tray

7.2 Tune-up Information

In the following procedure, the complete transmitter is adjusted for optimum performance, beginning with the start up procedure of the Frequency Generator, followed by the Agile Upconverter and Broadband Amplifier, adjusting each circuit for its specified performance while observing the appropriate output parameters of the board or subassembly being adjusted.

Because of the broadband nature of most of the amplifier stages, this is a straightforward procedure, easily accomplished if base-band, IF, and RF test equipment is available. In this procedure, the input signals are first connected and each circuit is adjusted in sequence by connecting the test equipment to the specified point.

Equipment required:
1. Spectrum Analyzer
2. Multi-meter
3. Frequency Counter
4. 10 MHz Source

Note: Agile must be placed into standby to change channels. To place agile in standby press the button under "STBY" on the LCD.

7.2.1 Modulator Tray

Follow the step listed below to bring the CM720M modulator online.

1. Turn on the tray by connecting the AC power cable the unit and observing the front panel LEDs. The front panel lights flash through a consistent sequence when the unit is first powered on. When power-up is complete, the four seven-segment LEDs will illuminate, and the Fault LEDs will not illuminate.

2. Verify that the power-up message is displayed on the front panel LCD. If necessary, adjust the LCD contrast by pressing the increase/decrease buttons on the front panel.

3. Set the time/date.

4. Set the transmit power to -40 dBm to -50 dBm.

5. Confirm that transmit power is enabled.

6. Use the front panel to verify that the AQM mode is at the desired setting.

7. Use the front panel to verify that the scrambler, Reed-Solomon encoder,

interleaver, and differential encoder are all enabled.

At this point the CM720M modulator has been powered up and the output spectrum may be observed.

Using a spectrum analyzer verify the proper shape and center frequency (44 MHz) of the spectrum at the IF output port (J5). Verify that the power level corresponds to that set in step 4 above.

The modulator circuitry requires no user adjustments.

7.2.2 Frequency Generator Tray (Automatic Mode Operation)

7.2.2.1 4 Channel VCXO Board (1527-1403)

Each 4 Channel VCXO Board contains four identical circuits grouped by channels. The components for each channel within the group begin with the same number (example: C103 and L101 belong to oscillator A1 and C203 and L201 belong to oscillator A2). During this procedure the component number will begin with an "x". The operator must know in which oscillator section the desired oscillator is located.

1. Turn the rear panel circuit breaker to the "ON" position.
2. Remove the external 10 MHz reference from rear panel of the tray (J2).
3. Verify that the ribbon cable is connected from J8 of the PLL board to J9 of the Frequency Generator Control Board.
4. Set Frequency Generator Control SW1 - SW8 to the off position.
5. Set the jumper on J13 of the Frequency Generator Control Board to Automatic.
6. Set the jumper on J12 of the PLL Board to the operate position.
7. Set the jumper on J11 of the PLL Board to the operate position.
8. Adjust R39 for -3.0 VDC at TP4.
9. Set the jumper on J11 of the PLL Board to the normal position.
10. Select the desired channel with the front panel keys.
11. Remove the cover from the desired 4 Channel VCXO Module. Do not remove the RF Shield. All adjustments must be made with the shield on.
12. Monitor sample output jack of the board (J4) or module output jack (J1) with a spectrum analyzer set to the appropriate frequency and a span of 1 MHz.
13. Monitor the front panel sample with a frequency counter.
14. A display should be visible on the analyzer. IF not, slowly adjust Cx06 until the circuit begins to oscillate.
15. Peak the signal at J4 by adjusting Cx17, Lx01, Lx03.
16. Set the frequency of oscillation by adjusting Cx03.
17. The level at J4 should be approximately -10 dBm. The level at J1 should be +6 dBm. Verify that the level is adjustable with R123 and set the peak to the appropriate value.
18. Repeat steps 10-16 for all remaining oscillators. Try to set all output levels equal.

7.2.2.2 VHF Combiner Buffer Board (A9) 1527-1407

1. Select the lowest channel using the front panel push buttons.
2. Verify that the input is +6 dBm.
3. Reconnect J1. Connect the spectrum analyzer to J10. Adjust R16 for an output of +6 dBm.
4. With the analyzer connected to J10, repeat step 3 for at least one channel in each group.

5. Reconnect J10.

7.2.2.3 Broadband X4 Multiplier Board (A13-A1) 1527-1404

1. Select a middle band channel using the front panel keys.
2. Connect the spectrum analyzer to the output of the X4 Multiplier (J2). Set the frequency of the analyzer to the selected crystal X4. Set the span of the analyzer so the third and fifth harmonics are visible.
3. Peak the output with C4, C6, c10 and C12. The fourth harmonic should be approximately +4 dBm. Try to maximize the fourth harmonic while minimizing the third and fifth harmonics.
4. Reconnect J2.

7.2.2.4 PLL Board (A1) 1527-1402

1. Connect the 10 MHz reference to J2 on the rear panel.
2. Select the lowest channel.
3. After several seconds the PLL should lock. IF the PLL does not lock go to step 4.
4. Monitor U3 pin 28 with an oscilloscope.
5. Adjust R27 to narrow the pulse displayed on the oscilloscope (pulse amplitude will remain the same). Allow several second for the PLL to lock.
6. Connect the analyzer to J3. Set the analyzer frequency to the selected crystal X4. Verify that the PLL output is approximately +0.5 dBm.
7. Monitor the front panel sample with the frequency counter. Verify that the locked oscillator is on frequency.
8. Repeat steps 6 and 7 for each channel in each group.
9. Reconnect J3.

7.2.2.5 UHF I/P X4 Multiplier Board (A15-A1) 1128-1206

1. Using the front panel keys, select a channel in the middle of the band.
2. Connect the spectrum analyzer to the output of the multiplier (J2). Set the center frequency of the analyzer to the selected channel X16. Set the span of the analyzer such that the fourteenth and seventeenth harmonics are visible.
3. Peak the output using C4, c6, C10, and C12. The sixteenth harmonic should be approximately +4 dBm. Maximize the desired harmonic and diminish the adjacent harmonics.
4. Reconnect J2.

7.2.2.6 Filter Assembly (A16 and A18) 1128-1102

This filter has been factory tuned and should not be retuned unless attenuation is noticed at the band edges.

1. Using the tracking generator of the spectrum analyzer sweep the input of the filter with a frequency span sufficiently wide to view the 200 MHz bandwidth o the filter.

2. Adjust the three tuning capacitors located on the top of the filter assembly for a flat response.

3. Reconnect the output of the filter (J2).

7.2.2.7 L.O. Amplifier Module (A17) 1557-1213

This module uses a VNA-25 MMIC amplifier. No user adjustments are available within the module.

7.2.2.8 Switch Board (A12) 1527-1506

The Switch Board passes parallel data from the Frequency generator control Board or ABS Controller Board to the LCD display. This board also sets the back brightness of the LCD display. To set the back brightness of the display:

1. Place the jumper on J6 to the High position.
2. Adjust the front panel contrast potentiometer clock wise and counter clockwise to verify proper operation.

7.2.2.9 Frequency Generator Tray (Manual Mode Operation)

To verify manual operation of the Frequency generator tray, the 10 MHz reference must be connected.

1. Disconnect the ribbon cable from J9 of the Frequency Generator Control Board and connect it to J9 of the PLL Board.
2. Place the jumper on J13 of the Frequency Generator Control Board to the Manual position.
3. Place dip switches SW1-SW8 on the Frequency generator Control Board to ON.
4. Set the dip-switch SW1-1 to off (Frequency Generator Control Board).
5. Set the programmable divider on the PLL Board for oscillator one, crystal one.
6. Momentarily place the jumper on J12 of the PLL board from the center position (operate) then back to the center position.
7. Verify that the PLL locks.
8. Repeat this process for each installed VCXO.

7.2.3 Upconverter/Amplifier Tray

Using a spectrum analyzer verify the proper shape and center frequency (44 MHz) of the spectrum of the IF input signal to the Agile Upconverter.

Verify that the input power level is -11 dBm to -6 dBm (average).

Adjust a Network Analyzer for the following settings:

Center Frequency = 44 MHz
Span = 20 MHz
Markers set to 41 MHz, 44MHz, and 47 MHz
Channel 1
Transmission
Reference Level = 2.5 dB
Scale/div. = 0.2 dB
Channel 2
Delay
Scale/div. = 10nSec

7.2.3.1 IF Input Equalizer Board (A1) 1555-1219

Follow the steps below to align the IF Input Equalizer Board.

1. Place the on board jumpers to the positions indicated below:

Input Impedance Matching (75Ω)	W1 and W2 to pins 1 and 2 on J2 and J3.
Input Attenuators (LOW)	W3, W4, W5, and W6 to pins 1 and 2 on J4, J5, J6 and J7.
SAW Filter (OUT)	W7 and W8 to pins 1 and 2 of J8 and J9.
Delay Equalizers 1 and 2 (OUT)	W9, W10, W12, and W13 to pins 1 and 2 on J12, J13, J14, and J15.
Response Corrector (IN)	W15 and W16 to pins 1 and 2 on J17 and J18.

2. Connect the RF output of the Network Analyzer to the input of the board (J1).
3. Connect the RF input of the Network Analyzer to the output of the board (J19)
4. Preset Resistors R31, R33, and R35 fully CCW.
5. Turn R31 fully CW, tune C29 to place a notch at 40 MHz, turn R31 CCW.
6. Turn R33 fully CW, tune C30 to place a notch at 44 MHz, turn R33 CCW.
7. Turn R35 fully CW, tune C31 to place a notch at 48 MHz, turn R35 CCW.
8. Now adjust R31, R33, and R35 for ±0.1 dB response across the channel.
9. Place the SAW filter in the circuit by moving the jumpers on J8 and J9 to pins 2 and 3. The level will decrease about 3 dB.
10. Readjust for a ±0.1 dB response across the channel.
11. Remove the SAW filter from the circuit by moving the jumpers on J8 and J9 to pins 1 and 2.
12. Place Delay Equalizer 1 in circuit by moving jumpers on J11 and J12 to pins 2 and 3.
13. Remove jumper on J13 and tune L4 for a notch at 44 MHz, reinstall jumper on J13.
14. Tune L5 and C17 for a delay of 20 to 25 nSec from band edge (41 MHz), to the center frequency (44 MHz).
15. Remove Delay Equalizer 1 from the circuit by moving the jumpers on J11 and J12 to pins 1 and 2.
16. Place Delay Equalizer 2 in circuit by moving jumpers on J14 and J15 to pins 2 and 3.
17. Remove jumper J16, tune L6 for a notch at 44 MHz, reinstall jumper on J16.
18. Tune L7 and C23 for a delay of 25 to 30 nSec from band edge (41 MHz) to center frequency (44 MHz) (note: adjusting delay effects frequency response).
19. Remove Delay Equalizer 2 from the circuit by moving jumpers on J14 and J15 to pins 1 and 2.
20. Place the Saw filter in circuit by moving jumpers on J8 and J9 to pins 2 and 3, then readjust frequency response.
21. Connect the modulated signal from the CM720M Modulator to the IF input on the rear of the tray (J2).
22. Connect the input to the board (J1) and check the output level at J19 with the spectrum analyzer. The level should be -11 to -6 dBm (average).
23. Reconnect the output of the board at J19.

7.2.3.2 ALC/AGC Board (A5) 1555-1216

1. Verify that the input level to J1 of the board to be -11 to -6 dBm (average).
2. Set jumpers J12 and J13 to the High Gain Position, pins 1 and 2.
3. Remove the harness from J10 (Mute).
4. Move jumpers on J4 and J11 to the Manual position (pins 1 and 2).

5. Using a DVM, set TP1 for 4 VDC using R25 (Manual ALC Adjust).
6. Using a DVM, set TP11 for 4 VDC using R105 (Manual AGC adjust).
7. Using a Network Analyzer, sweep the circuit from the input (J1) to the Loop Out (J2) at a center frequency of 44 MHz and a span of 50 MHz.
8. Tune (Filter 1) C2, C3, C4, L2, and L4 for an in-channel response of ±0.1 dB and a response of ±0.2 dB 9 MHz from the upper and lower channel edges. This section should exhibit approximately a 1 dB gain factor.
9. Using a Network Analyzer, sweep the circuit from the Loop In (J7) to the output of the board (J8).
10. Turn R125 fully CW, tune C69 to place a notch at 40 MHz, turn R125 CCW.
11. Turn R126 fully CW, tune C70 to place a notch at 44 MHz, turn R126 CCW.
12. Turn R127 fully CW, tune C71 to place a notch at 48 MHz, turn R127 CCW.
13. Tune (Filter 2) C39, C40, and C41 for a response of ±0.1 db across the channel. Note: This section should exhibit approximately an -5 dB Gain factor.
14. Adjust Manual Gain Potentiometer (R25) to achieve a level of -8 dBm at J2 (Loop Out), with a modulated input.

The signal is looped out at J2 to the Linearity Equalizer Board input (J1).

7.2.3.3 Linearity Equalizer Board (A2) 1555-1220

1. Disable the correction by switching S1 to Disable.
2. Adjust R3 and R13 fully CCW.
3. Adjust R23 fully CW.
4. Adjust R13 to achieve -8 dBm (average) at J2.

The output of the Linearity equalizer Board (J2) is fed to the input of the Phase Corrector Board (J1).

7.2.3.4 Phase Corrector Board (A3) 1555-1244

1. Adjust all Potentiometers fully CCW, move jumper on J9 to Disable, jumper on J10 to the right, jumper on J9 to the rear, and jumper on J8 to the left.
2. The output of the board should be about -15 dB (average).

The output (J4) is connected to the Loop In (J7) of the ALC/AGC Board.

7.2.3.5 ALC/AGC Board (A5) 1555-1216

1. With a modulated signal present, adjust R80 for a voltage of -1.0VDC at TP10.
2. Measure the voltage at TP9. This voltage should be about +1.0VDC.
3. Adjust ALC REF Potentiometer R31 fully CCW.
4. Move jumper on J4 to the ALC position and adjust R31 for -1.0VDC at TP10.
5. Adjust AGC REF potentiometer R88 fully CCW.
6. Connect the Spectrum Analyzer to the output of the board (J8) and adjust Manual Gain potentiometer R105 for -18 dBm (average).
7. Move jumper on J4 to the Manual position.
8. With the Network Analyzer adjusted for a span of 50 MHz, sweep the ALC/AGC Board from the IF input (J1) to the IF output (J8). Adjust R125, R126 and R127 for an in-band frequency response of ±0.1 dB and an out-of-band frequency response of ±0.2 dB.
9. Reconnect the harness to the IF Input jack (J1) and the IF Output jack (J8).

7.2.3.6 VHF Generator Control Board (A14) 1555-1214

1. Disconnect the PLL reference frequency by removing the plug at J5 and/or J6.

2. Connect a digital voltmeter between TP4 (+) and ground (-). Adjust the manual bias potentiometer (R87) for a reading of -3 VDC at TP4.

3. Connect a frequency counter to J11 to measure the VHF frequency (if frequency adjustments are necessary, follow the above procedure for the UHF Generator board).

4. Set PLL programming per required channel frequency.

5. Connect an oscilloscope between pin 28 of U2 or TP9 (+) and ground (-).

6. Reconnect the plugs at J5 and/or J6 and minimize the spike amplitude that will be observed on the oscilloscope using the phase detector balance potentiometer R70.

PROGRAMMING CHART FOR PLL BOARD (1527-1402)

BRS/EBS CHANNEL NUMBER	CHANNEL CARRIER (MHz)	F_{VCXO} = (F_V-539)/4 (MHz)	L.O. (MHz)	(ON = 0) (S1) 1234	(S2) 1234	(S3) 1234	(S4) 1234
A4	2575.00	127.250	2036	1100	1111	0100	0001
B4	2581.00	127.625	2042	1100	1111	1100	0010
C4	2587.00	128.000	2048	0010	0000	0000	0000
D4	2593.00	128.375	2054	0010	0000	0000	0011
G4	2599.00	128.750	2060	0010	0000	1000	0001
F4	2605.00	129.125	2066	0010	0000	0100	0010
E4	2611.00	129.500	2072	0010	0000	1100	0000

NOTE: ON SWITCHES S1-(1-4), S2-(1-4), S3-(1-4), AND S4-(1-4), "ON" EQUALS 0.

7.2.3.7 UHF Generator Board (A15-A1) 1512-1101

1. Connect the main output from the channel oscillator section of the UHF Generator Board (J1) to a spectrum analyzer, tuned to the crystal frequency and peak the tuning capacitors C6 and C11 for maximum output. Tune L3 and L2 for maximum output. The output level should be +5 dBm ±2 dB.

While monitoring with a DVM, maximize each of the following test point voltages by tuning the broadband multipliers in sequence.

2. Monitor TP1: Tune C32 for maximum (Typical 0.6 VDC).
   Monitor TP2: Tune C34 and C38 for maximum (Typical 1.2 VDC).
   Monitor TP3: Tune C40 and C44 for maximum (Typical 2.0 VDC).
   Monitor TP4: Tune C46 for maximum.
   Monitor TP4: Re-peak C38, C40, C44 and C46 (Typical 3.5 VDC).

3. Connect a spectrum analyzer, tuned to 8 times the crystal frequency, to the UHF Generator output (J3). Monitor the output while peaking the tuning capacitors for maximum output.

4. The output level at J2 should be +15 dBm ±2 dB.

7.2.3.8 UHF Filter (A6) 1007-1101

This filter has been factory tuned and should not be tuned without proper equipment. The filter has a typical loss of approximately 4 dB. The output of the filter is sent to L.O. input of the first double balanced mixer (A4).

7.2.3.9 L.O. Amplifier Module (A34) 1557-1213

This module uses a VNA-25 MMIC amplifier and provides a gain of approximately +9 dBm. No user adjustments are available within the module.

7.2.3.10 4 Pole UHF Filter (A7) 2005-1047

The input to this filter is the 2nd IF output signal of the first double balanced mixer (A4). This filter has been factory tuned and should not be tuned without proper equipment. The filter has a typical loss of approximately 1 dB. The output of the filter is sent to the input of the Amplifier Module (A8).

7.2.3.11 Amplifier Module (A8) 1527-1213

This module amplifies the 2nd IF signal using a VNA-25 MMIC amplifier and provides a gain of approximately +6 dBm. No user adjustments are available within the module.

7.2.3.12 L.O. Amplifier Module (A16) 1557-1213

This module is identical to the L.O. Amplifier Module above and uses a VNA-25 MMIC amplifier providing a gain of approximately +9 dBm to the RF output signal of the second double balanced mixer (A13). No user adjustments are available within the module.

7.2.3.13 Three-Section Broadband Filter (A17) 1107-1101

This filter has been factory tuned and should not be tuned without proper equipment. The filter has a typical loss of approximately 2 dB. The output of the filter is sent to a circulator then to the input of the 3-Stage Amplifier Module.

7.2.3.14 Three-Stage Amplifier Module (A10-A1) 1516-1108

This amplifier does not contain any RF tuning adjustments. The module contains three cascaded broadband GaAsFET amplifier stages (FLL101ME driving a FLL351ME driving a FLL2001-3) providing a nominal gain of 36 dB. The operating current for each device (Q101, Q201, Q301) is controlled by a pot mounted on a bias board within the module and can be set by measuring the voltage drop across the across the .05 ohm resister (R1) on the Seven Section Bias Protection Board (A20) for Q301, and the voltage drops across R14, and R15 (0.22Ω) on the Drain Daughter Board (1516-1114) for Q101 and Q201 respectfully.

1. With no RF signal applied and with the transmitter off, unsolder the drain leads located near the ferrite beads of Q201 and Q301 on the drain Daughter Board (1516-1120). Connect a digital voltmeter across R14 on the drain Daughter Board. Apply AC power to the transmitter and place the transmitter into the Operate mode.

2. Adjust the bias control (R103) for a reading of .04V across R14 on the drain Daughter Board (1516-1120). This voltage represents a bias current of .18 amps on Q101.

3. Place the transmitter into the standby mode and then turn the transmitter off. Unsolder the drain lead of Q101 and re-solder the drain lead of Q201. Apply AC power to the transmitter and place the transmitter into the Operate mode. Adjust the bias control (R203) for a reading of .16V across R15 on the drain Daughter Board. This voltage represents a bias current of .720 amps on Q201.

4. Place the transmitter into the standby mode and then turn the transmitter off. Re-solder the drain leads of Q101 and Q301. Apply AC power to the transmitter and place the transmitter into the Operate mode. Adjust the bias control potentiometer R303 for a reading of .24V across R1 on the Seven Section Bias Protection Board. This represents a bias current of 4.8 amps on Q301.
   The output of this amplifier is fed to a circulator then to the Feed Forward Correction Module (A13).

7.2.3.15 Feed Forward Cancellation Module (A33) 1555-1232

The Feed Forward Cancellation Module inputs the undistorted output of the 3 Stage Driver Amplifier (A10-A1), phase shifts the signal (180°), and couples it with a sample output from 50 Watt Amplifier (A10-A3) canceling the information carrying component of the signal leaving only the distortion of the 50 Watt Amplifier at the output the module (J4). This distortion cancellation signal is fed to the input of the 3-stage Correction Amplifier (A10-A2).

7.2.3.16 Three-Stage Correction Amplifier (A10-A4) 1516-1108

The Three Stage Correction Amplifier amplifies the distortion cancellation signal to a

suitable level to cancel the distortion in the output of the 50-Watt Amplifier (A10-A3). The output signal (J2) is fed to the correction input (J2) of the Feed Forward Correction Module (A13). For alignment of this module see the Three Stage amplifier Module (A10-A1) alignment procedure above (substitute R2 for R1 on the Seven Section bias Protection Board when setting the bias for Q101 in the above procedure).

7.2.3.17 50-Watt Amplifier Module (A10-A3) 1512-1107

This Amplifier module does not contain any RF tuning adjustments. The module contains two cascaded broadband GaAs FET amplifier stages (FLL200-3 driving four parallel FLL200-3 's) providing a nominal gain of 18 dB. The operating current for each device (Q101, Q201, Q301, Q401,and Q501) is controlled by a pot mounted on a bias board within the module, next to each corresponding FET, and can be set by measuring the voltage drop across the .05 Ω resistors (R3, R4, R5, R6, and R43) on the bias protection board. See chart below.

GaAs FET Transistor	Potentiometer Adjustment	Bias Protection Board Resistor	Voltage Across Bias Protection Resistor	Drain Current Calculated
Q101	R902	R3	.24	4.8
Q201	R802	R4	.24	4.8
Q301	R902	R5	.24	4.8
Q401	R802	R6	.24	4.8
Q501	R902	R43	.24	4.8

The output of this amplifier is sent through a circulator (A50), then to the RF input jack (J1) of the Feed Forward Correction Module (A13).

The voltages needed to operate the amplifier modules are provided by the +12V/21 amp switching supplies (A9 and A10) and the ±12VDC Power Supply Board (A26), which produces the -5VDC bias voltage.

The -5VDC supply is non-adjustable with a regulated output. To prevent damage to the GaAs FET amplifiers, the +12VDC Supplies will not turn on until the -5VDC bias supply is operating.

The +12VDC/21 amp switching, regulated power supplies do not require any adjustment.

7.2.3.18 Seven Section Bias Protection Board (A20) 1555-1213

This board does not contain any RF tuning adjustments. Indicators DS1, DS2, DS3, DS4, DS5, DS6, and DS7 will illuminate if the amplifier circuits are operating correctly with normal biasing and operating voltages.

7.2.3.19 ALC/AGC Board (A5) 1555-1216

1. Connect an RF Power Meter to the RF output jack (J10) on the rear of the tray.
2. Place the jumper on J4 to the Manual ALC position (pins 1 and 2).

3. Place the jumper on J11 to the Manual AGC position (pins 1 and 2).
4. Adjust Manual Gain potentiometer R105 for the rated output power on the Power Meter (15 watts average).
5. Move jumper on J4 to the ALC position (pins 2 and 3).
6. Move jumper on J11 to the AGC position (pins 2 and 3).
7. Adjust AGC Reference potentiometer R88 for the rated output power on the Power Meter.

7.2.3.20 Dual Peak Detector Board (A22) 1555-1264

With the front panel selector switch in the Driver O/P Power position, adjust Metering Adjust potentiometer R23 for 100% on the front panel meter. Note: A front panel meter reading of 100% indicates a tray output power of 10 Watts (average). When driving an amplifier, the output power will be reduced to typically 20 - 40%.

7.2.3.21 Dual Peak Detector Board (A55) 1555-1264

With the front panel selector switch in the Combined O/P Power position, adjust Metering Adjust potentiometer R35 for 100% on the front panel meter. Note: A front panel meter reading of 100% indicates a system output power of 50 Watts (average).