

RF10K User manual

The RF10K is a 902-928 MHz FM transceiver Module.

There are NO user adjustable or serviceable parts inside. The transceiver is shipped fully adjusted from the factory.

There is a nine pin connector accessible by the user. Pin one (1) is the pin closest to the edge of the unit. The nine (9) pins are named and have the following functions:

Pin	Name	Description
1)	AF	Analog received signal out, 0.6 Volts Peak to Peak
2)	SQ	Receive signal present, active High
3)	CLK	Clock signal, used to clock in DATA for the internal PLL
4)	DATA	Data that is clocked in with the CLK line
5)	LE	Latch Enable control signal for the CLK and DATA lines
6)	+V	Power, +3.3 Volt input +/- 5%
7)	GND	Signal and power Ground
8)	TX	Turns on/off the transmission section of transceiver, active high
9)	MOD	Analog signal for FM transmission, typical 0.3 V Peak to Peak

Power must be applied to the unit before the PLL can be programmed.

After power is applied the LE signal can be lowered, and then PLL data is clocked into the transceiver unit to set the TX and RX frequencies. Data is latched on the clock rising edge.

The PLL data consist of three 21 bit sequences. First the reference divider of the PLL is loaded with the following 21 bits of data, in HEX MSB first:

0x17 0xE0 0x8A

Following this the RX and TX PLL dividers are loaded, with 21 bit of data, in HEX MSB first:

0x14 0x55 0x1A RX PLL frequency load

0x02 0x48 0x13 TX PLL frequency load

The LE signal must be asserted after each 21 bit sequence of Data.

After loading the PLL data, the TX signal may be asserted. Internal circuitry prevents the TX section on the Transceiver from powering up, until the PLL has been loaded with proper data and has locked on the correct TX frequency in the 902-928 MHz band. There

is a DUAL SAW Filter (FT501) which prevents out of band signals from being transmitted or received by the RF10K.

The SQ pin will go high, and analog received signal will be present on the AF pin if a RF signal is present. Analog signals fed into the MOD line will be transmitted after the internal PLL has locked, and the TX line is asserted.