

C-8249 (915MHz FCC) TECHNICAL DESCRIPTION

A. CIRCUIT DESCRIPTION

1. The equipment is wireless weather forecast station ,the outdoor data from 915MHz frequency FSK receiver ,reception cycle every 5 seconds in each channel and the 915MHz RF-IC is all programmable and no alignment required in production ,the receive frequency very stable .
2. The equipment power up full display then the micro controller setting RF IC and read the digital pressure sensor data and indoor temperature & humidity data ,during the power up after 8 seconds to 60 seconds is 915MHz RX test mode , after power up 68 seconds radio controlled receiver power on.

B. MAIN COMPONENT DESCRIPTION

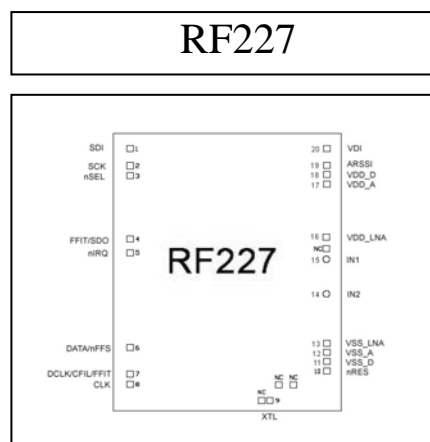
SYMBOL	COMPONENT	NAME	DESCRIPTION
X4	10MHz	Crystal	Stable RF transmitter Oscillator frequency and other.
X1	32.768kHz	Crystal	Provide reference clock 1 for MCU.
X5	3.58MHz	Crystal	Provide reference clock 2 for MCU.
X3	60.000kHz	Crystal	Radio controlled clock receiver crystal
	Buzzer	Buzzer	alarm sound output
U1	TM8959	MCU (micro controller unit)	Temperature and Humidity and air pressure and weather forecast icon and moon phase and air pressure bar calculate. Radio controlled clock and outdoor temperature and humidity data decoding .
U2	CME6005	Radio controlled clock receiver	Provide radio controlled clock data for micro controller unit
P03	P03	Pressure sensor	Provide air pressure data for MCU
HH1	CL-HQM3R	Humidity sensor	Provide Humidity data for MCU
TT1	RB103FS3435F01	Temperature sensor	Provide temperature data for MCU
LCD902	LCD902	LCD	Display in/out door temperature and clock .
U6	RF 227	RF IC	Receive outdoor 915MHz transmitter temperature
U7	MD7336	Regulator	Stable 3.6 voltage for RFIC operating
U8	CS5333	Regulator	Stable 3.3 voltage for MCU operating
	Loop antenna	Loop antenna	915MHz band reception antenna
L1	Ferrite antenna	Ferrite antenna	Radio control clock reception 60kHz ferrite antenna

CHUNG'S ELECTRONIC CO.,LTD	
Name	TECHNICAL DESCRIPTION
Model	C8249(FCC)915
File No	RX8249(915)
Date	26-7-10
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Universal ISM Band FSK Receiver RF227

DESCRIPTION:

Hope's RF227 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 315, 433, 868, and 915 MHz bands. Used in conjunction with Hope's FSK transmitters, the RF227 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation.

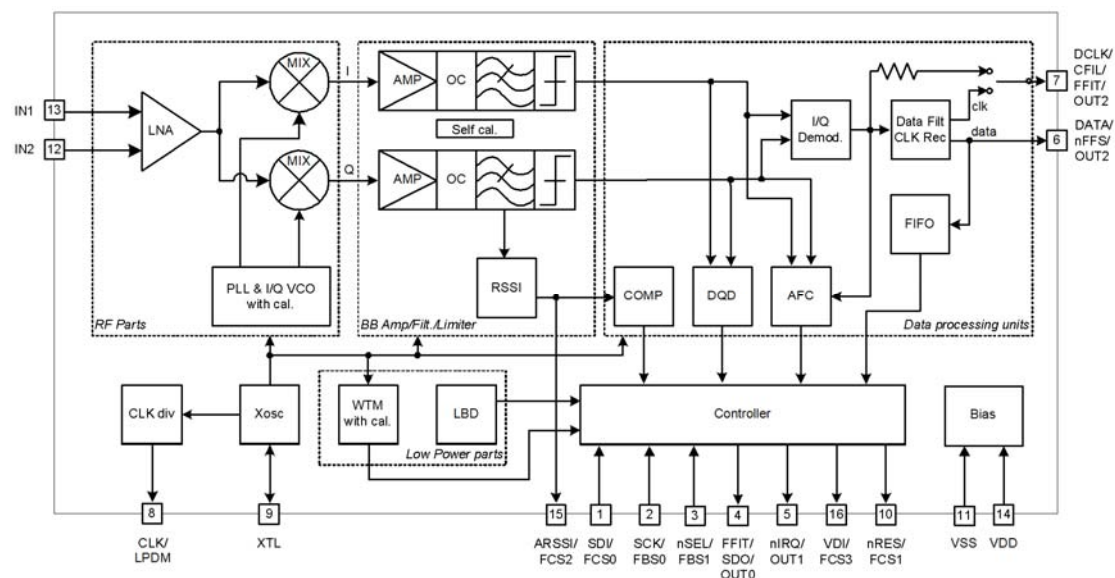


The RF227 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multi-path fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements. The receiver employs the Zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The RF227 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

For low power applications, the device supports low duty-cycle operation based on the internal wake-up timer.

BLOCK DIAGRAM



FEATURES:

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input
- Programmable baseband bandwidth (67 to 400 kHz)
- Analog and digital RSSI outputs
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 16 bit RX data FIFO
- Low power duty-cycle mode (less than 0.5 mA average supply current)
- Standard 10 MHz crystal reference
- Wake-up timer
- Low battery detector
- 2.2 to 5.4 V supply voltage
- Low power consumption (~9 mA in low bands)
- Low standby current (0.3 μ A)

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED DESCRIPTION

General

The RF227 FSK receiver is the counterpart of the Hope's FSK transmitter. It covers the unlicensed frequency bands at 315, 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The RF227 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. Calibration always occurs when the synthesizer begins. If temperature or supply voltage changes significantly, VCO recalibration can be invoked easily. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

LNA

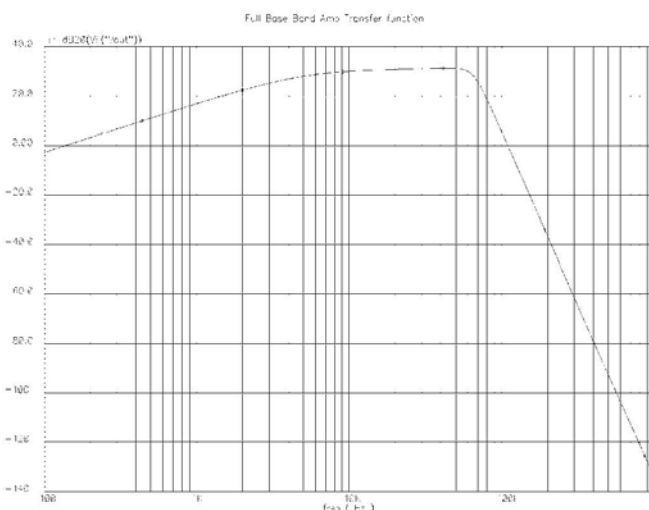
The LNA has 250 Ohm input impedance, which works well with the recommended antennas.

If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, -6, -14, -20 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received. An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at $2 \times BW$ frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 7 kHz.



Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation:

The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

Digital operation:

The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

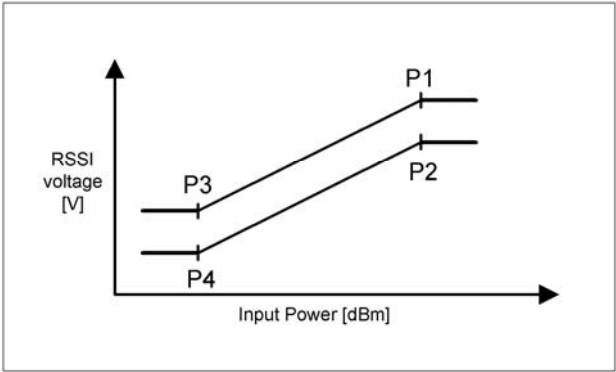
Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

Voltage on ARSSI pin vs. Input RF power

P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV



DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bit rate, there should be four transitions during a single one bit period in the I/Q signals. As the bit rate decreases in comparison to the deviation, more and more transitions will happen during a bit period.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a fixed number (128) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 μ A typical) and can be programmed from 1 ms to several days with an accuracy of $\pm 5\%$.

It calibrates itself to the crystal oscillator at every startup, and then at every 30 seconds. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by several wake-up events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

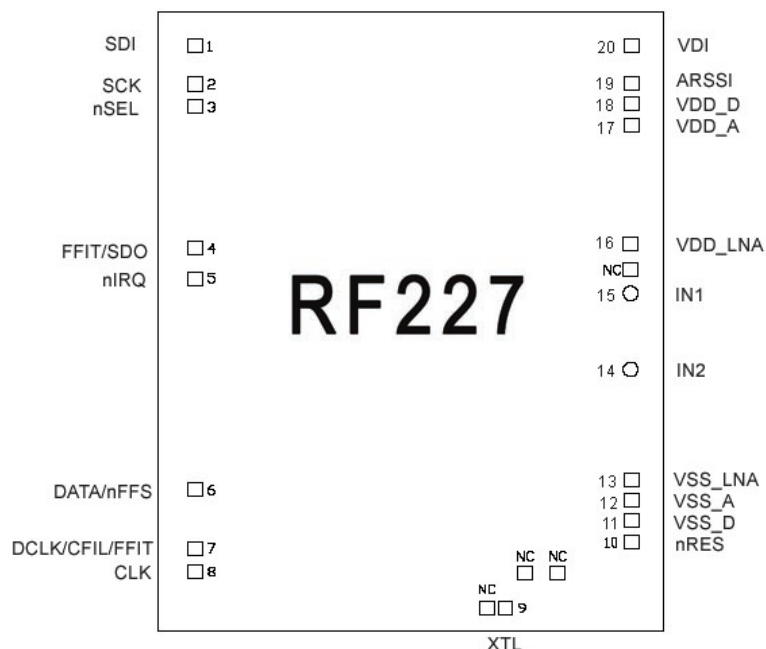
If any wake-up event occurs, the wake-up logic generates an interrupt signal which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 16bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the fe bit to 1 in the Output and FIFO Mode Command.

PACKAGE PIN DEFINITIONS

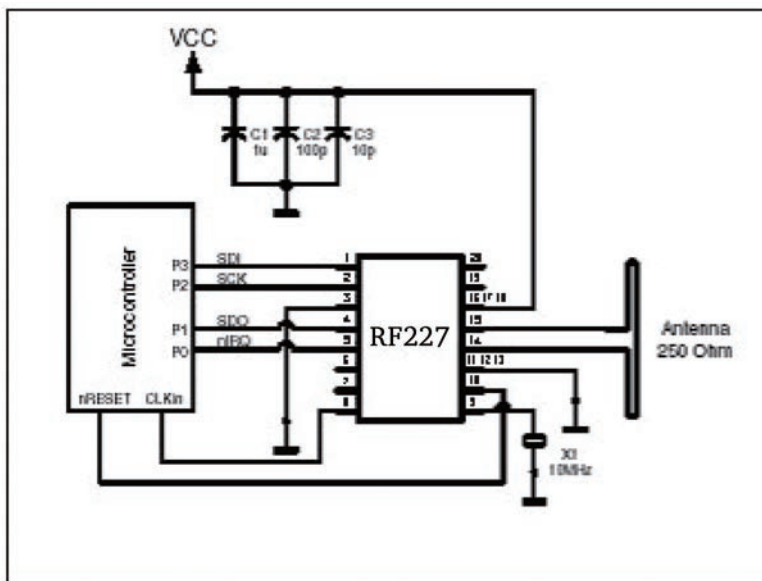
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



Pin	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of three-wire control interface (active low)
4	FFIT/SDO	DO	FIFO IT (active low) or serial data out for Status Read Command. Tristate with bushold cell if nSEL=H
5	nIRQ	DO	Interrupt request output, (active low)
6	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input
7	DCLK	DO	Received data clock output (Digital filter used, FIFO not used)
	CFIL	AIO	External data filter capacitor connection (Analog filter used)
	FFIT	DO	FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to one
8	CLK	DO	Clock output for the microcontroller
9	XTL/REF	AIO	Crystal connection (other terminal of crystal to VSS) / External reference input
10	nRES	DO	Reset output (active low)
11	VSS_D	S	Digital VSS(connect to VSS)
12	VSS_A	S	Analog VSS(connect to VSS)
13	VSS_LNA	S	LNA VSS(connect to VSS)
14	IN2	AI	RF differential signal input
15	IN1	AI	RF differential signal input
16	VDD_LNA	S	Positive supply voltage

17	VDD_A	S	Analog VDD(connect to VDD)
18	VDD_D	S	Digital VDD(connect to VDD)
19	ARSSI	AO	Analog RSSI output
20	VDI	DO	Valid Data Indicator output

Typical Application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{SS} , the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V _{dd}	Positive supply voltage	-0.5	6.0	V
V _{in}	Voltage on any pin	-0.5	V _{dd} +0.5	V
I _{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T _{st}	Storage temperature	-55	125	°C

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V _{dd}	Positive supply voltage	2.2	5.4	V
Top	Ambient operating temperature	-40	85	°C

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions: $T_{op} = 27\text{ }^{\circ}\text{C}$;

$V_{dd} = 2.7 \text{ V}$)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{dd}	Supply current	315 and 433 MHz bands 868 MHz band 915 MHz band		9 10.5 12	11 12.5 14	mA
I_{pd}	Standby current	All blocks disabled		0.3		μA
I_{lb}	Low battery voltage detector current consumption			0.5		μA
I_{wt}	Wake-up timer current consumption (Note 1)			1.5		μA
I_x	Idle current	Crystal oscillator and base-band parts are ON		3.0	3.5	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{lba}	Low battery detection accuracy			± 3		%
V_{il}	Digital input low level				$0.3 \cdot V_{dd}$	V
V_{ih}	Digital input high level		$0.7 \cdot V_{dd}$			V
I_{il}	Digital input current	$V_{il} = 0 \text{ V}$	-1		1	μA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, $V_{dd} = 5.4 \text{ V}$	-1		1	μA
V_{ol}	Digital output low level	$I_{ol} = 2 \text{ mA}$			0.4	V
V_{oh}	Digital output high level	$I_{oh} = -2 \text{ mA}$	$V_{dd} - 0.4$			V

Note: Using the internal wake-up timer and counter reduces the overall current consumption, which should permit approximately 6 months operation from a 1500mAh battery.

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Receiver frequency	315 MHz band, 2.5 kHz resolution 433 MHz band, 2.5 kHz resolution 868 MHz band, 5.0 kHz resolution 915 MHz band, 7.5 kHz resolution	310.24 430.24 860.48 900.72		319.75 439.75 879.51 929.27	MHz
BW	Receiver bandwidth	mode 0 mode 1 mode 2 mode 3 mode 4 mode 5	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	kHz
BR	FSK bit rate	With internal digital filters			115.2	kbps
BRA	FSK bit rate	With analog filter			256	kbps
P_{min}	Receiver Sensitivity	BER 10^{-3} , BW=67 kHz, BR=1.2 kbps (Note 1)		-109	-100	dBm
AFC_{range}	AFC locking range	δf_{FSK} : FSK deviation in the received signal		$0.8 \cdot \delta f_{FSK}$		
$IIP3_{inh}$	Input IP3	In band interferers in high bands		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers $f - f_{LO} > 4 \text{ MHz}$		-18		dBm
$IIP3_{inl}$	IIP3 (LNA –6 dB gain)	In band interferers in low bands		-15		dBm
$IIP3_{outl}$	IIP3 (LNA –6 dB gain)	Out of band interferers $f - f_{LO} > 4 \text{ MHz}$		-12		dBm

CCR	Co-channel rejection	BER=10 ⁻² with continuous wave interferer in the channel		-7		dB
ACS	Adjacent channel selectivity	BER=10 ⁻² with continuous wave interferer in the adjacent channel, mode 0, channels at 134 kHz, BR=9.6 kbps, δf_{FSK} =30 kHz		23		dB
P _{max}	Maximum input power	LNA: high gain	0			dBm
R _{in}	RF input impedance real part (differential) (Note 2)	LNA gain (0, -14 dB) LNA gain (-6, -20 dB)		250 500		Ohm
C _{in}	RF input capacitance			1		pF
RS _a	RSSI accuracy			+/-5		dB
RS _r	RSSI range			46		dB
C _{ARSSI}	Filter capacitance for ARSSI		1			nF
RS _{step}	RSSI programmable level steps			6		dB
RS _{resp}	DRSSI response time	Until the RSSI output goes high after the input signal exceeds the pre-programmed limit. CARRSI=5nF		500		μs

Note 1: See the BER diagrams in the measurement results section for detailed information.

Note 2: See matching circuit parameters and antenna design guide for information.

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f _{ref}	PLL reference frequency	(Note 3)	8	10	12	MHz
f _{res}	PLL frequency resolution	Depends on selected bands	2.5		7.5	kHz
t _{lock}	PLL lock time	Frequency error < 1kHz after 10 MHz step		20		us
t _{st, P}	PLL startup time	With running crystal oscillator			250	us
C _{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t _{POR}	Internal POR pulse width (Note4)	After V _{dd} has reached 90% of final value		50	100	ms
t _{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms			5	ms
t _{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.08	ms
t _{wake-up}	Programmable wake-up time		1		5*10 ¹¹	ms
C _{in, D}	Digital input capacitance				2	pF
t _{r, f}	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 3: Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

Note 4: During this period, commands are not accepted by the chip.

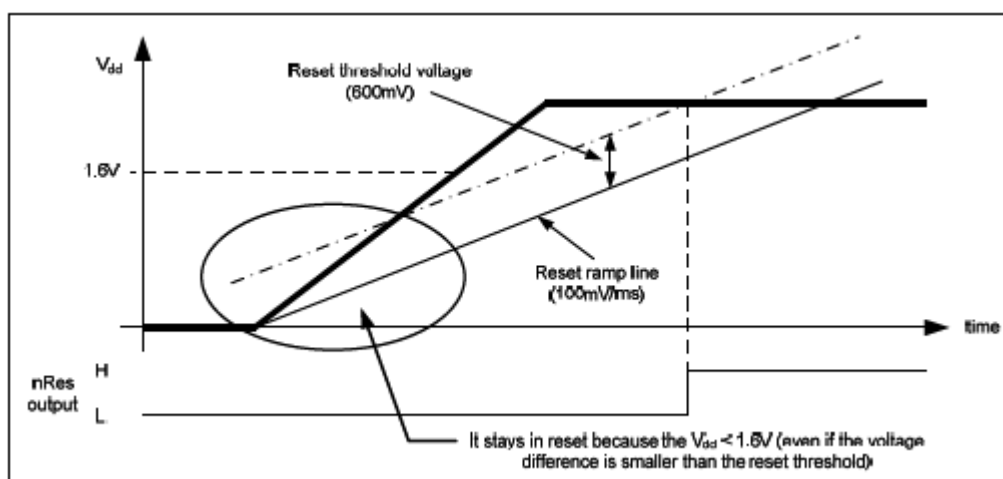
To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

Power-on reset

After power up the supply voltage starts to rise from 0V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V_{dd} and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the V_{dd} voltage is less than 1.6V (typical) the chip stays in reset mode regardless the voltage difference between the V_{dd} and the internal ramp signal. The reset event can last up to 150ms supposing that the V_{dd} reaches 90% its final value within 1ms. During this period the chip does not accept control commands via the serial control interface.

Power-on reset example:



Power glitch reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see *Related control commands* at the end of this section). In normal mode the power glitch detection circuit is disabled.

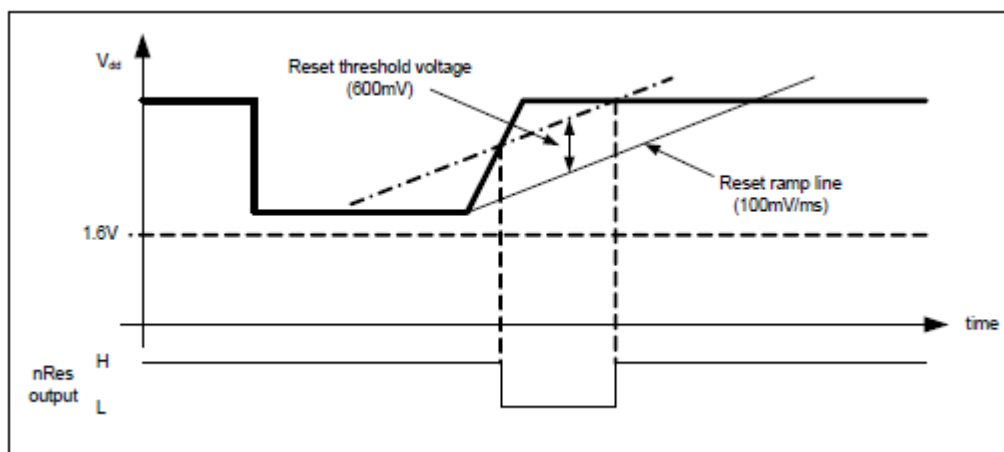
There can be spikes or glitches on the V_{dd} line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the V_{dd} has a rising rate greater than 100mV/ms and the voltage difference between the internal ramp signal and the V_{dd} reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the V_{dd} level reaches the reset threshold voltage (250mV in normal mode, 1.6V in sensitive reset mode).

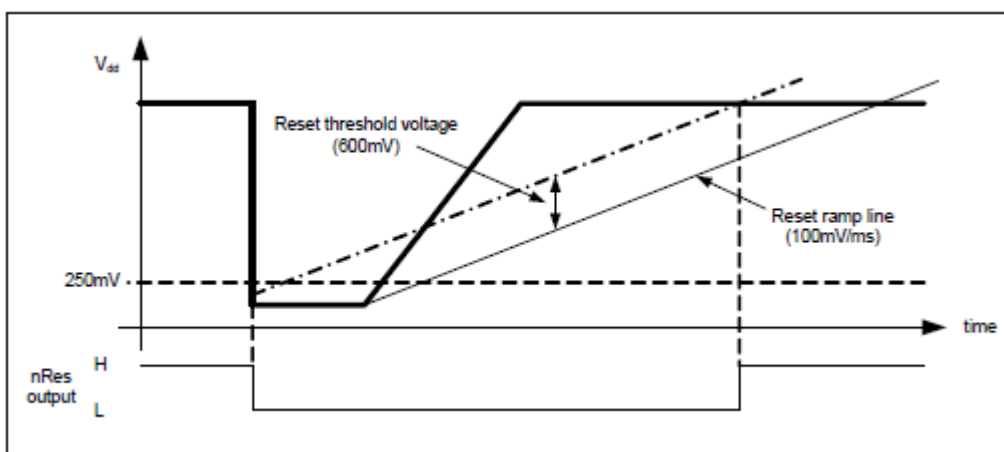
If the sensitive mode is disabled and the power supply turned off the V_{dd} must drop below 250mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

Sensitive Reset Enabled, Ripple on V_{dd} :



Sensitive reset disabled:



Software reset

Software reset can be issued by sending the appropriate control command (described at the end of the section) to the chip. The result of the command is the same as if power-on reset was occurred. When the $nRES$ pin connected to the reset pin of the microcontroller, using the software reset command may cause unexpected problems.

V_{dd} line filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command) it is very important to keep the V_{dd} line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below 10mV_{p-p} in the DC – 50kHz range for 200ms from V_{dd} ramp start.. Typical example when a switch-mode regulator is used to supply the radio, switching noise may be present on the V_{dd} line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

Related control commands

“Reset Mode Command”

Setting bit<0> to high will change the reset mode to normal from the default sensitive.

“SW Reset Command”

Issuing FF00h command will trigger software reset. See the Wake-up Timer Command.

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RF227 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps		Transmitter Deviation [+/- kHz]						
		30	60	90	120	150	180	210
	315 MHz	30	75	100	100	100	100	100
	433 MHz	20	50	75	100	100	100	100
	868 MHz	10	25	40	60	75	100	100
	915 MHz	10	25	40	50	75	75	100

Bit Rate: 9.6kbps		Transmitter Deviation [+/- kHz]						
		30	60	90	120	150	180	210
	315 MHz	25	70	100	100	100	100	100
	433 MHz	15	50	75	100	100	100	100
	868 MHz	8	25	40	60	75	75	100
	915 MHz	8	25	40	50	70	75	100

Bit Rate: 38.3kbps		Transmitter Deviation [+/- kHz]						
		30	60	90	120	150	180	210
	315 MHz	don't use	30	75	100	100	100	100
	433 MHz	don't use	20	50	75	100	100	100
	868 MHz	don't use	10	30	40	60	75	100
	915 MHz	don't use	10	25	40	60	75	75

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The

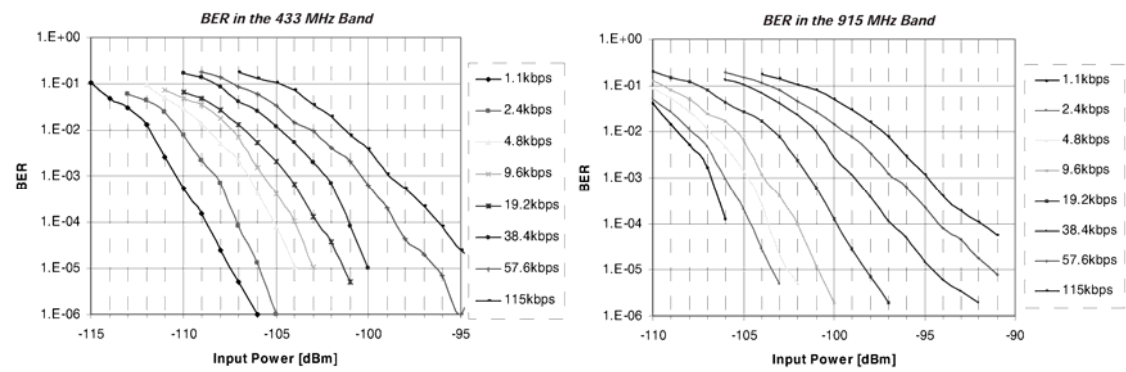
“pull-ability” of the crystal is defined by its motional capacitance and C_0 .

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

MEASUREMENT RESULTS

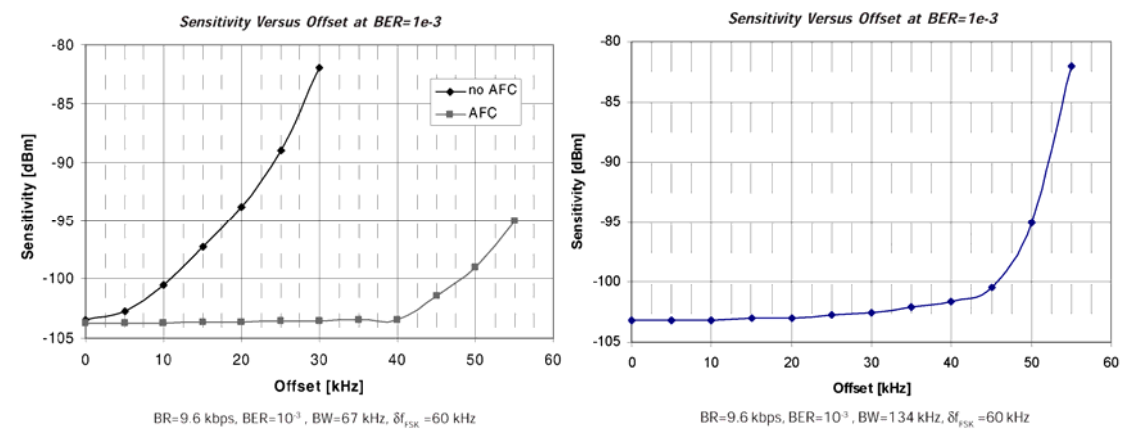
BER Measurement Results



1.134 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115 kbps
BW=67 kHz	BW=67 kHz	BW=67 kHz	BW=67 kHz	BW=67 kHz	BW=134 kHz	BW=134 kHz	BW=200 kHz
$\delta f_{FSK}=30$ kHz	$\delta f_{FSK}=30$ kHz	$\delta f_{FSK}=30$ kHz	$\delta f_{FSK}=45$ kHz	$\delta f_{FSK}=45$ kHz	$\delta f_{FSK}=90$ kHz	$\delta f_{FSK}=90$ kHz	$\delta f_{FSK}=120$ kHz

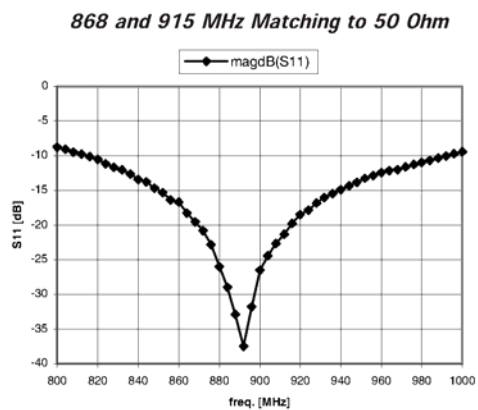
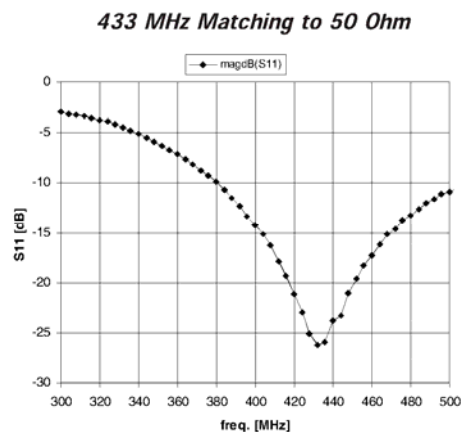
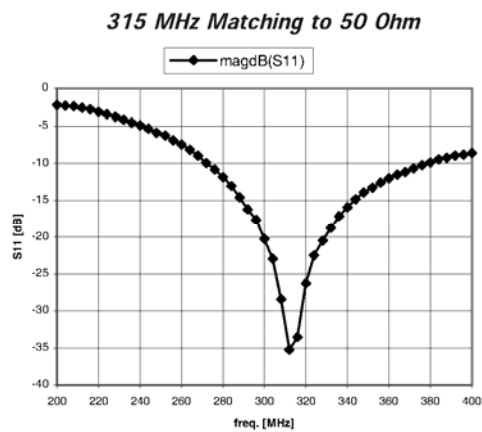
The table shows the optimal BW and δf_{FSK} selection for different data rates

Frequency Offset Effectuated Sensitivity Degradation



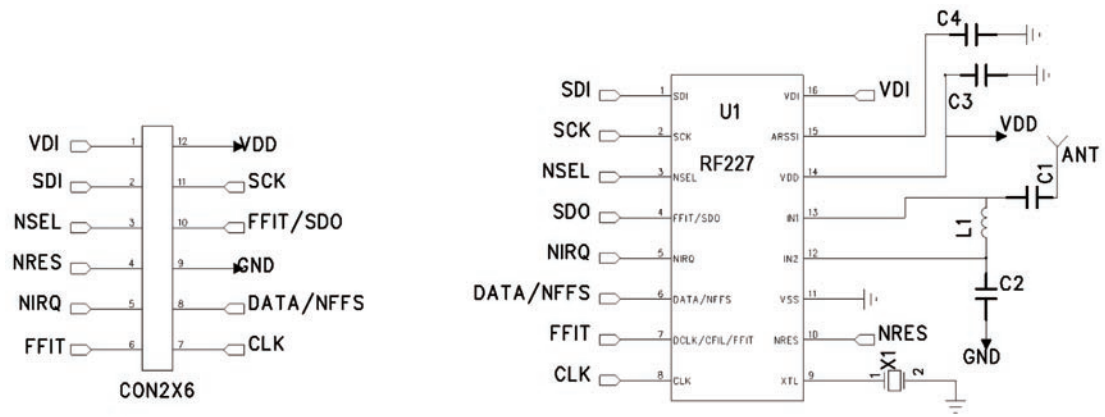
Input impedance

Measured input return loss on the demo boards with suggested matching circuit



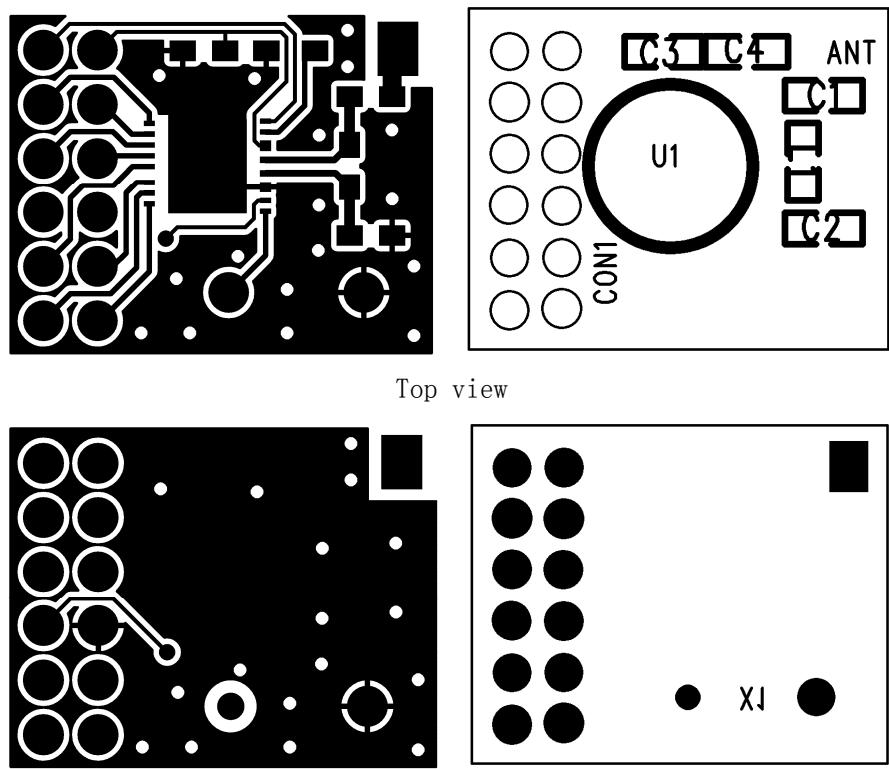
REFERENCE DESIGNS

Schematic



LOCATION BAND	C1	C2	L1	C3	C4
315	6PF	6PF	56nH	100nF	4.7nF
433	6PF	6PF	39nH	100nF	4.7nF
868	2.2PF	2.2PF	18nH	100nF	4.7nF
915	2.2PF	2.2PF	18nH	100nF	4.7nF

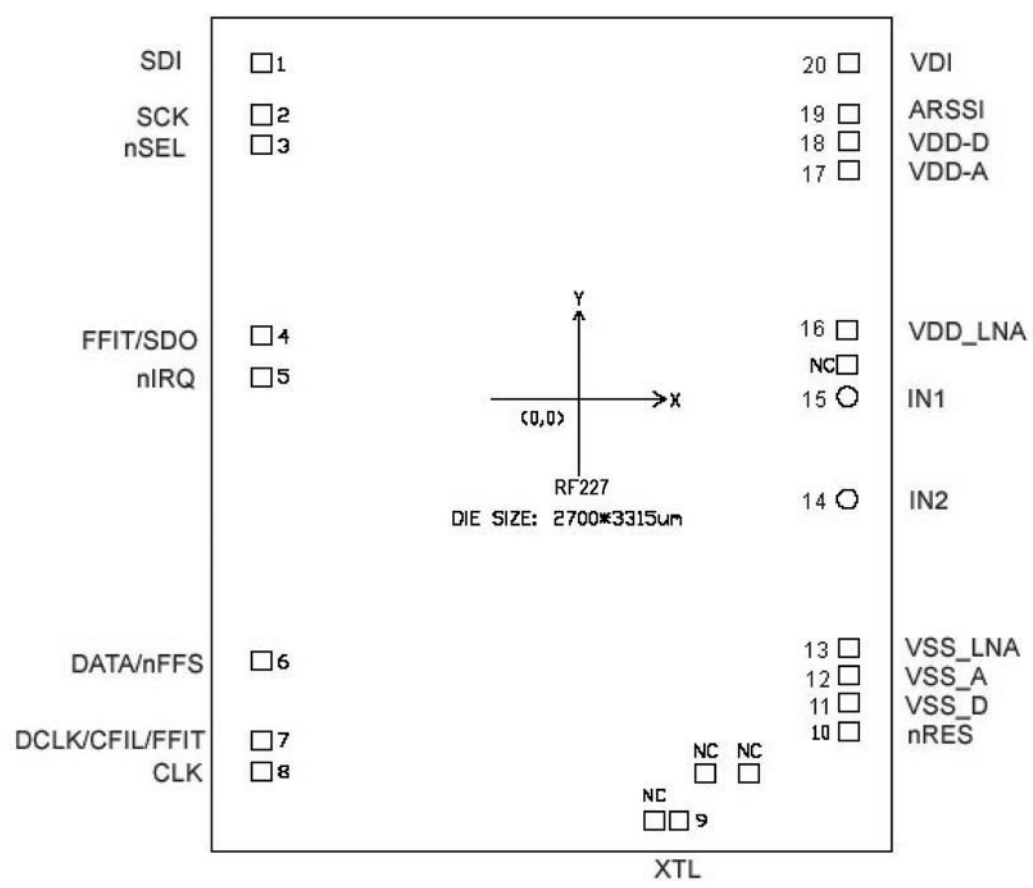
PCB layout



Top view

Bottom view

RF227 BONDING DIAGRAM



Pad Opening: 85 um square, except 76 um octagon pads (AN1, AN2)

Die Size: 2700 X 3315 um

