C-8201 -915MHz(FCC) TECHNICAL DESCRIPTION

A. CIRCIUT OPERATION

1. The equipment is 915MHz band FSK transmitter ,the first power up full display and the micro controller setting RF IC then read channel code and random code and temperature and humidity code then send to RF IC transmit. every 5 second or (model B 30 second) changed transmit frequency once .

(example 912MHz---→915MHz--→918MHz)

B. COMPONENT DESCRIPTION

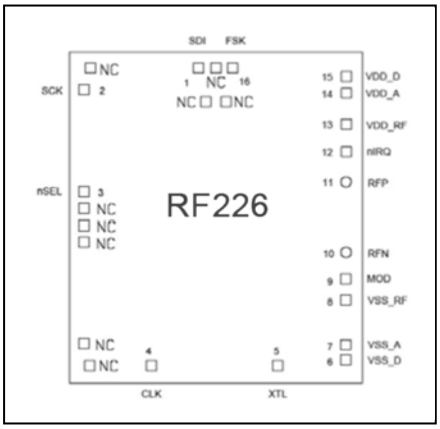
	COMPONENT	NAME	DESCRIPTION
	10MHz	Crystal	Stable RF transmitter Oscillator frequency and other.
	32.768kHz	crystal	Provide reference clock for MCU.
	C14,C15,C16,C17 and L1,L2,L3,L4		915MH Band-pass filter and antenna matching
	TM8726	Micro controller unit	The micro controller unit (MCU) are encoding and manipulating temperature data and controlled RF IC
	CL-HQM3R	Humidity sensor	Provide Humidity data for MCU
	RB103FS3435F01	Temperature sensor	Provide temperature data for MCU
	LL4148	Diode	Production test and humidity choice
	LED	LED	Every 30s transmit indicator
	RF IC (RF226)	RF IC	Convert MCU encoded data to RF FSK modulated signals. Frequency and low battery and FSK setting
	3 Channel switch		The three channel switch assign different channel code not changed frequency.

CHUNG'S ELECTRONIC CO.,LTD	
Name	TECHNICAL DESCRIPTION
Model	C8201(FCC)915
File No	TX8201(915)
Date	6/3/09
Name	Chan Kai Hung

RF226 Universal ISM Band FSK Transmitter

DESCRIPTION

RF226

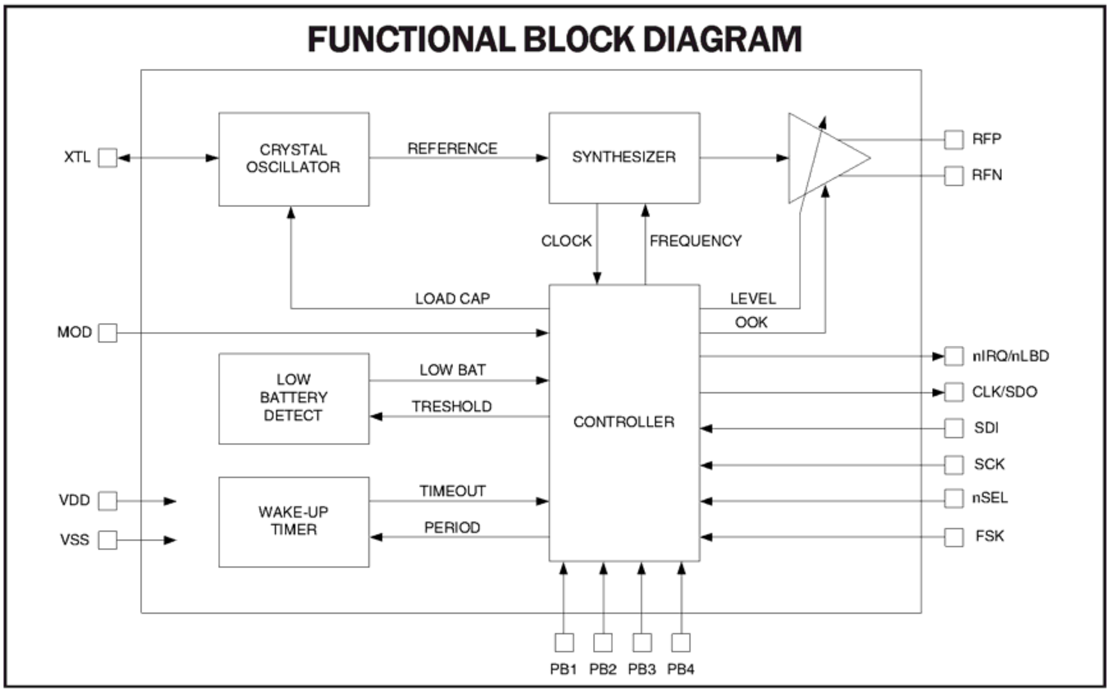


RF226 is a single chip, low power, multi-channel FSK transmitter designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with RF225, a FSK receiver, the RF226 transmitter produces a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation. The RF226 offering a higher output power and an improved phase noise characteristic.

The RF226 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading and interference to achieve robust wireless links. In addition, highly stable and accurate FSK modulation is accomplished by direct closed-loop modulation with bit rates up to 115.2 kbps. The PLL's high resolution allows the use of multiple channels in any of the bands.

The integrated power amplifier of the transmitter has an open-collector differential output that directly drive a loop antenna with programmable output level. No additional matching network is required. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and de-tuning due to the "hand effect".

For low-power applications, the device supports automatic activation from sleep mode. Active mode can be initiated by several wake-up events (on-chip timer timeout, low supply voltage detection).



FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- Stable and accurate FSK modulation with programmable deviation
- Programmable PLL loop bandwidth
- Direct loop antenna drive
- Automatic antenna tuning circuit
- Programmable output power level
- SPI bus for applications with microcontroller
- Clock output for microcontroller
- Integrated programmable crystal load capacitor
- Multiple event handling options for wake-up activation
- Wake-up timer
- Low battery detection
- 2.2V to 5.4V supply voltage
- Low power consumption
- Low standby current (0.3 μA)
- Transmit bit synchronization

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The RF226FSK transmitter is designed to cover the unlicensed frequency bands at 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands. The FSK deviation is selectable (from 30 to 210 kHz with 30 kHz increments) to accommodate various bandwidth, data rate and crystal tolerance requirements, and it is also highly accurate due to the direct closed-loop modulation of the PLL. The transmitted digital data can be sent asynchronously through the FSK pin or over the control interface using the appropriate command.

RF Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transmitters can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. When the chip receives a Sleep Command from the microcontroller and turns itself off, it provides several further clock pulses ("clock tail") for the microcontroller to be able to go to idle or sleep mode. The length of the clock tail is programmable.

Low Battery Voltage Detector

The low battery voltage detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 uA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then every 30 seconds. When the oscillator is switched off, the calibration circuit switches on the crystal oscillator only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the device supports sleep mode. Active mode can be initiated by several wake-up events: timeout of wake-up timer, detection of low supply voltage or through the serial interface.

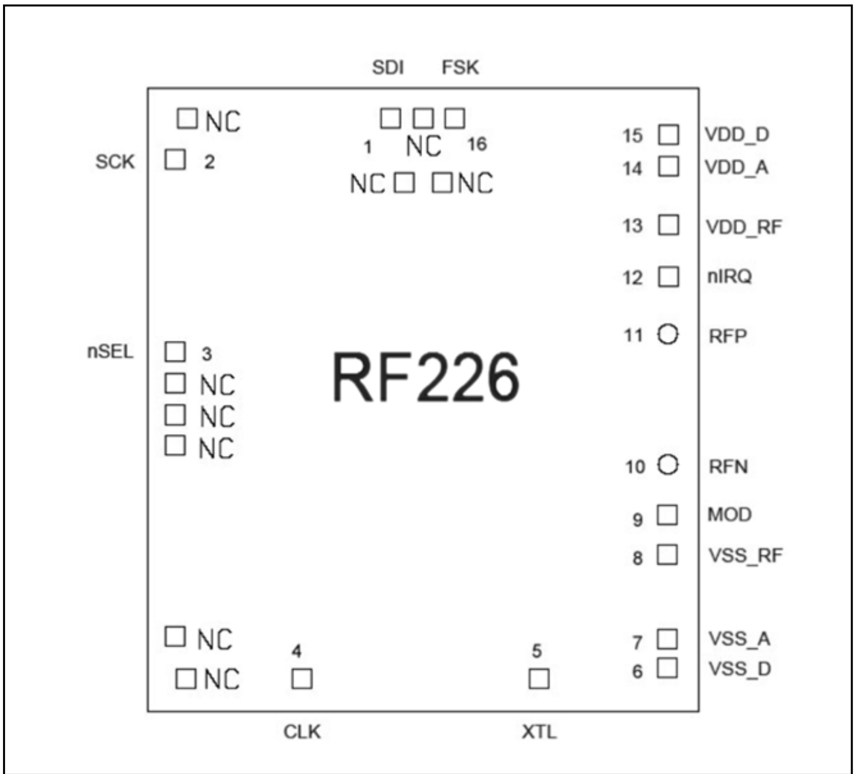
If any wake-up event occurs, the wake-up logic generates an interrupt, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the transmitters by the microcontroller through the nIRQ pin.

Interface

An SPI compatible serial interface lets the user select the operating frequency band and center frequency of the synthesizer, polarity and deviation of FSK modulation, and output power level. Division ratio for the microcontroller clock, wake-up timer period, and low battery detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode.

PACKAGE PIN DEFINITIONS

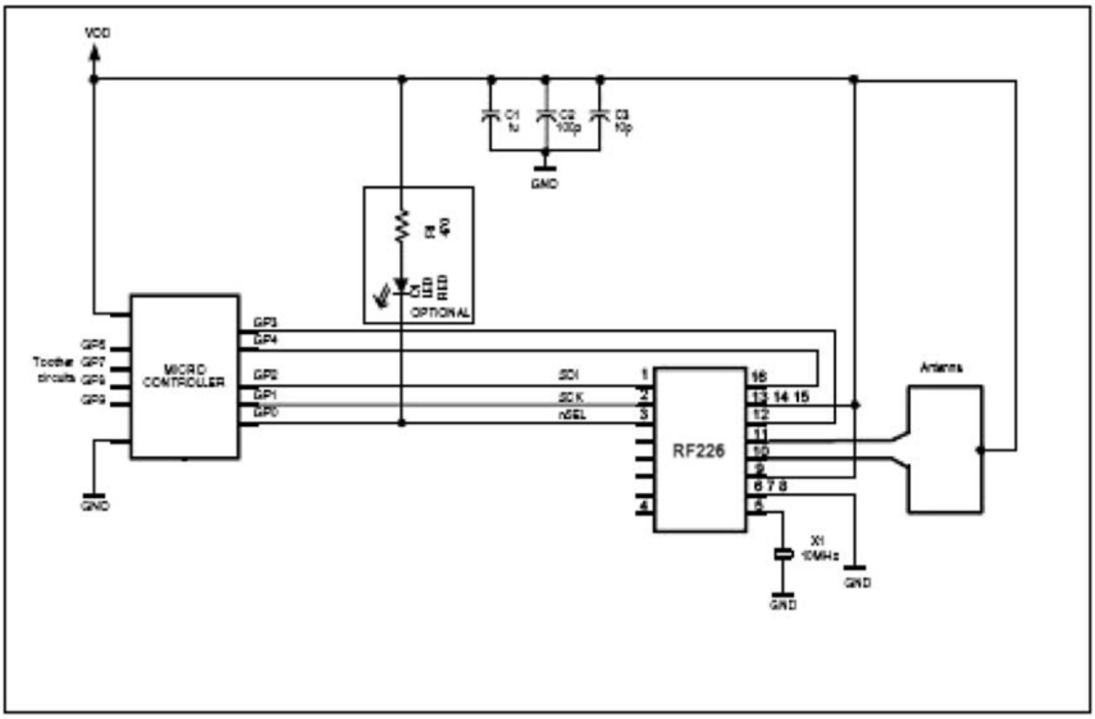
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



PinP	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of serial control interface (active low)
4	CLK	DO	Microcontroller clock (1 MHz-10 MHz)
5	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
6	VSS_D	S	Digital VSS(Connect to VSS)
7	VSS_A	S	Analog VSS(Connect to VSS)
8	VSS_RF	S	RF VSS(Connect to VSS)

9	MOD	DI	Connect to logic high
10	RFN	AO	Power amplifier output (open collector)
11	RFP	AO	Power amplifier output (open collector)
12	nIRQ	DO	Interrupt request output for microcontroller (active low) and status read output
13	VDD_RF	S	RF VDD(Connect to VDD)
14	VDD_A	S	Analog VDD(Connect to VDD)
15	VDD_D	S	Digital VDD(Connect to VDD)
16	FSK	DI	Serial data input for FSK modulation

Typical application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs	-0.5	6.0	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	℃

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
V_{oc}	Voltage on open collector outputs (Max 6.0 V)	V_{dd} - 1	V_{dd} + 1	V
T_{op}	Ambient operating temperature	-40	85	℃

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions:

T_{op} =27℃;V_{dd} =V_{oc}=2.7V)

DC Characteristics

Symbol	Parameter		Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, Pout =0dBm)	433 MHz band 868 MHz band 915 MHz band	Active state with 0dBm output power		12 14 15		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, Pout =P_{max})	433 MHz band 868 MHz band 915 MHz band	Active state with maximum output power		21 23 24		mA
I_{pd}	Standby current in sleep mode (Note 1)		All blocks disabled		0.3		μA
I_{wt}	Wake-up timer current consumption				1.5		μA
I_{lb}	Low battery detector current consumption				0.5		μA
I_x	Idle current		Only crystal oscillator is on		1.5		mA
V_{lba}	Low battery detection accuracy				75		mV

V_{lb}	Low battery detector threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{il}	Digital input low level				0.3*V_{dd}	V
V_{ih}	Digital input high level		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	μA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 5.4 V	-1		1	μA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristic

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	Crystal operation mode is parallel (Note 2)	9	10	11	MHz
f_o		433MHz band, 2.5kHz resolution 868MHz band, 5.0kHz resolution 915MHz band, 7.5kHz resolution	430.24 860.48 900.72		439.75 879.51 929.27	MHz
t_{lock}	PLL lock time	Frequency error < 10 kHz after 10 MHz step, POR default PLL setting(Note 7)		20		μs
t_{sp}	PLL startup time	After turning on from idle mode, with crystal oscillator already stable, POR default PLL setting (Note 7)			250	μs
I_{OUT}	Open collector output current (Note 3)	At all bands	0.5		6	mA
P_{maxL}	Available output power (433MHz band)	With opt. antenna impedance (Note 4)		8		dBm
P_{maxH}	Available output power (868 and 915 MHz band)	With opt. antenna impedance (Note 4)		6		dBm
P_{out}	Typical output power	Selectable in 3 dB steps (Note 3)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission	At max power with loop antenna (Note 5)			-50	dBc
C_o	Output capacitance (set by the automatic antenna tuning circuit)	At low bands At high bands	1.5 1.6	2.3 2.2	2.8 3.1	pF

Q_o	Quality factor of the output capacitance		16	18	22	pF
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier (Note 7)		-85 -105		dBc/Hz
BR_{FSK}	FSK bit rate	(Note 7)			115.2	kbps
df_{fsk}	FSK frequency deviation	Programmable in 30 kHz steps	30		210	kHz
C_{xl}	Crystal load capacitance See Crystal Selection Guidelines	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t_{POR}	Internal POR timeout (Note 6)	After V_{dd} has reached 90% of final value			50	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms		1.5	5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.95		1.05	ms
$t_{wake-up}$	Programmable wake-up time		1		$5 * 10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 1: Using a CR2032 battery (225 mAh capacity), the expected battery life is greater than 2 years using a 60-second wake-up period for sending 50 byte packets in length at 19.2 kbps with +6 dBm output power in the 915 MHz band.

Note 2: Using anything but a 10 MHz crystal is allowed but not recommended because all crystal-referred timing and frequency parameters will change accordingly.

Note 3: Adjustable in 8 steps.

Note 4: Optimal antenna admittance/impedance for the RF226:

	Yantenna [S]	Zantenna [Ohm]	Lantenna [nH]
434 MHz	1.3E-3 - j6.3E-3	31 + j152	58.00
868 MHz	1.35E-3 - j1.2E-2	9 + j82	15.20
915 MHz	1.45E-3 - j1.3E-2	8.7 + j77	13.60

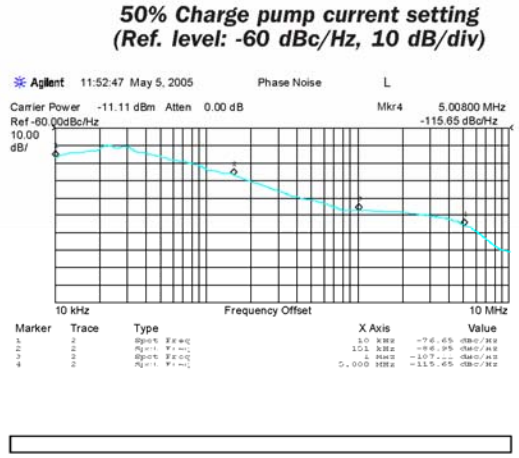
Note 5: With selective resonant antennas .

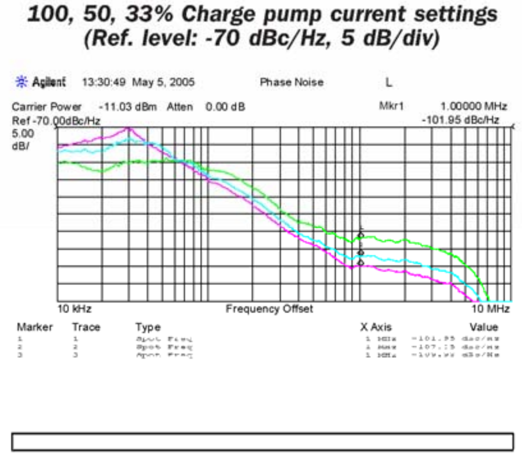
Note 6: During this period, no commands are accepted by the chip.

Note 7: The maximum FSK bitrate and the Output phase noise are dependent on the actual setting of the PLL Setting Command.

TYPICAL PERFORMANCE DATA (RF226)

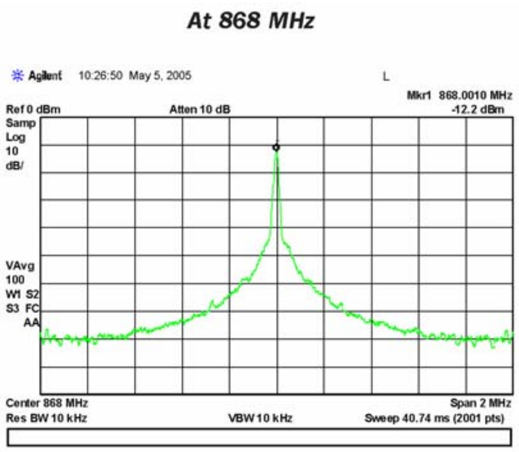
Phase noise measurements in the 868 MHz ISM band

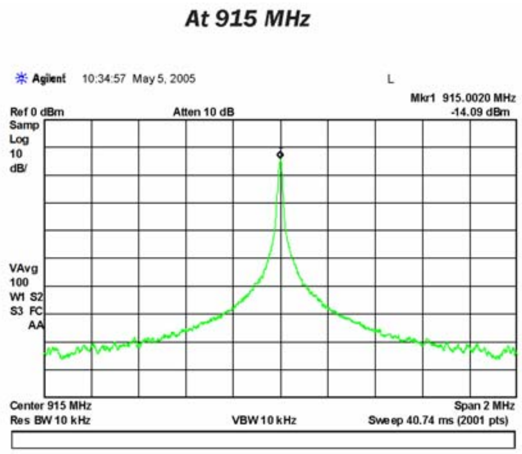




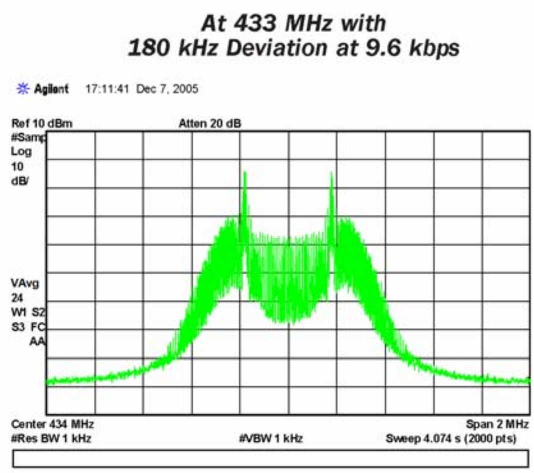
Unmodulated RF Spectrum

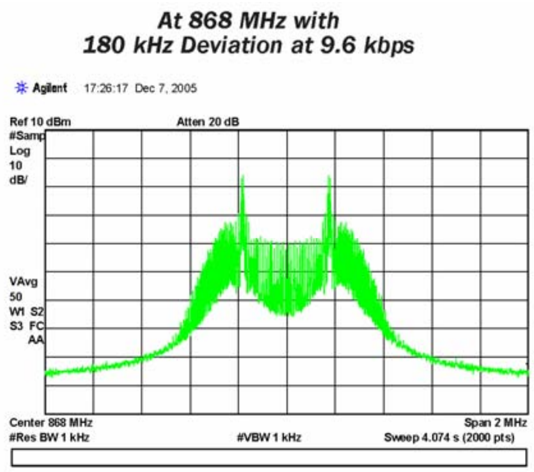
The output spectrum is measured at different frequencies. The output is loaded with 50 Ohms through a matching network.





Modulated RF Spectrum





RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RF226 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 100 ohms ESR (equivalent series loss resistance). However, lower C0 and ESR values guarantee faster oscillator startup. It is recommended to keep the PCB parasitic capacitances on the XTL pin as low as possible.

The crystal frequency is used as the reference of the PLL, which generates the RF carrier frequency (fc). Therefore fc is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable carrier frequency error.

The first 3 bytes compose a 24 bit length ‘01’ pattern to let enough time for the clock recovery of the receiver to lock. The next two bytes compose a 16 bit synchron pattern which is essential for the receiver’s FIFO to find the byte synchron in the received bit stream. The synchron patters is followed by the payload. The first byte transmitted after the synchron pattern (D0 in the picture above) will be the first received byte in the FIFO.

Important: The bytes of the data stream should follow each other continuously, otherwise the clock recovery circuit of the receiver side will be unable to track.

Further details of packet structures can be found in the RF ISM-UGSB1 software development kit manual