VADER

PROFESSIONAL SECURE RADIO

Federal Communications Commission Rules & Regulations

Part 2. 1033 (C) Application for Certification

Type of Radiation

16F3E

Range of Frequency

150 - 162 MHz (VADER Model Type: SR20A-01A)

160 - 172 MHz (VADER Model Type: SR20A-02A)

Rated RF Output Power

Hi 100 mW

Lo 10 mW

Method of Varying Radio-Frequency Power

As shown in the schematic diagrams of the VADER Radio MAIN circuit, at the Comparator (IC5), the direct current (DC) voltage which is proportional to the radio-frequency output power detected by D2 and D3 is compared with the reference voltage divided from stabilized 4.5 V at IC8. By controlling the Input Attenuator of the power amplification section that consists of a pin diode (D1) with the output from the Comparator, a desired output is produced.

Hi/Lo switching is done by changing the reference voltage at Q12.

D9, D12, D13, D14, and R14 (Thermistor) are elements for thermal compensation.

Collector Voltage and Current of Transistor of Final Power Amplifier

Collector Voltage (100 mW/10 mW) 9/9 V

Collector Current (100 mW/10 mW) 64/17 mA

Determination and Stabilization of Frequency

As shown in the schematic diagrams of the VADER Radio MAIN circuit, the frequency is stabilized within plus or minus 5 PPM at minus -30 to plus 60 degrees C by employing a PLL circuitry that uses TCXO as a reference oscillator. In the schematic diagrams, IC7 is PLL IC, TCX1 is TCXO, and an area encompassed by a dotted line is VCO.

IC7 is a PLL IC of Pulse Swallow type, and consists of Programmable Reference Divider, Pre-scaler, Swallow Counter, Programmable Counter, Phase Detector, Charge Pump, and Status Register.

The oscillation output from TCXO of 14.4 MHz is divided by 1152 into a reference frequency of 12.5 KHz by the Reference Divider.

The VCO oscillation frequency is scaled by the Pre-scaler, Swallow Counter, and Programmable Counter.

The phase difference between the divided frequency output and the reference frequency of 12.5 KHz is detected by the Phase Detector.

The detected phase difference is proportionally converted into the DC voltage by the Charge Pump and LPF. With this voltage, the VCO oscillation frequency is controlled and locked to the reference frequency.

The VCO for transmission oscillates on the transmission frequency, and VCO for reception oscillates on

the transmission frequency minus 21.7 MHz.
When PLL is locked, the oscillation frequency is formularized as follows:

fvco = [(P x N) + A] x 12.5 KHz

f vco: VCO oscillation frequency
P: division ratio for the Pre-scaler ("8" for this applied model)
N: setting value of the Programmable Counter (3 - 2047)
A: setting value of the Swallow Counter (0 - 127; A < N)

By selecting the values for N and A, any frequency can be obtained in multiples of 12.5 KHz. The CPU calculates necessary values for N and A based on specified frequency.

Suppression of Spurious Radiation

As shown in the schematic diagrams of the VADER Radio MAIN circuit, spurious radiation is suppressed below minus 60 dBC by the impedance matching circuit comprising VC1, VC2, C11, C12 and L14, and the 3-pole LPF comprising L1, L2, L3, C1, C2, C3, C4, C5, C6, and C7.

Limitation of Modulation

As shown in the schematic diagrams of the VADER Radio DSP circuit, the maximum deviation and adjacent-channel leakage power are controlled below their specified values by the ALC circuitry comprising Q1, Q2, D4 and C18, BPF and LPF (passband of 270 Hz - 3.2 KHz) that are built in IC2, IDC and the splatter filter built in IC1.

Operations of Transmitter

When the PTT button is pressed in the PTT mode, or when the PTT button is pressed or PTT is triggered by human voice in the VOX mode, the DSP (IC7 TMS320LC) sends a Start-of-Transmit signal "XF=H" to the CPU (IC2 μPD78054).

Upon receiving the "XF=H" signal, the CPU stops channel scanning. If it confirms no existence of any carrier wave with the RSSI signal, it sends out a "TX=H" signal to activate TX VCO oscillation. At the same time, it sends PLL data in the transmission frequency to the PLL IC (IC7 MB15F02).
When PLL is completely locked and a "LD=H" signal is sent back from the PLL IC (IC7 MB15F02), TX 4.5V is set to ON and carrier transmission is started.
After its harmonics component is reduced by the BPF comprising T1 and T2 of the MAIN PWB, the carrier wave passes through the RF ATT D1, is amplified by the Driver Amplifier IC4, and is additionally amplified up to the specified power (10 mW or 100 mW) by the Final Amplifier Q1. Then, it passes through the ANT SW IC1 and 3-pole LPF comprising L1, L2, and L3. By passing through those elements, the harmonics and spurious components in the carrier wave are fully reduced and it is supplied to the ANT.

By the APC circuitry comprising D1, D2, D3, and IC5, the output power is maintained constant with stability against varying temperature and power voltage.

The CPU receives the "LD=H" signal, and directs the Audio Processor (IC1 TC35491F) to turn off (mute) the MIC and transmit an ID signal.

At the same time, it sends out a Start-of-Transmit BEEP signal to the receiving AF line, and gives a "Pip!" sound via a speaker.

Once the ID transmission is completed, the MIC is turned on (de-muted) and voice transmission is started. The Audio Processor (IC1 TC35491F) performs scrambling transmission if it is programmed. Pre-emphasizing of voice signal is also done in this IC.

When the PTT is released, or if the VOX circuitry detects no voiced sound for 0.7 seconds, "XF=L" is processed. In response to this, the CPU turns off (mutes) the MIC, sends out an End-of-Transmit signal, and gives an ending BEEP ("Pip! Pip!") sound. It sets TX 4.5V to OFF for terminating carrier transmission and restarting channel scanning.

Operations of Receiver

Usually, the receiver scans a group of channels (10 ch + EM ch max.) which are selected by the Group Selector Switch at a speed of approximately 30 ch/sec.

As shown in the schematic diagrams of the VADER Radio MAIN circuit, the reception signal passes through the LPF comprising L1, L2, and L3, ANT SW (IC1 TC2206F), and 2-pole BPF comprising T3 and T4. The RF Amplifier Q2 amplifies it and its image signal is removed by the 3-pole BPF comprising T5, T6, and T7. Then, it is entered into the 1st Mixer Q3.

At the 1st Mixer Q3, the reception signal is mixed with the 1st Local Signal which is 21.7 MHz lower than the reception frequency produced by the CPU-controlled PLL circuit, and then converted into the 1st Intermediate Frequency (hereafter referred to as IF) of 21.7 MHz.

Since this signal contains many frequency components other than the 1st IF, the X'tal filters F1 and F2 remove unnecessary components and ensure the selectivity. The signal is amplified by the 1st IF Amplifiers Q4 and Q5, and then entered into the 2nd IF System IC (IC6 TA31137FN).

In the 2nd IF System IC (IC6 TA31137FN), this 1st IF signal is mixed with the 2nd Local Oscillator of 21.245 MHz by the 2nd Mixer, and converted into the 2nd IF of 455 KHz.

Since this signal contains many frequency components other than the 2nd IF, the ceramic filters F3 and F4 remove unnecessary components and ensure the sufficient selectivity. The signal is amplified by the 2nd IF Amplifier and the Limiter. It is then demodulated into an AF signal by the Discriminator, and entered into the Audio Processor (IC1 TC35491F).

If scrambling transmission is programmed in the Audio Processor (IC1 TC35491F), the De-scrambler is activated. The de-emphasizing of voice signal is also done in this IC. The AF signal is amplified by the AF Power Amplifier (IC3 NJM2113V), and the voice is output via a speaker.