LinkaNet Labs
FCC Part 15, Certification Application
FIRELINK 2000

June 22, 2000

MEASUREMENT/TECHNICAL REPORT

COMPANY NAME: **LinkaNet Labs**

MODEL: **FIRELINK 2000**

FCC ID: **OO8LNL001**

DATE: **June 22, 2000**

This report concerns (check one): Original grant_X_
Class II change_____

Equipment type: **__Direct Sequence Spread Spectrum Transmitter__**

Deferred grant requested per 47 CFR 0.457(d)(1)(ii)? yes_____ No_X_

If yes, defer until:_____
date

__N.A.__ agrees to notify the Commission by__N.A.____
date
of the intended date of announcement of the product so that the grant can be issued on that date.

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GENERAL INFORMATION

1.1 Product Description

The Equipment Under Test (EUT) is a LinkaNet Labs, Model FIRELINK 2000. The FIRELINK 2000 is a Direct Sequence Spread Spectrum radio designed for point to point microwave applications for voice and sub-rate data connectivity. The radio is capable of 64, 128, 256, 384, or 512 kbps data rates. The tables shown on the following pages give the typical transmitter frequencies associated with data rate. The EUT may be powered by 120 VAC, -48 VDC, or +24 VDC.

LO2

	Desired	Actual				LSB										SYNTHESIZER REGISTERS												MSB		LOAD Hexadecimal					
Fref (MHz)	0.5	0.5																												L1	L2	M1	M2	H1	H2
Fxtal (MHz)	13		IF		R_Format	C1	C2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20								
Flo2 (MHz)	560	560	280																																
R lo2	26				R lo2	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0			6	8	0	0	1	2
P lo2	16				N lo2	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1	0			0	1	8	C	1	0
B lo2	70				R lo1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0			6	A	0	0	1	2
A lo2	0				N_Format	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20								

Check R 26
Check B 70
Check A 0

Load PLL command:
testdrv bwfH1H2M1M2L1L2

LO1

Prescaler P lo1 64

								LSB										SYNTHESIZER N REGISTER														MSB		LOAD Hexadecimal					
CHANNEL	TX	LO1	TX	LO1	Ntotal	A	B	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20		L1	L2	M1	M2	H1	H2
fcc64_0	2403.5	2123.5	2403.5	2123.5	4247	23	66	1	1	1	1	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0		5	F	8	4	1	0
fcc64_1	2408.5	2128.5	2408.5	2128.5	4257	33	66	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0		8	7	8	4	1	0
fcc64_2	2413.5	2133.5	2413.5	2133.5	4267	43	66	1	1	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0		A	F	8	4	1	0
fcc64_3	2418.5	2138.5	2418.5	2138.5	4277	53	66	1	1	1	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0		D	7	8	4	1	0
fcc64_4	2423.5	2143.5	2423.5	2143.5	4287	63	66	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0		F	F	8	4	1	0
fcc64_5	2428.5	2148.5	2428.5	2148.5	4297	9	67	1	1	1	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0		2	7	8	6	1	0
fcc64_6	2433.5	2153.5	2433.5	2153.5	4307	19	67	1	1	1	1	0	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0		4	F	8	6	1	0
fcc64_7	2438.5	2158.5	2438.5	2158.5	4317	29	67	1	1	1	0	1	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0		7	7	8	6	1	0
fcc64_8	2443.5	2163.5	2443.5	2163.5	4327	39	67	1	1	1	1	1	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0		9	F	8	6	1	0
fcc64_9	2448.5	2168.5	2448.5	2168.5	4337	49	67	1	1	1	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0		C	7	8	6	1	0
fcc64_10	2453.5	2173.5	2453.5	2173.5	4347	59	67	1	1	1	1	0	1	1	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0		E	F	8	6	1	0
fcc64_11	2458.5	2178.5	2458.5	2178.5	4357	5	68	1	1	1	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0		1	7	8	8	1	0
fcc64_12	2463.5	2183.5	2463.5	2183.5	4367	15	68	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0		3	F	8	8	1	0
fcc64_13	2468.5	2188.5	2468.5	2188.5	4377	25	68	1	1	1	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0		5	7	8	8	1	0
fcc64_14	2473.5	2193.5	2473.5	2193.5	4387	35	68	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0		8	F	8	8	1	0
	Desired	Desired	Actual	Actual				CTRL					A									B							PROG							

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128k plan

LO2

	Desired	Actual				LSB												SYNTHESIZER REGISTERS										MSB		LOAD Hexadecimal					
Fref (MHz)	0.5	0.5																												L1	L2	M1	M2	H1	H2
Fxtal (MHz)	13		IF		R_Format	C1	C2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20								
Flo2 (MHz)	560	560	280																																
R lo2	26				R lo2	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0			6	8	0	0	1	2
P lo2	16				N lo2	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1	0			0	1	8	C	1	0
B lo2	70				R lo1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0			6	A	0	0	1	2
A lo2	0				N_Format	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20								

Check R 26
Check B 70
Check A 0

Load PLL command:
testdrv bwfH1H2M1M2L1L2

LO1

Prescaler P lo1 64

								LSB										SYNTHESIZER N REGISTER												MSB		LOAD Hexadecimal					
CHANNEL	TX	LO1	TX	LO1	Ntotal	A	B	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20		L1	L2	M1	M2	H1	H2
fcc128_1	2406	2126	2406	2126	4252	28	66	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0		7	3	8	4	1	0
fcc128_2	2416	2136	2416	2136	4272	48	66	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0		C	3	8	4	1	0
fcc128_3	2426	2146	2426	2146	4292	4	67	1	1	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0		1	3	8	6	1	0
fcc128_4	2436	2156	2436	2156	4312	24	67	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0		6	3	8	6	1	0
fcc128_5	2446	2166	2446	2166	4332	44	67	1	1	0	0	1	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0		B	3	8	6	1	0
fcc128_6	2456	2176	2456	2176	4352	0	68	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0		0	3	8	8	1	0
fcc128_7	2466	2186	2466	2186	4372	20	68	1	1	0	0	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0		5	3	8	8	1	0
fcc128_8	2474.5	2194.5	2474.5	2194.5	4389	37	68	1	1	1	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0		9	7	8	8	1	0
	Desired	Desired	Actual	Actual				CTRL					A								B								PROG						

256k plan

LO2

	Desired	Actual		
Fref (MHz)	0.5	0.5		
Fxtal (MHz)	13		IF	
Flo2 (MHz)	560	560	280	
R lo2	26			
P lo2	16			
B lo2	70			
A lo2	0			

Check R 26
Check B 70
Check A 0

	LSB																						MSB
R_Format	C1	C2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20	
R lo2	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	
N lo2	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1	0	
R lo1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	
N_Format	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20	

LOAD Hexadecimal					
L1	L2	M1	M2	H1	H2
6	8	0	0	1	2
0	1	8	C	1	0
6	A	0	0	1	2

Load PLL command:
testdrv bwfH1H2M1M2L1L2

LO1

Prescaler P lo1 64

CHANNEL	TX	LO1	TX	LO1	Ntotal	A	B
	Desired	Desired	Actual	Actual			
foc256_1	2411	2131	2411	2131	4262	38	66
foc256_2	2421	2141	2421	2141	4282	58	66
foc256_3	2431	2151	2431	2151	4302	14	67
foc256_4	2441	2161	2441	2161	4322	34	67
foc256_5	2451	2171	2451	2171	4342	54	67
foc256_6	2461	2181	2461	2181	4362	10	68
foc256_7	2468	2188	2468	2188	4376	24	68

	LSB																						MSB
	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20	
	1	1	0	1	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	
	1	1	0	1	0	1	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	
	1	1	0	1	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	
	1	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	
	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	
	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	
	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	
	CTRL		A									B											PROG

LOAD Hexadecimal					
L1	L2	M1	M2	H1	H2
9	B	8	4	1	0
E	B	8	4	1	0
3	B	8	6	1	0
8	B	8	6	1	0
D	B	8	6	1	0
2	B	8	8	1	0
6	3	8	8	1	0

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384k plan

LO2

	Desired	Actual				LSB		SYNTHESIZER REGISTERS																	MSB		LOAD Hexadecimal					
																											L1	L2	M1	M2	H1	H2
Fref (MHz)	0.5	0.5																													
Fxtal (MHz)	13		IF		R_Format	C1	C2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20						
Flo2 (MHz)	560	560	280																												
R lo2	26				R lo2	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0		6	8	0	0	1	2
P lo2	16				N lo2	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1	0		0	1	8	C	1	0
B lo2	70				R lo1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0		6	A	0	0	1	2
A lo2	0				N_Format	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20						

Check R 26
Check B 70
Check A 0

Load PLL command:
testdrv bwfH1H2M1M2L1L2

LO1

Prescaler P lo1 64

								LSB		SYNTHESIZER N REGISTER																MSB		LOAD Hexadecimal					
CHANNEL	TX	LO1	TX	LO1	Ntotal	A	B	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20	L1	L2	M1	M2	H1	H2
fcc384_1	2421	2141	2421	2141	4282	58	66	1	1	0	1	0	1	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	E	B	8	4	1	0
fcc384_2	2431	2151	2431	2151	4302	14	67	1	1	0	1	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	3	B	8	6	1	0
fcc384_3	2441	2161	2441	2161	4322	34	67	1	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	8	B	8	6	1	0
fcc384_4	2451	2171	2451	2171	4342	54	67	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	D	B	8	6	1	0
fcc384_5	2458	2178	2458	2178	4356	4	68	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	1	3	8	8	1	0
	Desired	Desired	Actual	Actual				CTRL				A										B						PROG						

512k plan

LO2

	Desired	Actual				LSB		SYNTHESIZER REGISTERS																		MSB		LOAD Hexadecimal					
Fref (MHz)	0.5	0.5																									L1	L2	M1	M2	H1	H2
Fxtal (MHz)	13		IF		R_Format	C1	C2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20						
Flo2 (MHz)	560	560	280																												
R lo2	26				R lo2	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0		6	8	0	0	1	2
P lo2	16				N lo2	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	0		0	1	8	C	1	0
B lo2	70				R lo1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0		6	A	0	0	1	2
A lo2	0				N_Format	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20						

Check R 26
Check B 70
Check A 0

Load PLL command:
testdrv bwfH1H2M1M2L1L2

LO1

Prescaler P lo1 64

								LSB										SYNTHESIZER N REGISTER										MSB		LOAD Hexadecimal					
CHANNEL	TX	LO1	TX	LO1	Ntotal	A	B	C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20	L1	L2	M1	M2	H1	H2
foc512_1	2421	2141	2421	2141	4282	58	66	1	1	0	1	0	1	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	E	B	8	4	1	0
foc512_2	2431	2151	2431	2151	4302	14	67	1	1	0	1	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	3	B	8	6	1	0
foc512_3	2441	2161	2441	2161	4322	34	67	1	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	8	B	8	6	1	0
foc512_4	2451	2171	2451	2171	4342	54	67	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	D	B	8	6	1	0
foc512_5	2458	2178	2458	2178	4356	4	68	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	1	3	8	8	1	0
	Desired	Desired	Actual	Actual				CTRL				A										B						PROG						

FCC ID: OO8LNL001

1.2 Related Submittal(s)/Grant(s)

The EUT will be used with part of a system to send/receive data. The transceiver presented in this report will be used with other like transceivers.

The EUT is subject to the following authorizations:

a) Certification as a transmitter
b) Verification as a digital device

The information contained in this report is presented for the certification & verification authorization(s) for the EUT.