5.Description of circuitry

5.1. Modem MOD 915M is intended for reception/ transmission of signals in the frequency band of 902 – 928 MHz for frequency hopping (FH) operational mode or direct spread spectrum (DSS) operational mode.

Modem can be operated only along with a navigation receiver REC GPS. Information signals on reception / transmission are generated and processed by hardware and software of the REC GPS. The same signals get MOD 915M under control. Supply voltage of the modem is generated by the REC GPS board.

The following operational modes are available:

-Reciever / transmitter (rover / base);

-FH / DSS;

-antenna int / ext;

-output power 10/50 mW.

Keyboard input of control commands is implemented by PC connected with any connector SERIAL A … D of the REC GPS. Established modes are maintained in the Battery Backed-Up RAM of the REC GPS.

5.2. MOD 915M comprises the following modules:

-RF RECEIVER;

- RF AMPL;

-UP & DOWN CONVERTER with LO _RF;

-BPF FH and BPF DSS;

-receiving FH_IF part;

-receiving DSS_IF part;

-LO_IF;

-MODULATOR;

-CONTROL UNIT;

-LOCAL LINEAR REGULATORS.

5.3. Receiver

5.3.1. The received signal through the connector ANT_INT (ANT_EXT) and the commutator SW1 based on pin diodes is filtered by the BPF011 and is amplified by the LNA. The limiter of the diodes D011, D012 and AGC- circuit increase the dynamic band of the receiving system and eliminate signal restriction in the LNA and RF_MIX under occurring interference level much greater than the level of the received signal. Through SW2, switching operational modes TRANSMIT / RECEIVE of the modem, the signal is applied to the DOWN CONVERTER where it is additionally filtered by the BPF031 and converted into the first IF equal either to 280 MHz for DSS mode or to 270 MHz for FH mode. The signal from LO _RF is applied to the heterodyne input of the diode mixer RF_MIX . For DSS mode LO _RF generates the signal of constant frequency of 1195 MHz, for FH mode heterodyne frequency follows the pseudorandom law in the band of 1172.2 – 1197.8 MHz across a 200 KHz band.

The IF signal is amplified by a bi-directional amplifier and through the switch SW3 is delivered to the paths of signal filtration for both FH and DSS modes (BPF FH and BPF DSS correspondingly). The parameters of these filters will be given below. The switch SW5 (SW6) commutes the signal to the receiving part FH_IF (DSS_IF).

5.3.2. The receiving part FH_IF consists of AGC amplifier U054 and monolithic FM IF system U053 (SA626) incorporating a mixer, two intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio op amp. Besides, this part comprises two narrow band – pass filters BPF051 and BPF052 for frequency band of 10.7 MHz , frequency discriminator X001, op amps (U052), and two comparators (U051).

The signal with frequency of 270 MHz is amplified and converted in the mixer into the second intermediate frequency IF2 equal to 10.7 MHz, the signal LO_IF with frequency of 280.7 MHz being applied to the heterodyne input of the diode mixer. The main signal amplification is implemented by amplifiers in U053 (about 92 dB) while channel filtration is carried out by the filters BPF051 and BPF052. The signal from the second limiting amplifier

goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF2. The other output of the IF2 is AC-coupled to a tuned quadrature network X001. This signal, which now has a 90^0 phase relationship to the internal signal, drives the other port of the multiplier cell.

The information signal assigned by the frequency discriminator is amplified and converted by a comparator U051 into the CMOS compatible signal. This signal by RX_FH_DATA circuit is applied to ASIC JPS on the REC GPS board. In ASIC there exists clock rate separation , signal restoration, Cyclic Redundancy Checsum, and extraction of information from each correctly received packet.

5.3.3. The receiving DSS_IF part consists of AGC amplifier U063 and monolithic IF subsystem U062 (AD607) incorporating a mixer, linear four-stage IF strip, logarithmic received signal strength detector, and the temperature stable gain control system which provides an accurate RSSI capability. Moreover, this part comprises two similar low-pass frequency filters LPF1 and LPF2 based on discrete components with the 1dB bandwidth about 17 MHz, and two transistor-based buffer amplifier.

The signal with the frequency of 280 MHz is amplified and converted in the mixer into the second intermediate frequency IF2 equal to 9.9 MHz, the signal LO_IF with the frequency of 289.9 MHz coming at the heterodyne input of the mixer. The main signal amplification is implemented by the mixer and amplifiers in U062 (about 90 dB), the filters LPF1 and LPF2 restricting the bandwidth by the intermediate frequency. The received signal with IF2 equal to 9.9 MHz comes to the REC GPS board through the circuit RX_DSS_SIGN_ADC. At this board the signal goes to the binary qiantizier of the comparator and further to ASIC.

In ASIC the digital coherent processing of the received signal is carried out. This processing is based on generating reference oscillations whose phases coincide with phases of carrier and modulating oscillations (within the accuracy of small tracking errors). That coherent processing is implemented with the help of phase-lock-loop (PLL) and delay-lock –loop (DLL). Signals from the correlators are stored over the PRN period and go to the processor (uC). ASIC contains a set of correlators, reference frequency and PRN-code syntezators, and reset adders. The signals of PLL and DLL discriminators for adjusting reference syntezators are computed in the processor. The processor separates the received information signal.

5.4. Transmitter

5.4.1. The transmitting path of the modem comprises the following modules:

- modulator MOD;
- BPF FH and BPF DSS;
- UP CONVERTER;
- RF AMPL.

5.4.2. Under FH mode operation MSK signal modulation can be used as follows: the transmitted information signal having clock rate of 64 kHz and CMOS levels comes from ASIC JPS through TX_FH_DATA to the input FSEL of DIRECT DIGITAL SYNTEZATOR (DDS) U108 which generates MSK signal with peak frequency deviation of 16 kHz on the intermediate frequency of 10.7 MHz. This signal is filtered by narrow-band filter BPF061, then is amplified and through open SW7 goes to the mixer U072 (HPMX-2007) which implements spectrum transformation into IF equal to 270 MHz.

The signal LO_IF with the frequency of 280.7 MHz comes at the heterodyne input LOMOD U072. The output signal is amplified and filtered by BPF FH and through open SW3 goes to the bi-directional amplifier and further to the RF_MIX IF input.

The signal with parameters similar to p.5.3.1 from LO_RF comes at the mixer input LO. The filter BPF031 separates the signal in the operational frequency bandwidth of 902 – 928 MHz and suppresses both the signal LO and unwanted sideband. From the filter output through SW2 the signal comes at RF AMPL.

5.4.3. RF AMPL comprises variable gain amplifier U021, matching attenuators ATT1 and ATT2, filter BPF021, and transistor-based final amplifier.

Stabilizing the power mean value of modem output signal is implemented by the AGC circuit, which includes level detector based on diodes D021, D022, op ampl U022, and variable gain amplifier U021. The voltage from the detector output through MODEM_ADC is applied to

the REC GPS board, is then processed by uC, which computes control voltage TX_AGC, and through DAC U105 applies the voltage further to the amplifier U021.

The final power amplifier can provide power outputs at the connectors J001 or J002 equal to either 10 or 50 mW depending on the established mode.

The filters BPF001, BPF002 provide extra filtering harmonic components of transmitter's signal.

5.4.4. Under DSS mode operation BPSK modulation of the signal can be used. The transmitted information signal having clock rate of 7.0MHz and CMOS levels comes from ASIC JPS through TX_DSS_DATA at the signal input of the modulator U072 while the signal LO_IF with the frequency of 280MHz goes to the heterodyne input LOMOD. The modulator generates BPSK signal on the intermediate frequency of 280 MHz. This signal is amplified and flittered by BPF DSS, then through open SW3 comes at the bi-directional amplifier, and further at the RF_MIX IF input.

The signal LO_RF with the frequency of 1195 MHz comes at the mixer LO input. Subsequent filtration and signal amplification are carried out like FH mode.

5.5. The filtering module BPF FH (BPF DSS) comprises SAW filter with the frequency of 270(280)MHz and the 1dB bandwidth equal to 330(17000)kHz, match circuit of the filter, and switch SW5(SW6) connecting output MOD or input FH_IF(DSS_IF) with the filter BPF042 (BPF041). SW4 in BPF DSS provides extra attenuation of LO signals and unwanted sideband , which can pass through wide-band filter BPF041under transmit- FH-mode operation.

5.6. LO_RF generates a signal with the following parameters:

- Frequency band from 1172 to 1198 MHz across a 0.2 MHz band;
- Output at 50 Î ì is minus 10 dBm;
- Level of harmonic components is not greater than minus 30 dBm.

5.7. LO_IF generates a signal as follows:

- Frequency band from 280 to 290 MHz across a 0.1 MHz band;
- Output at 50 Î ì is minus 2.5 dBm;
- Level of harmonic components:the 2^{nd} harmonic is not greater than minus 13 dBm, 3^{rd} is not greater than minus 27 dBm, 4-th is not greater than minus 60 dBm.

5.8.Modules comprising CONTROL UNIT provide interface between REC GPS and internal circuits of the MOD 915M.

5.9. MOD 915M uses power supply of 3.3V from the REC GPS board. This voltage applies to commutable linear regulators having output voltage of 3.0V. These regulators power separate modules of the modem and operate if necessary.