1. Processing Gain.

THE TEST SETUPS:

This section provides measurement guidelines for the Direct Sequence Spread Spectrum Systems. The tests below are run with the DCT transmitter set at high power in TDD mode. A serial port from a computer to the DCT UUT is needed to force selection of output power level and channel.

Section 15.247(e) : Processing Gain.

The processing gain may be measured using the CW jamming margin method. Figure 1 shows the test configuration. The test consists of stepping a signal generator in 50 KHz increments across the passband of the system (up to 960 KHz away in RI's DCT). At each point, the generator level required to produce the recommended Bit Error Rate (BER) (Set at BER=10^{-3}) is recorded. This level is the jamming level. The output power of the transmitting unit is measured at the same point. The jammer to Signal (J/S) ratio is then calculated. Discard the worst 20% of the J/S data point. The lowest remaining J/S ratio is used to calculate the processing gain. The maximum implementation loss a system can claim in calculating processing gain is 2 dB. The equation to calculate the processing gain (Gp) is the following.

$$Gp = (S/N)o + Mj + Lsys$$

Where Lsys=system implementation loss= 2dB.

Mj=jamming margin (J/S) in dB.

(S/N)o=signal to noise ratio required for a DBPSK system with BER of 10^{-3}=8.0dB

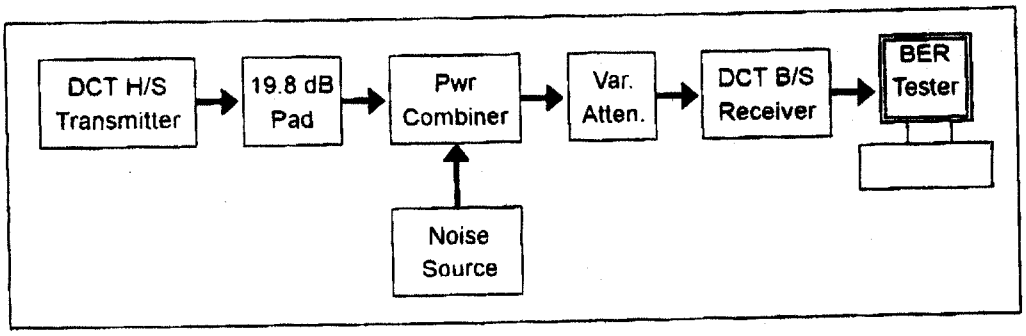

Figure 1 : Jamming Test Setup

S = Signal Power – Attn – Comb loss – cable Loss

= 4.0 – 109.8 – 3.6 – 0.5

= -27.9 dB

J = Sig Gen O/PivI(N) – cal factor – Comb Loss

= N – 0.3 – 3.6 dB

Jammer Freq.(MHz)	Signal Lv DB	CW Noise N dB	Mj J/S dB	Proc.Gain dB
915.6	-27.9	-15.1	8.8	19
915.65	-27.9	-15	8.9	19.1
915.7	-27.9	-22.9	1	11.2
915.75	-27.9	-19.9	4	14.2
915.8	-27.9	-19.6	4.3	14.5
915.85	-27.9	-20.3	3.6	13.8
915.9	-27.9	-21.3	2.6	12.8
915.95	-27.9	-19.3	4.6	14.8
916	-27.9	-21	2.9	13.1
916.05	-27.9	-11.8	12.1	22.3
916.1	-27.9	-19.5	4.4	14.6
916.15	-27.9	-11.8	12.1	22.3
916.2	-27.9	-17	6.9	17.1
916.25	-27.9	-14.2	9.7	19.9
916.3	-27.9	-12.5	11.4	21.6
916.35	-27.9	-10	13.9	24.1
916.4	-27.9	-6	17.9	28.1
916.45	-27.9	-4	19.9	30.1
916.5	-27.9	-1.2	22.7	32.9
916.55	-27.9	-1.8	22.1	32.3

2. Data Rate

80 Kb/s Time Division Duplex(TDD)

32K Transmit + 32K Receive + Overhead

3. Chip Rate

960 Kchips/s (12 chips per bit) DSSS

4. Sampling Rate

1.92 Msamples/s (2 samples/chip)