4.0 VTU Circuit Description

4.1 Introduction

The main subsystems of the VTU are OEM Data Transceiver, OEM GPS Receiver, and Digital Baseband Board. A block diagram of critical RF circuitry are depicted in Section 4.

4.2 Digital Baseband Board

The Digital Baseband Board handles all I/0 external to the VTU and all I/O functions to and from the OEM GPS Receiver and OEM Data Transceiver.

4.2.1 Microprocessor (U1), RAM/ROM (U3,U2,U9)

The Microprocessor in conjunction with the RAM/ROM memory executes programming to control all I/O functions, process receive and transmit data, control all functioning on the Digital Baseband Board and with the Data Transceiver and GPS Receiver. A 8 MHz clock generates pulses used by the microprocessor to execute programming, clock I/O and program the synthesizer. Programming information is fed out on enable, data, and clock lines and is distributed by buffers to other digital components.

The microprocessor provides receiver and transmitter control information including Synchronization Enable (PA5/JP1, pin 8), Synchronization Data (PD3/JP1, pin 9), Synchronization Clocking (PD4/JP1, pin 10) through digital buffers (U13) to the Data Transceiver. The Data Transceiver is mated to the Digital Baseband Board via the 14 pin JP1 connector. The microprocessor receives a Synchronization Lock indication (JP1, pin 7) directly from the Data Transceiver. The microprocessor receives a Carrier Detection (PA7) indication from the Carrier Detection logic on the Digital Baseband Board. The same Carrier Detection indication is provided directly to the Data Transceiver (JP1, Pin 11).

The microprocessor also provides transmit data (Txdata) and accepts received data (Rxdata) from the MX909 Modem (U12) via data lines D0 through D7. Data and control information exchanged between the OEM GPS Receiver and external to the VTU occurs through the RS232 interface controlled by U23 and U24.

4.2.2 Splatter Filter and Bias Control

The modulated transmit signal is coupled to and shaped by a two stage splatter filter (U15, U28). The splatter filter is a low pass filter that attenuates frequencies above defined value related to the modulation rate. The purpose of the splatter filter is to prevent over modulation of the transmited audio signal before it is presented to the Data Transceiver. Over modulation could cause adjacent channel interference.

The output from the splatter filter is fed to a gating circuit (U29) that imposes a +2.5V DC, ±.1V bias on the audio signal. This bias level is adjusted via VR1 based on factory alignment procedures. Bias control of the modulated audio signal is required to maintain accurate receive and transmit frequencies with the Data Transceiver. The output of the gate circuit is presented to the Data Transceiver on JP1, pin 6.

4.2.3 Rxout Amplifier and DC Bias Control

Received audio signals from the Data Transceiver (JP1, pin 13) are buffered, amplified and bias controlled before transfer to the MX909 Modem chip (U12). Audio signals are first buffered by U10(pins 12,13,14) and then amplified by U10(pins 8, 9, 10) with an above unity gain. R36 is adjusted to yield a +2.7V DC, ±.1V signal bias using factory alignment procedures. DC bias control is needed to minimize BER on receive data derived from the MX909 modulation process.

4.2.4 Carrier Detection

RSSI signals presented by the Data Transceiver (JP1, pin 12) are used to declare carrier detection. The RSSI signal has a voltage level that increases in proportion to increases in the received signal strength at the Data Transceiver IF frequency.

The RSSI signal is first buffered by U10(pins 2,3,4) and then applied to amplifier/comparator U10(pins 5,6,7). When the RSSI signal reaches the reference voltage the output goes low. Low output indicates a carrier of significant strength (greater than 110 dBm) and a high output indicates no carrier present condition. Potentiometer R47 allows the setting of the reference voltage level providing hysterisis for weak and fading signals.

4.2.5 Receiver/Transmit Switching Control

Circuits on the Digital Baseband Board under the control of the microprocessor (U1) provide switched voltages to the Data Transceiver to control receive and transmit functions. Switched +8V DC is presented at JP1, pin 3 for control of transmit functions and +5V DC is presented at JP1, pin 4 for control of receive functions. Additionally non switched +8V DC and +5V DC are presented at JP1, pins2, 3 and 14.

4.2.6 RS-232 Modem

The RS232 modem (U23, U24) support a data interface between 1) the Digital Baseband Board microprocessor and the GPS Receiver card and 2) the Digital Baseband Board microprocessor and external devices to the VTU. External devices interfacing via the RS232 typically consist of data digital display device.

The RS232 port is operated at a 9600 Baud rate and is designed to be compatible with the RS232 standard of the Electronic Industries Association (EIA). This standard specifies pin assignments and voltage levels associated with the interface between data terminals

and data communications equipment. Equipment connected to this modem should be compatible with this standard.

4.2.7 Modem Data Pump

The Modem Data Pump (U12/MX909A) is microprocessor device that contains all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for GMSK Wireless operation.

In the transmit mode, the modem assembles application data received from the data microprocessor (U1), adds forward error correction (FEC) and error detection codes, time spreads this data by interleaving and scrambles the bit pattern. After adding the bit and frame sync code words, the data packets are converted into GMSK signals for modulating the Data Transceiver transmitter. Before the Data Transceiver receives the modulated audio it is passed through the splatter filter (U15,U28) and adjusted for DC signal bias.

In the receive mode, the modem performs the reverse functions as is performed in the transmit mode after demodulating the receiver signal. The demodulated signal information is unscrambled, de-interleaved, error corrected and packet overhead data is removed. Final recovered application data is provided to the data microprocessor. CRC detected residual uncorrected data errors are flagged and SNR of received packets are also provided.

The modem is driven by a 4.9152 MHz oscillator used as a source generating the composite sine waves making up the GMSK modulation waveform.

4.2.8 Data Transceiver

The Data Transceiver is a E.F. Johnson DM-3474 model (High Specification Data Transceiver Part Number 242-3474-xxx) synthesized UHF receiver/transmitter operating in the 450 through 512 MHz frequency range utilizing either 25kHz or 12.5 kHz channels. Frequencies and channel widths are characteristics of the particular version of the baseline DM-3474 model selected. Transmitted power output is 2 watts nominal and operation is simplex. The Data Transceiver interfaces with the Digital Baseband Board via connector JP1 and is internal to the VTU.

Descriptions of circuit operation for the Data Transceiver is provided in Section 4.5 and is excerpted from the High Specification Data Transceiver Part No. 242-3474-xx0 Service Manual.

4.2.9 GPS Receiver

The Oncore GPS Receiver has 12 independent receiver channels that track GPS satellite signals in both code and carrier phase. Time recovery and utilization of differential GPS corrections are integrated features. On achieving a full solution, the GPS receiver presents position, velocity, heading, time as 1PPS and status representing the GPS

receive antenna. The GPS Receiver generates no intentional transmissions to perform its functions.

The GPS Receiver interfaces with the Digital Baseband Board via an RS232 port across connector JP2. The 12 independent receivers track the L1 GPS signal (1575.42Mhz) and operates off the clear /acquisition (C/A) carrier tracking. RF signals from the antenna port are down converted to IF frequency and then passed to Channel code and carrier digital correlators where a single high speed analog-to-digital converts IF to a digital sequence. Further digital processing performs code correlation, filtering, tracking and signal detection.

Full GPS solutions are transferred via the RS232 port to the Digital Baseband Board microprocessor.

4.3 Transmit Data Processing

After transmit messages are formatted and assembled with required control information with the data microprocessor (U1) the data is transferred through a serial port to the MX909A modem (U12) where the information is temporarily buffered. The modem scrambles and modulates the data to create an audio signal in real-time to forward to the Data Transceiver. Before the Data Transceiver receives the modulated audio signal it is filtered and biased.

4.4 Receive Data Processing

Received signals are down converted to audio signals by the Data Transceiver and based to the Digital Baseband Board as Rxout and overall signal level indication RSSI. The RSSI is processed by a comparator generating a Carrier Detect indication used by both the data microprocessor (U1) and the Data Transceiver. Rxout is amplifier and biased before transfer to the modem microprocessor (U12) for demodulation and data extraction. Extracted data is transferred from the modem microprocessor to the application microprocessor for final data extraction, data processing and presentation to I/O.

4.5 Data Transceiver Circuit Description

SECTION 4

CIRCUIT DESCRIPTION

4.1 GENERAL

4.1.1 INTRODUCTION

The main subassemblies of this transceiver are the RF board, VCO board, and TCXO. A block diagram of the transceiver is located in Figure 4-1.

The VCO board is enclosed by a metal shield and soldered directly to the RF board. The VCO is not serviceable.

The 3474 is available with a reference oscillator stability of ±1.5 PPM. The TCXO (Temperature Compensated Crystal Oscillator) is soldered directly to the RF board.

4.1.2 SYNTHESIZER

The VCO (voltage-controlled oscillator) output signal is the receiver first injection frequency in the Receive mode and the transmit frequency in the Transmit mode. The first injection frequency is 52.95 MHz above the receive frequency. The frequency of this oscillator is controlled by a DC voltage produced by the phase detector in synthesizer chip U801.

Channels are selected by programming counters in U801 to divide by a certain number. This programming is performed over a serial bus formed by the Synth Clock, Synth Enable, and Synth Data pins of J201. This programming is performed by user supplied hardware and software (see Section).

The frequency stability of the synthesizer in both the receive and transmit modes is established by the stability of the reference oscillator described in the preceding section. These oscillators are stable over a temperature range of -30° to +60° C (-22° to +140° F).

4.1.3 RECEIVER

The receiver is a double-conversion type with intermediate frequencies of 52.95 MHz / 450 kHz. Two helical bandpass filters reject the image, half IF, injection, and other unwanted frequencies. A four-pole crystal filter enhances receiver selectivity

CIRCUIT DESCRIPTION

4.1.4 TRANSMITTER

The transmitter produces a nominal RF power output of 2W adjustable to 500 mW (-XX0). Frequency modulation of the transmit signal occurs in the synthesizer. Transmit audio processing circuitry is contained in the customer-supplied equipment.

4.2 SYNTHESIZER

4.2.1 INTRODUCTION

A block diagram of the synthesizer is shown in Figure 4-1 and a block diagram of Synthesizer IC U801 is shown in Figure 4-2. As stated previously, the synthesizer output signal is produced by a VCO (voltage controlled oscillator). The VCO frequency is controlled by a DC voltage produced by the phase detector in U801. The phase detector senses the phase and frequency of the two input signals and causes the VCO control voltage to increase or decrease if they are not the same. The VCO is then “locked” on frequency.

Programming of the synthesizer provides the data necessary for the internal prescaler and counters. One input signal is the reference frequency. This frequency is produced by the 17.5 MHz reference oscillator (TCXO). The other input signal is the VCO frequency.

CIRCUIT DESCRIPTION

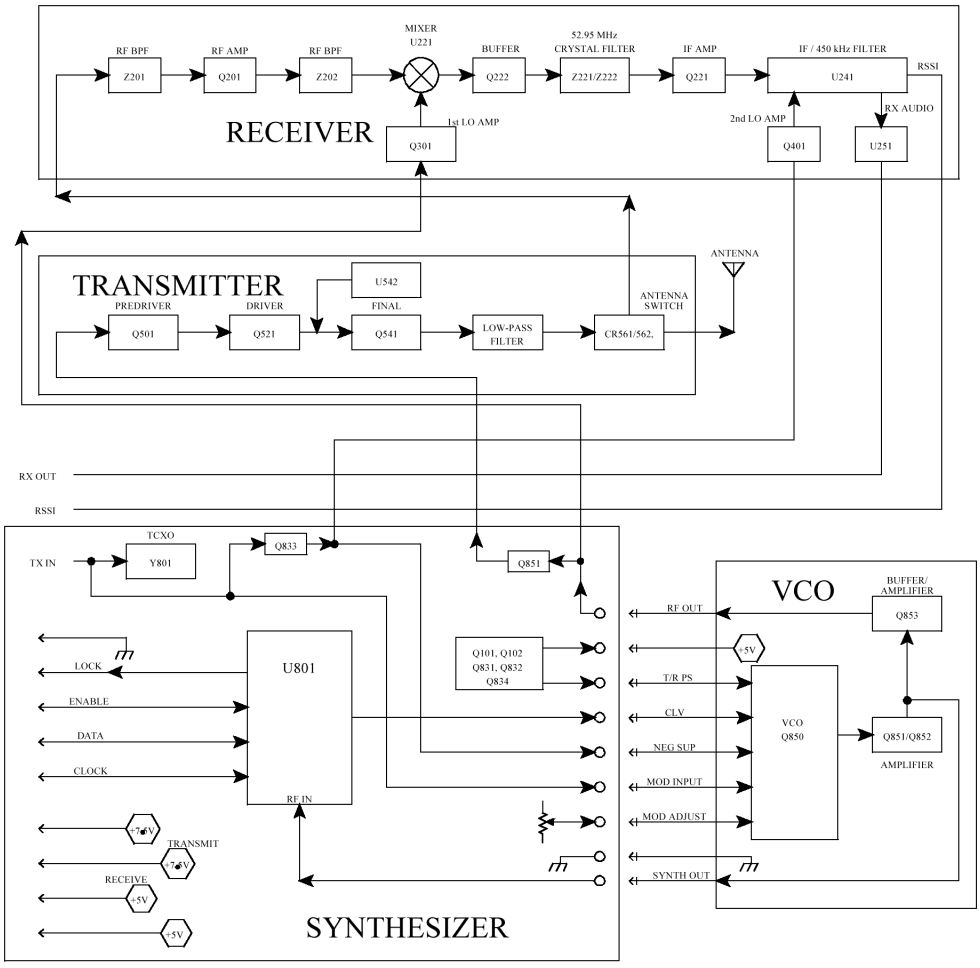

Figure 4-1 DATA TRANSCEIVER BLOCK DIAGRAM

CIRCUIT DESCRIPTION

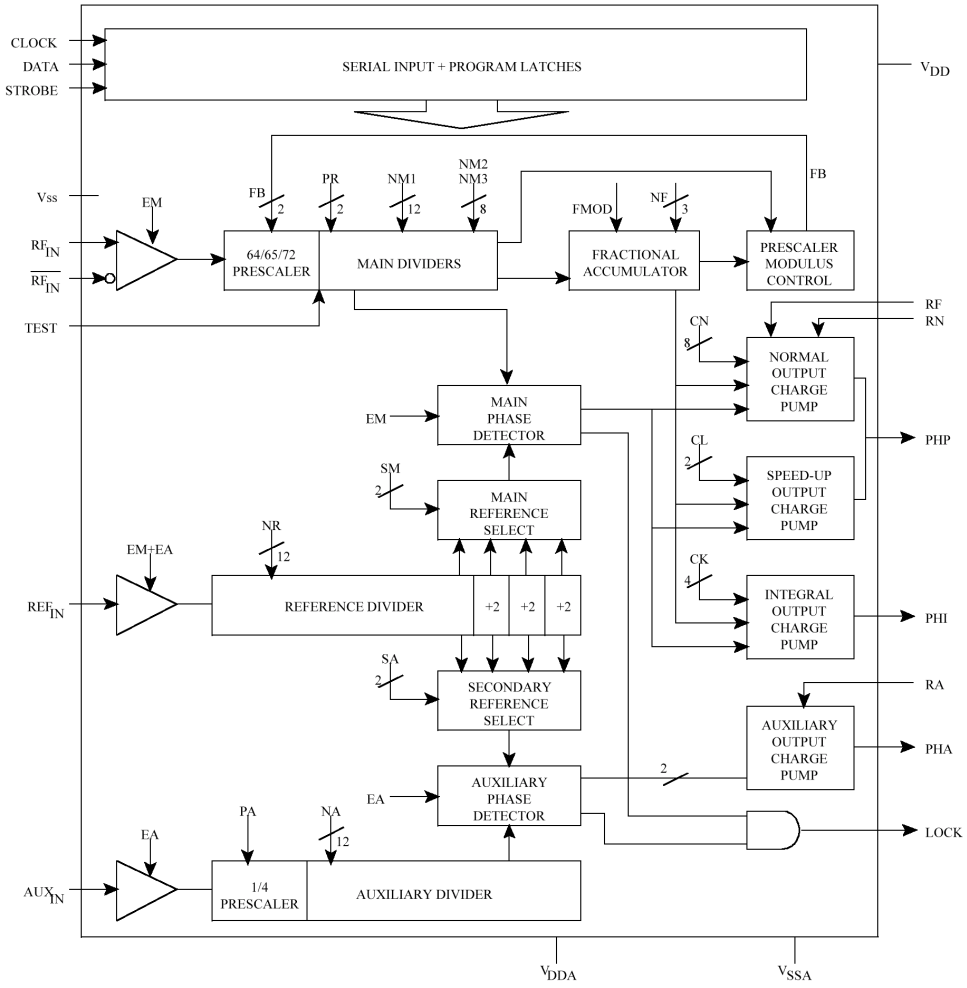

Figure 4-2 U801 SYNTHESIZER BLOCK DIAGRAM

CIRCUIT DESCRIPTION

4.2.2 VOLTAGE-CONTROLLED OSCILLATOR

Oscillator (Q850)

The VCO is formed by Q850, several capacitors and varactor diodes, and a ceramic resonator. It oscillates at the transmit frequency in transmit mode and first injection frequency in the receive mode (approximately 450 MHz in transmit and 500 MHz in receive).

Biasing of Q850 is provided by R862, R867 and R868. An AC voltage divider formed by C859, C861 and C862 initiates and maintains oscillation and also matches Q850 to the tank circuit. The ceramic resonator is grounded at one end to provide shunt inductance to the tank circuit.

Frequency Control and Modulation

The VCO frequency is controlled in part by DC voltage across varactor diodes CR854, CR855, CR856 and CR851. As voltage across a reverse-biased varactor diode increases, its capacitance decreases. Therefore, VCO frequency increases as the control voltage increases. CR854/CR855 and CR856/CR851 are paralleled varactor to divide the capacitance and improve linearity. The varactors are biased at -2V to adjust to the voltage output of U801. The control line is isolated from tank circuit RF by choke L851 and L854 and decoupling capacitor C854. The amount of frequency change produced by CR854/CR855/CR856/CR851 is controlled by series capacitor C853.

The -2V applied to the VCO is derived from the TCXO frequency that is amplified by Q833, rectified by CR831 and filtered by C844, C845, C846 and C847 on the RF board.

The VCO frequency is modulated using a similar method. The transmit audio/data signal is applied across varactor diode CR852 which varies the VCO frequency at an audio rate. Series capacitors C856/C870 set the amount of deviation produced along with CR853 and C858. R854 provides a DC ground on the anodes of CR852/CR853, and isolation is provided by R852 and C855.

The DC voltage across CR853 provides compensation to keep modulation relatively flat over the entire bandwidth of the VCO. This compensation is required because modulation tends to increase as the VCO frequency gets higher (capacitance of CR854/CR855/CR856/CR851 gets lower). CR853 also balances the modulation signals applied to the VCO and TCXO. An external voltage from J201, pin 14 can also adjust the modulation.

The DC voltage applied across CR853 comes from the modulation adjust control R810. R811 applies a DC biasing voltage to CR852; C814 provides DC blocking; and C818 attenuates AC signals applied through R811. RF isolation is provided by C858, R853, C817 and R812.

CIRCUIT DESCRIPTION

4.2.3 VCO AND REFERENCE OSCILLATOR MODULATION

Both the VCO and reference oscillator (TCXO) are modulated in order to achieve the required frequency response. If only the VCO was modulated, the phase detector in U801 would sense the frequency change and increase or decrease the VCO control voltage to counteract the change (especially at the lower audio frequencies). If only the reference oscillator frequency is modulated, the VCO frequency would not change fast enough (especially at the higher audio frequencies). Modulating both VCO and reference oscillators produces a flat audio response. Potentiometer R810 sets the VCO modulation sensitivity so that it is equal to the reference oscillator modulation
sensitivity.

4.2.4 CASCODE AMPLIFIERS (Q851/Q852)

The output signal on the collector of Q850 is coupled by L861/C864 to buffer amplifier Q851/Q852. This is a shared-bias amplifier which provides amplification and also isolation between the VCO and the stages which follow. The signal is direct coupled from the collector of Q852 to the emitter of Q851. The resistors in this circuit provide biasing and stabilization, and C865 and C866 are bypass capacitors.

4.2.5 AMPLIFIER (Q853)

Amplifier Q853 provides amplification and isolation between the VCO and receiver and transmitter. C868 provides matching between the amplifiers. Bias for Q853 is provided by R871, R872 and R874. Inductor L856 and capacitor C873 provide impedance matching on the output.

4.2.6 VOLTAGE FILTER (Q832)

Q832 is a capacitance multiplier to provide filtering of the 4.6V supply to the VCO. R836 provides transistor bias and C834 provides the capacitance that is multiplied. If a noise pulse or other voltage change appears on the collector, the base voltage does not change significantly because of C834. Therefore, base current does not change and transistor current remains constant. CR832 decreases the charge time of C834 when power is turned on. This shortens the start-up time of the VCO. C841, C840 and C855 are RF decoupling capacitors.

4.2.7 VCO FREQUENCY SHIFT (Q831)

The VCO must be capable of producing frequencies from approximately 403-564.95 MHz to produce the required receive injection and transmit frequencies. If this large of a shift was achieved by varying the VCO control voltage, the VCO gain would be undesirably high. Therefore, capacitance is switched in and out of the tank circuit to provide a coarse shift in frequency.

This switching is controlled by the T/R pin shift on J201, pin 4, Q831/Q834 and pin diode CR850. When a pin diode is forward biased, it presents a vary low impedance to RF; and when it is reverse biased, it presents a very high impedance. The capacitive leg is switched in when in transmit and out when in receive.

CIRCUIT DESCRIPTION

When J201, pin 4 is high in receive, Q834 is turned off, Q101 is turned on and the collector voltage goes low. A low on the base of Q102 turns the transistor on and the regulated +5.5V on the emitter is on the collector for the receive circuitry. With a low on the base of Q831 the transistor is off and the collector is high. With a high on the collector of Q831 and a low on the emitter of Q834, this reverse biases CR850 for a high impedance.

The capacitive leg is formed by C851, CR850, C852 and C876. When J201, pin 4 is low in transmit, Q834 is turned on and a high is on the emitter, Q101 is turned off and the collector voltage goes high. A high on the base of Q102 turns the transistor off and the regulated +5.5V is removed from the receive circuitry. With a high on the base of Q831 the transistor is on and the collector is low. With a low on the collector of Q831 and a high on the emitter of Q834, this forward biases CR850 and provides an RF ground through C851 and C852/C876 are effectively connected to the tank circuit. This decreases the resonant frequency of the tank circuit.

4.2.8 SYNTHESIZER INTEGRATED CIRCUIT (U801)

Introduction

Synthesizer chip U801 is shown in Figure 4-2. This device contains the following circuits: R (reference), Fractional-N, NM1 and NM2; phase and lock detectors, prescaler and counter programming circuitry. The basic operation was described in Section 4.2.1.

Channel Programming

Frequencies are selected by programming the R, Fractional-N, NM1 and NM2 in U801 to divide by a certain number. These counters are programmed by a user supplied programming circuit. More information on programming is located in Section .

As previously stated, the counter divide numbers are chosen so that when the VCO is oscillating on the correct frequency, the VCO-derived input to the phase detector is the same frequency as the reference oscillator-derived frequency.

The VCO frequency is divided by the internal prescaler and the main divider to produce the input to the phase detector.

4.2.9 LOCK DETECT

When the synthesizer is locked on frequency, the SYNTH LOCK output of U801, pin 18 (J201, pin 7) is a high voltage. Then when the synthesizer is unlocked, the output is a low voltage. Lock is defined as a phase difference of less than 1 cycle of the TCXO.

CIRCUIT DESCRIPTION

4.3 RECEIVER CIRCUIT DESCRIPTION

4.3.1 HELICAL FILTER (Z201), RF AMPLIFIER (Q201)

Capacitor C201 couples the receive signal from the antenna switch to helical filter Z201. (The antenna switch is described in Section 4.4.5.) Z201 is a bandpass filter tuned to pass only a narrow band of frequencies to the receiver. This attenuates the image and other unwanted frequencies. The helicals are factory set and should not be tuned.

Impedance matching between the helical filter and RF amplifier Q201 is provided by C203, C204 and L201. Q201 amplifies the receive signal to recover filter losses and also to increase receiver sensitivity. Biasing for Q201 is provided by R201, R202 and R203; and C208/C209 provide RF bypass. CR201 protects the base-emitter junction of Q201 from excessive negative voltages that may occur during high signal conditions. Additional filtering of the receive signal is provided by Z202. L202, and C205 provide impedance matching between Q201 and Z202. Resistor R204 is used to lower the Q of L202 to make it less frequency selective.

4.3.2 MIXER (U221), FIRST LO AMPLIFIER (Q301)

First mixer U221 mixes the receive frequency with the first injection frequency to produce the 52.95 MHz first IF. Since high-side injection is used, the injection frequency is 52.95 MHz above the receive frequency. The RF signal is coupled to the mixer through C206.

The first injection frequency from the VCO is coupled to the first local oscillator amplifier Q301 through C301. L301 and C302 match Q301 to the VCO. Bias for Q301 is provided by R301, R302 and R303, and C303 decouples RF signals. Impedance matching to the mixer is provided by L302, R304 and C304.

4.3.3 AMPLIFIER (Q222), CRYSTAL FILTER (Z221/Z222), IF AMP (Q221)

The output of U221 is coupled to buffer Q222. C222, R229 and Q222 match the 50 ohm output of U221. Bias for Q222 is provided by R228 and R229. The output of Q222 is matched to crystal filter Z221 via L222, C223 and R230. This filter presents a low impedance to 52.95 MHz and attenuates the receive, injection, and other frequencies outside the 52.95 MHz passband.

Z221 and Z222 form a 2-section, 4-pole crystal filter with a center frequency of 52.95 MHz and a -3 dB passband of 8 kHz (12.5 kHz BW) or 15 kHz (20/25 kHz BW). This filter establishes the receiver selectivity by attenuating the adjacent channel and other signals close to the receive frequency. C232, C224, and L223 adjust the coupling of the filter. L224, C225 and C227 provide impedance matching between the filter and Q221.

IF amplifier Q221 amplifies the 52.95 MHz IF signal to recover filter losses and improves receiver sensitivity. Biasing for Q221 is provided by R222, R223, R225 and R226 and C228, C229 decouple RF signals. The output of Q221 is coupled to the detector by C230.

4.3.4 SECOND LO AMP/TRIPLER (Q401), SECOND IF FILTER (Q901)

The input frequency to Q401 is 17.5 MHz from TCXO Y801 coupled through C402. Bias for Q401 is provided by R401, R402, R403 and R404. C403, C404 decouple RF from the amplifier. L401, L402, C405, C406 and C407 pass the third harmonic of the input (52.5 MHz) to U241, pin 1. The output of the amplifier is coupled to U241, pin 1 by C241, and C410 and L404 provided low frequency decoupling.

4.3.5 SECOND MIXER/DETECTOR (U241)

Oscillator and Mixer

As shown in Figure 4-3, U241 contains the second oscillator, second mixer, limiter, detector, and squelch circuitry. The 52.95 MHz IF signal is mixed with a 52.5 MHz signal produced by second LO amplifier Q401 from TCXO Y801.

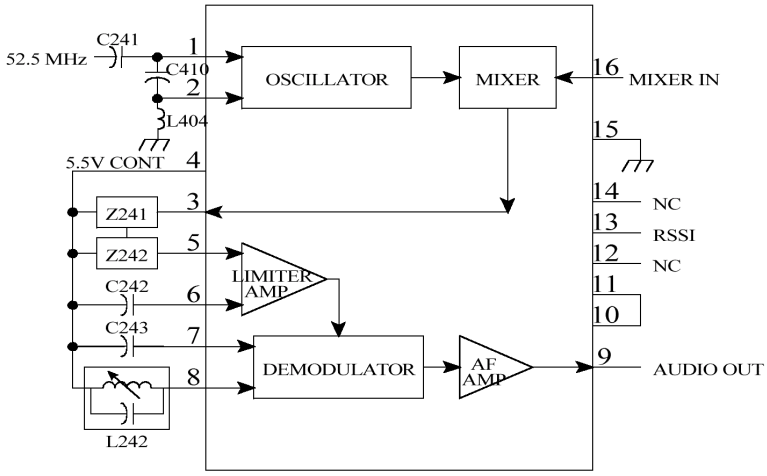

Figure 4-3 U241 BLOCK DIAGRAM

CIRCUIT DESCRIPTION

Second IF Filter

The output of the internal double-balanced mixer is the difference between 52.95 MHz and 52.5 MHz which is 450 kHz. This 450 kHz signal is fed out on pin 3 and applied to second IF filters Z241 and Z242. These filters have passbands of 9 kHz (12.5 kHz BW), 15 kHz (20 kHz BW) or 20 kHz (25 kHz BW) at the -6 dB points and are used to attenuate wideband noise.

Limiter-Amplifier

The output of Z241/Z242 is applied to a limiter-amplifier circuit in U241. This circuit amplifies the 450 kHz signal and any noise present; then limits this signal to a specific value. When the 450 kHz signal level is high, noise pulses tend to get clipped off by the limiter; however, when the 450 kHz signal level is low, the noise passes through. C242, C243 decouple the 450 kHz signal.

Quadrature Detector

From the limiter stage the signal is fed to the quadrature detector. An external phase-shift network connected to pin 8 shifts the phase of one of the detector inputs 90° at 450 kHz (all other inputs are unshifted in phase). When modulation occurs, the frequency of the IF signal changes at an audio rate as does the phase of the shifted input. The detector, which has no output with a 90° phase shift, converts this phase shift into an audio signal. L242 is tuned to provide maximum undistorted output from the detector. R242 is used to lower the Q of L242. From the detector the audio and data signal is fed out on pin 9.

Audio/Data Amplifier

The audio/data output of U241 on pin 9 is fed to the audio amplifier U261. U261 amplifies the detected audio/data signal and shifts the DC bias level to 2.5V. The gain is set at approximately 1.5 by R261/R262. R263 and R264 provide a 1.9V DC reference bias voltage. The audio output of U261 is applied to J201, pin 13.

Receive Signal Strength Indicator (RSSI)

U241, pin 13 is an output for the RSSI circuit which provides a current proportional to the strength of the 450 kHz IF signal. The voltage developed across R241 is applied to J201, pin 12.

4.4 TRANSMITTER CIRCUIT DESCRIPTION

4.4.1 BUFFER (Q851)

The output signal is applied to a 50-ohm pad formed by R851, R852, and R853. This pad provides attenuation and isolation. Q851 provides amplification and also additional isolation between the VCO and transmitter. Biasing for this stage is provided by R854, and decoupling of RF signals is provided by C852. Impedance matching with the transmitter is provided by L501 and C502.

4.4.2 PRE-DRIVER (Q501), DRIVER (Q521)

Pre-driver Q501 is biased class A by R501 and R502 and R506. L501 and C502 match Q501 to Q851. C520 and C508 bypass RF from the DC line, and R503 provides supply voltage isolation. R507 ties the +7.5V supply to the circuit for high power applications and R508 ties the circuit to +5V for low power applications. Impedance matching between Q501 and Q521 is provided by L502, L503 and C511. R504 and C504 provide negative feedback to prevent
oscillation.

Driver Q521 is biased nearly Class C by R521 and R522. Impedance matching with Q541 is provided by L521, C525, C527, L522 and C526.

4.4.3 -5V POWER CONTROL SUPPLY

The 17.5 MHz from the TCXO is coupled through C902 to Q901. Bias for Q901 is provided by R903, R904, R901, R902 and R905. C901 and C903 provide RF decoupling. The amplified signal rectified by CR901/CR902 to produce a -5V DC source. C909 stabilizes the voltage level and C910 and C911 provide RF decoupling. This -5V source is used in the transmit power control circuit U542.

4.4.4 FINAL (Q541), POWER CONTROL (U542)

Q541 is biased for Class C operation. The output is matched to the low-pass filter by L541, C552, and several capacitors. The supply voltage is isolated from RF by ferrite bead EP541.

Power control is provided by U542. The 5.5V transmit supply is passed by U542 to power adjust R542. The other end of R542 is the rectified -5V from Q901. This negative voltage is required when low power is used to pinch off Q541 to the required output.

The low-pass filter consists of L561, C561, L562, C562, L563, C563 and L564. The filter attenuates spurious frequencies occurring above the transmit frequency band. The transmit signal is then fed through the antenna switch to antenna jack J501.

4.4.5 ANTENNA SWITCH (CR561, CR562)

The antenna switching circuit switches the antenna to the receiver in the receive mode and the transmitter in the transmit mode. In the transmit mode, +7.5V is applied to L565 and current flows through diode CR561, L566, diode CR562, and R562/R563. When a diode is forward biased, it presents a low impedance to the RF signal; conversely, when it is reverse biased (or not conducting), it presents a high impedance (small capacitance). Therefore, when CR561 is forward biased, the transmit signal has a low-impedance path to the antenna through coupling capacitor C568.

CIRCUIT DESCRIPTION

C567, L566, and C570 form a discrete quarter- wave line. When CR561 is forward biased, this quarter-wave line is effectively AC grounded on one end by C570. When a quarter-wave line is grounded on one end, the other end presents a high impedance to the quarter-wave frequency. This blocks the transmit signal from the receiver. C569 matches the antenna to 50 ohms in transmit and receive.

In the receive mode, no power is applied to L565, so all the diodes are “off”. The receive signal then has a high-impedance path into the transmitter and a low-impedance path into the receiver because the quarter-wave line is not grounded.

5.0 VTU Circuits Determining Frequency

The Data Transceiver transmit frequency selection is under the full control of the application microprocessor (U1) firmware programming. Programming of the microprocessor firmware and therefore operational frequencies is accomplished only at the factory. Operators of VTU equipment have no provisions for selecting or designating receiver or transmitter frequencies. Servicing and maintenance of VTUs will be provided at the factory or by approved service centers. Special test support gear is required to allow special VTU testing, including frequency selection, required for FCC part 90 certification.

The Digital Baseband board application microprocessor (U1) sends control information to the Data Transceiver to 1) lock and unlock the synthesizer frequency (Sync Enable, JP1, pin 8) 2) provide synthesizer frequency selection data (Sync Data, JP1, pin 9) and 3) synthesizer clocking information (Sync Clock, JP1, pin 10). Control of synthesizer frequencies is to resolution of 6.25 kHz. Algorithms and bit sequences required to fully control the synthesizer are described in subsequent paragraphs and are direct excerpts from High Specification Data Transceiver Service Manual Part No. 242-3474-xx0.

Splatter Filters and DC bias control on the modulated audio pumped into the Data Transceiver ensures that the synthesizer frequency is not shifted and excessively spread by modulation. The Data Transceiver uses the synthesized base frequencies along with a 52.95 MHz IF frequency to create the UHF channel frequencies modulated by the Digital Baseboard provided audio.

5.1 Data Transceiver Synthesizer

The VCO output signal is the receiver first injection frequency in the receive mode and the transmit frequency in the transmit mode. The first injection frequency is 52.95 MHz above the receive frequency. The frequency of this oscillator is controlled by DC voltage produced by the phase detector in the synthesizer chip U801.

Channels are selected by programming counters in the U801 to divide by a certain number. This programming is performed over a serial bus and provided by the Digital Baseband board.

The frequency stability of the synthesizer in both receive and transmit modes is established by the stability of the reference oscillator described in subsequent sections. This oscillator is stable over a temperature range of –30deg to +60deg C.

5.2 High Specification Data Transceiver Synthesizer Data Programming

SECTION 2

INSTALLATION

2.1 PRE-INSTALLATION CHECKS

Field alignment should not be required before the 3474 is installed. However, it is a good practice to check the performance to ensure that no damage occurred during shipment. Performance tests are located in Section 6.2.

2.2 INTERFACING WITH DATA EQUIPMENT

2.2.1 DM3474 ONLY

Connector J201 on the data transceiver PC board provides the interface with the data equipment. This is a 14-pin female connector with .025" square pins on 0.1" centers (Dupont 76308-114).

The following is a general description of the various J201 input and output signals.

Pin 1 (Ground) - Chassis ground.

Pin 2 (+7.5V DC Continuous) - This voltage should be stabilized near +7.5V DC. Variations from +6V to +9V can change power output as much as 6 dB.

Pin 3 (+7.5V DC Transmit) - This input should be +7.5V DC in transmit mode only.

Pin 4 (+5V DC Receive Control Line) - This input should be +5V DC in the receive mode only, ≤ 0.3 V DC in Tx, input impedance ≥ 10k ohms.

Pin 5 (+5V DC Continuous) - This voltage should be stabilized near +5V DC.

Pin 6 (Tx Input) - Provides a response of ±1.5 dB from DC to 5 kHz. The sensitivity is approximately 7 kHz deviation per volt RMS. When this input is used, a temperature compensated 2.5V DC bias is required because variations in voltage cause the frequency to change. In addition, the transceiver regulatory compliance must be applied for with the customer supplied modulation limiting/filter circuit and chassis.

Pin 7 (Synthesizer Lock) - Output from synthesizer lock detect circuit. Low = unlocked, high = locked.

Pin 8 (Synthesizer Enable) - Latch enable signal. A rising edge on this input latches the data loaded into synthesizer IC U801.

Pin 9 (Synthesizer Data) - Serial data line used for programming synthesizer IC U801.

Pin 10 (Synthesizer Clock) - Software generated serial clock. Data is valid on the rising edge of this signal.

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Pin 11 (Carrier Detect) - This output is not used at this time.

Pin 12 (RSSI Output) - The RSSI (Receive Signal Strength Indicator) output provides a voltage that increases in proportion to the strength of the RF input signal.

Pin 13 (Rx Output) - The data output level is 600-1200 millivolts P-P (200-400 mV RMS) with a modulation signal of 1 kHz at 60% of maximum deviation. The output is DC coupled and referenced to +2.5V DC. Load impedance should be 10k-100k ohms.

SECTION 3

PROGRAMMING

3.1 INTRODUCTION

The information in Section 3.2 describes synthesizer programming protocol. This information can be used as a basis for designing the synthesizer programming hardware and software required.

3.2 DM3474 SYNTHESIZER DATA PROTOCOL

Programming of the dividers and the charge pumps are performed on a 3-line bus; SYNTH ENABLE, SYNTH DATA, AND SYNTH CLK. On initial power up three 34-bit words are required to load the 3474 Data Transceiver. After the initial load, one 32-bit word can be used to change channels.

The SA7025 Synthesizer IC uses four address words; D, C, B and A (see Figure 3-4). The C word is not used in the 3474. The 24- and 32-bit words contain one or four address bits, depending on the address bits, the data is latched into registers. When the A-word is loaded, the data of these temporary registers is loaded together with the A-word into the work
registers.

3.2.1 D-WORD

Refer to Figure 3-1.

TCXO Reference Frequency is 17.5 MHz.
Loop Reference Frequency is 50 kHz.
Reference Divide (NR) = 17.5 MHz ÷ 50 kHz =350 Decimal or 000101011110 Binary.

The 3474 has frequency resolution of 6.25 kHz and 10 kHz. When programming 6.25 kHz frequency resolution use FMOD=8. When programming 10 kHz frequency resolution use FMOD=5.

Example:

(FCM) ÷ FMOD = 50 kHz ÷ 8 = 6.25 kHz
(FCM) ÷ FMOD = 50 kHz ÷ 5 = 10 kHz

Where:
FCM = Loop Reference Frequency
FMOD = Fractional N Modulus

Since FMC is the same for both 6.25 kHz and 10 kHz the loop dynamics are very similar and the same loop filter values can be used.

PROGRAMMING

3.2.2 B-WORD

The B-Word is 24-bits long (see Figure 3-2). It contains the Address, Charge Pump setting factor (CN), Binary Acceleration factors (CK, CL), and Prescaler Type (PR).

The Charge Pump Current setting (CN) could be changed on a channel-by-channel basis for ultimate rejection of the Fraction N spurious responses close into the carrier frequency. The 3474 synthesizer has an adjust (R855) for the fractional compensation current. The factory preset value will allow CN to be set to the following ranges:

Frequency in a Band	CN
Lowest TX	86
Highest TX	90
Lowest RX	96
Highest RX	100

The value of CN should be interpolated for frequencies between the band edges. With these recommended values of CN, the transceiver should have the fractional spurs minimized far below the levels needed to make ETSI 70 dB adjacent channel RX or TX
specifications.

Example:

Model 3474-530 is a 450-466 MHz transceiver.
458 MHz TX CN = 88 01011000 Binary
458 MHz RX CN = 98 01100010 Binary

3.2.3 A-WORD

The A-Word must be sent last (see Figure 3-3). The A-Word contains new data for the loop dividers and is programmed for every channel. The A-Word can be a 24-bit or 32-bit word depending on the state of the flag LONG in the D-Word. The 24-bit word (A0) is sent if LONG=0 and the 32-bit word (A1) is sent if LONG=1. The extra 8-bits in A1 are the CN charge pump settings. Upon power up the D-, B- and A-Words must be sent, but after that only the A1 word needs to be sent.

The Fractional-N increment (NF) is a 3-bit word that is channel dependent. NF is used to program the sub-channels below the 50 kHz Loop Reference frequency. FCM = 50 kHz and if FMOD = 8, then the Fractional-N increment is: 50 kHz ÷ 8 = 6.25 kHz

To program an 18.75 kHz channel:

NF = 18.75 kHz ÷ 6.25 kHz
NF = 3

PROGRAMMING

NM1 and NM2 are calculated as follows:

N = (NM1 + 2) x 64 + NM2 x 65 Where: N = total division ratio

NM1 = Number of main divider cycles when prescaler modulus equals 64

NM2 = Number of main divider cycles when prescaler modulus equals 65

Example:

Calculate NM1 and NM2 to Receive 454.500 MHz.

LO = 454.5 + 52.95 = 507.45 MHz
(52.95 MHz IF with High Side Injection)

N = RX LO ÷ FCM = 507.45 ÷ 0.05 = 10149
(FMC = Loop Reference Frequency)

NM2 = 64 x FRAC [N ÷ 64]
= 64 x FRAC [10149 ÷ 64]
= 64 x 0.57813
= 37

NM1 = INTEGER [N ÷ 64] - 2 - NM2
= 158 - 2 - 37
= 119

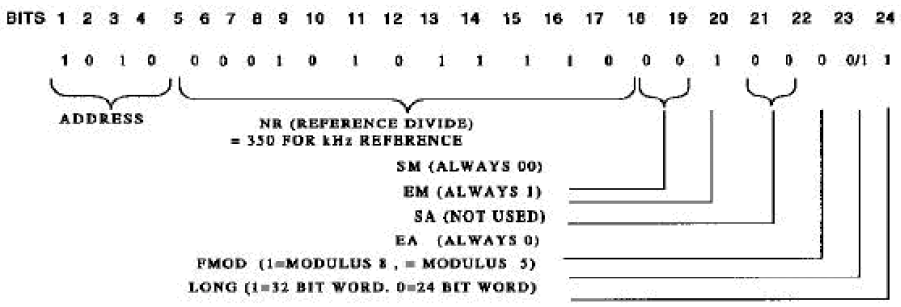

Figure 3-1 D-WORD

PROGRAMMING

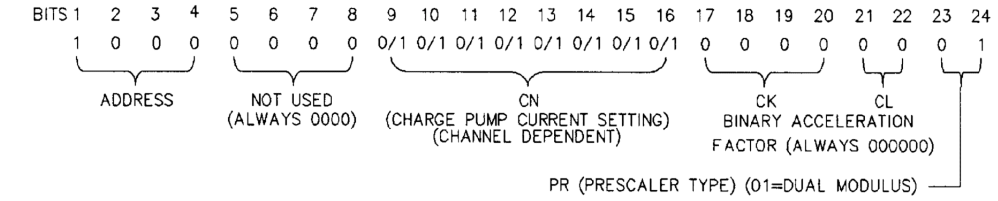

Figure 3-2 B-WORD

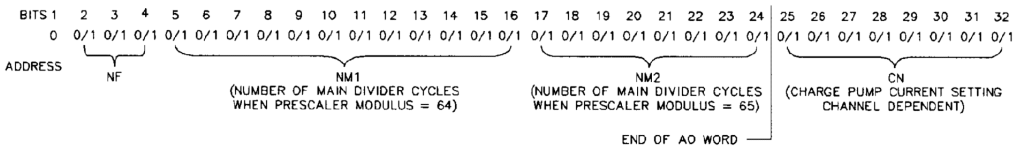

Figure 3-3 A-WORD

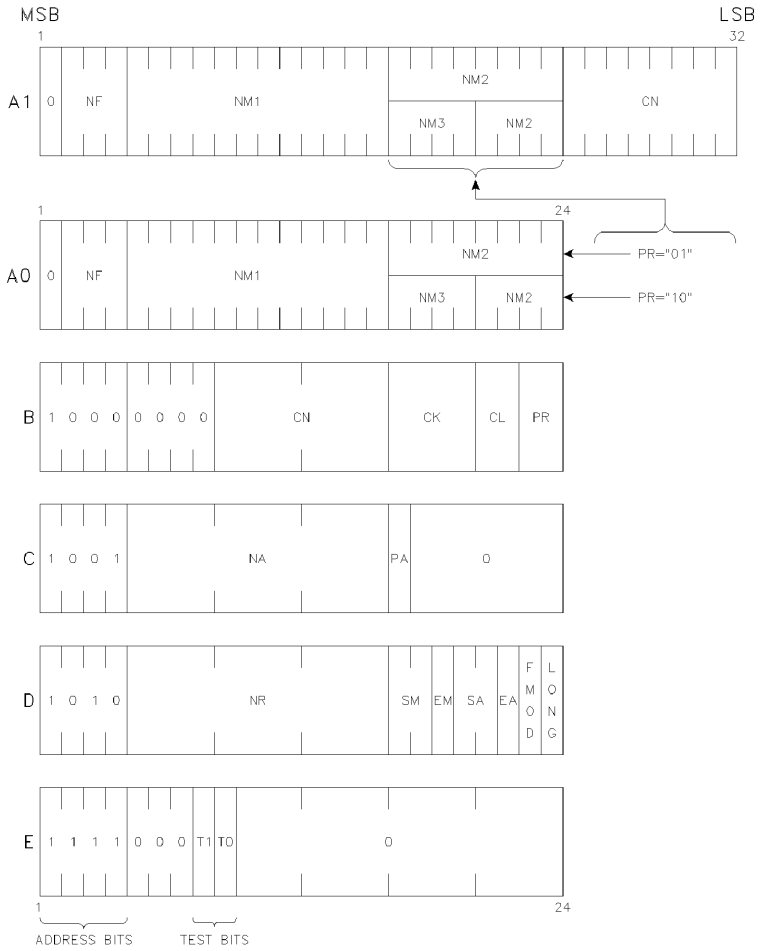

Figure 3-4 SERIAL INPUT WORD FORMAT

PROGRAMMING

3.3 RECEIVE TO TRANSMIT SEQUENCE

Refer to Figure 3-5.

1. Synthesizer is loaded (B and A 24-Bit words or one long 32-bit A-Word).

2. The state of the 5RCL line does not have to be changed until the last bit is sent. However, RX will cease as soon as it is changed.

3. The SYNTH ENABLE line should be held HIGH for 2 to 3 milliseconds after the last word is sent. This puts the frequency synthesizer in a SPEEDUP MODE and slightly improves lock times.

4. After the last word is strobed in, 7 milliseconds (worst case) should elapse before 7.5 TX is turned ON. This allows the synthesizer to come within 1 kHz of the desired frequency.

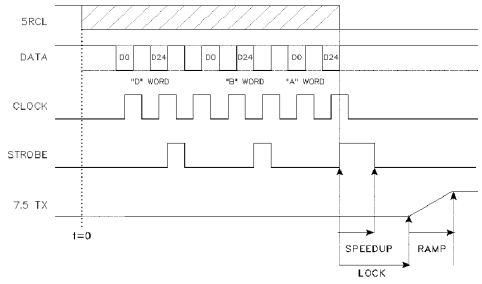

Figure 3-5 RX TO TX TIMING DIAGRAM

Dekey is a length of time to allow the TX to power down while the synthesizer is still in lock. This is needed to meet ETSI (European Telecommunications Standards Institute) adjacent power specifications. Dekey is approximately 3 ms in length. The 7.5 TX should be ramped or optimally filtered in such a way as to reduce the Sinx/x power spreading. Speedup will slightly improve lock times and is 1 to 2 ms.

PROGRAMMING

3.4 TRANSMIT TO RECEIVE SEQUENCE

Refer to Figure 3-6.

1. 7.5 TX is turned OFF. For best TX adjacent channel power performance this could be shaped.

2. The synthesizer load process could begin slightly before, but when the last bit is strobed in the synthesizer it will become unlocked. For ETSI specs, the TX should be turned OFF “on-frequency”.

3. The 5RCL line should switch from low to high AFTER the 7.5 TX is switched. The 5RCL not only turns the RX circuits on but also Pin Shifts the VCO.

4. For quickest lock times the SYNTH ENABLE line on the last load word should be held high for 2 to 3 milliseconds. It MUST NOT be left high as the synthesizer in the SPEEDUP mode has poor noise performance and would degrade the RX performance.

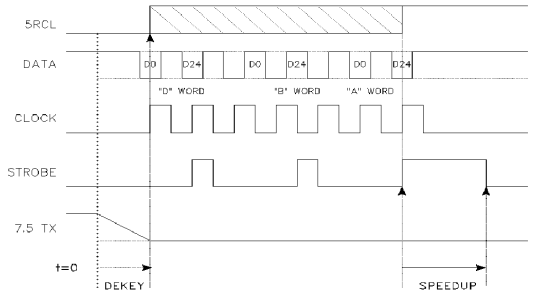

Figure 3-6 TX TO RX TIMING DIAGRAM

Speedup is 2 to 3 ms
Lock is approximately 7 ms
Ramp is approximately 3 ms

IMPORTANT

If the receiver is to be operated at 510-512 MHz (-810), a spurious condition may occur to degrade the receiver sensitivity 2 to 3 dB. If this degradation is unacceptable, the synthesizer can be reprogrammed to a comparison frequency (FCM) of 31.25 kHz (so that a multiple of this would not be 52.95 MHz) and a modulus (FMOD) of 5 with a reference divide (NR) of 560. These parameters place the spurious at harmonics of 31.25 kHz (instead of 50 kHz) outside the passband of the IF filters where the sensitivity is not degraded.

6.0 Circuits Suppressing Spurious and Harmonic Emissions

Circuits to suppress high frequency content and over modulation of the GMSK modulated audio signal transferred to the Data Transceiver are present on the Digital Baseband Board and are described in Sections 4.2.2.

Circuits to suppress spurious and harmonic emissions related to the Data Transceiver transmit section are described in Section 4.5.