4.0 VTU Circuit Description

4.1 Introduction

The main subsystems of the VTU are OEM Data Transceiver, OEM GPS Receiver, and Digital Baseband Board. A block diagram of critical RF circuitry is depicted in Section 2.

4.2 Digital Baseband Board

The Digital Baseband Board handles all I/O external to the VTU and all I/O functions to and from the OEM GPS Receiver and OEM Data Transceiver.

4.2.1 Microprocessor (U1), RAM/ROM (U3,U2,U9)

The Microprocessor in conjunction with the RAM/ROM memory executes programming to control all I/O functions, process receive and transmit data, control all functioning on the Digital Baseband Board and with the Data Transceiver and GPS Receiver. A 8 MHz clock generates pulses used by the microprocessor to execute programming, clock I/O and program the synthesizer. Programming information is fed out on enable, data, and clock lines and is distributed by buffers to other digital components.

The microprocessor provides receiver and transmitter control information including Synchronization Enable (PA5/JP1, pin 8), Synchronization Data (PD3/JP1, pin 9), Synchronization Clocking (PD4/JP1, pin 10) through digital buffers (U13) to the Data Transceiver. The Data Transceiver is mated to the Digital Baseband Board via the Data Transceiver interface board described in section 4.3. The microprocessor receives a Synchronization Lock indication (JP1, pin 7) directly from the Data Transceiver. The microprocessor receives a Carrier Detection (PA7) indication from the Carrier Detection logic on the Digital Baseband Board. The same Carrier Detection indication is provided directly to the Data Transceiver (JP1, Pin 11).

The microprocessor also provides transmit data (Txdata) and accepts received data (Rxdata) from the MX909 Modem (U12) via data lines D0 through D7. Data and control information exchanged between the OEM GPS Receiver and external to the VTU occurs through the RS232 interface controlled by U23 and U24.

4.2.2 Splatter Filter and Bias Control

The modulated transmit signal is coupled to and shaped by a two stage splatter filter (U15, U28). The splatter filter is a low pass filter that attenuates frequencies above defined value related to the modulation rate. The purpose of the splatter filter is to prevent over modulation of the transmited audio signal before it is presented to the Data Transceiver.

The output from the splatter filter is fed to a gating circuit (U29) that imposes a +2.5V

DC, +/- 0.1V bias on the audio signal. This bias level is adjusted via VR1 based on factory alignment procedures. Bias control of the modulated audio signal is required to maintain accurate receive and transmit frequencies with the Data Transceiver. The output of the gate circuit is presented to the Data Transceiver interface board on JP1, pin 6.

4.2.3 Rxout Amplifier and DC Bias Control

Received audio signals from the Data Transceiver (JP1, pin 13) are buffered, amplified and bias controlled before transfer to the MX909 Modem chip (U12). Audio signals are first buffered by U10(pins 12,13,14) and then amplified by U10(pins 8, 9, 10) with an above unity gain. R36 is adjusted to yield a +2.5V DC, +/- 0.1V signal bias using factory alignment procedures. DC bias control is needed to minimize BER on receive data derived from the MX909 modulation process.

4.2.4 Carrier Detection

RSSI signals presented by the Data Transceiver (JP1, pin 12) are used to declare carrier detection. The RSSI signal has a voltage level that increases in proportion to increases in the received signal strength at the Data Transceiver IF frequency.
The RSSI signal is first buffered by U10(pins 2,3,4) and then applied to amplifier/comparator U10(pins 5,6,7). When the RSSI signal reaches the reference voltage the output goes low. Low output indicates a carrier of significant strength (greater than 110 dBm) and a high output indicates no carrier present condition. Potentiometer R47 allows the setting of the reference voltage level providing hysterisis for weak and fading signals.

4.2.5 Receiver/Transmit Switching Control

Circuits on the Digital Baseband Board under the control of the microprocessor (U1) provide switched voltages to the Data Transceiver to control receive and transmit functions. Switched +8V DC is presented at JP1, pin 3 for control of transmit functions and +5V DC is presented at JP1, pin 4 for control of receive functions. Additionally non switched +8V DC and +5V DC are presented at JP1, pins2, 3 and 14.

4.2.6 RS-232 Modem

The RS232 modem (U23, U24) support a data interface between 1) the Digital Baseband Board microprocessor and the GPS Receiver card and 2) the Digital Baseband Board microprocessor and external devices to the VTU. External devices interfacing via the RS232 typically consist of data digital display device.

The RS232 port is operated at a 9600 Baud rate and is designed to be compatible with the RS232 standard of the Electronic Industries Association (EIA). This standard specifies pin assignments and voltage levels associated with the interface between data terminals and data communications equipment. Equipment connected to this modem should be compatible with this standard.

4.2.7 Modem Data Pump

The Modem Data Pump (U12/MX909A) is microprocessor device that contains all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for GMSK Wireless operation.

In the transmit mode, the modem assembles application data received from the data microprocessor (U1), adds forward error correction (FEC) and error detection codes, time spreads this data by interleaving and scrambles the bit pattern. After adding the bit and frame sync code words, the data packets are converted into GMSK signals for modulating the Data Transceiver transmitter. Before the Data Transceiver receives the modulated audio it is passed through the splatter filter (U15,U28) and adjusted for DC signal bias. It is then passed to the Data Transceiver interface board where a final bias adjustment is made and the signal can be inverted. Inversion is selected by the positioning a jumper on pins 1 and 2 of J3 on the interface board.

In the receive mode, the modem performs the reverse functions as is performed in the transmit mode after demodulating the receiver signal. The demodulated signal information is unscrambled, de-interleaved, error corrected and packet overhead data is removed. Final recovered application data is provided to the data microprocessor. CRC detected residual uncorrected data errors are flagged and SNR of received packets are also provided.

The modem is driven by a 4.9152 MHz oscillator used as a source generating the composite sine waves making up the GMSK modulation waveform.

4.3 Data Transceiver Interface Board

The data transceiver is connected to the baseband board through an interface board. This board provides a physical mounting connection and the option to invert the baseband signal before going to the transceiver. The inversion is selected by jumpering pins 1-2 of J3 on the interface board. In this configuration of the VTRAK unit this jumper connection is made. The inverting amplifier on the board, U1, also provides a final bias adjustment via potentiometer R11. The bias must be set to 2.5 VDC +/- 0.1 VDC. The interface board passes all other signals directly to the Data Transceiver without modification.

4.4 Data Transceiver

The Data Transceiver is a Dataradio Corp. DM-3464 model (High Specification Data Transceiver Part Number 242-3464-680) synthesized VHF receiver/transmitter operating in the 150 through 174 MHz frequency range utilizing 12.5 kHz channels. Transmitted power output is 2 watts nominal and operation is simplex. The Data Transceiver interfaces with the Digital Baseband Board via connector JP1 and the Data Transceiver interface board. The transceiver is internal to the VTU.

Descriptions of circuit operation for the Data Transceiver is provided in Section 4.8 and is excerpted from the High Specification Transceiver Part No. 242-3464-680 Technical Manual.

4.5 GPS Receiver

The Oncore GPS Receiver has 12 independent receiver channels that track GPS satellite signals in both code and carrier phase. Time recovery and utilization of differential GPS corrections are integrated features. On achieving a full solution, the GPS receiver presents position, velocity, heading, time as 1PPS and status representing the GPS receive antenna. The GPS Receiver generates no intentional transmissions to perform its functions.

The GPS Receiver interfaces with the Digital Baseband Board via an RS232 port across connector JP2. The 12 independent receivers track the L1 GPS signal (1575.42Mhz) and operates off the clear /acquisition (C/A) carrier tracking. RF signals from the antenna port are down converted to IF frequency and then passed to Channel code and carrier digital correlators where a single high speed analog-to-digital converts IF to a digital sequence. Further digital processing performs code correlation, filtering, tracking and signal detection.

Full GPS solutions are transferred via the RS232 port to the Digital Baseband Board microprocessor.

4.6 Transmit Data Processing

After transmit messages are formatted and assembled with required control information with the data microprocessor (U1) the data is transferred through a serial port to the MX909A modem (U12) where the information is temporarily buffered. The modem scrambles and modulates the data to create an audio signal in real-time to forward to the Data Transceiver. Before the Data Transceiver receives the modulated audio signal it is filtered and biased.

4.7 Receive Data Processing

Received signals are down converted to audio signals by the Data Transceiver and based to the Digital Baseband Board as Rxout and overall signal level indication RSSI. The RSSI is processed by a comparator generating a Carrier Detect indication used by both the data microprocessor (U1) and the Data Transceiver. Rxout is amplified and biased before transfer to the modem microprocessor (U12) for demodulation and data extraction. Extracted data is transferred from the modem microprocessor to the application microprocessor for final data extraction, data processing and presentation to I/O.

4.8 Data Transceiver Circuit Description

SECTION 4

CIRCUIT DESCRIPTION

4.1 GENERAL

4.1.1 INTRODUCTION

The main functional blocks of this transceiver include the Transmitter, Receiver, Synthesizer/VCO, and TCXO. A block diagram of the transceiver is shown in Figure 4-1.

The VCO board is enclosed by a metal shield and soldered directly to the RF board.

The 3464 has a reference oscillator (TCXO) stability of ±2.5 PPM.

4.1.2 SYNTHESIZER / VOLTAGE CONTROLLED OSCILLATOR (VCO)

The purpose of a synthesizer is to "lock" the radio on the desired frequency of operation. U811 is the integrated circuit (IC) that provides this function. A temperature compensated crystal oscillator (TCXO Y801) is used to set the reference for the synthesizer. This oscillator operates at 14.85 MHz for 132-150 MHz band radios and 17.5 for 150-174 MHz band radios. Refer to Section 5 for how to check and adjust this component.

Pins 8, 9, and 10 of J201 provide the serial interface (clock, data, enable) from the microprocessor to the synthesizer IC. Pin 7 provides a "lock" detect indication to the microprocessor.

Pin 5 of J201 on the transceiver is the transceiver enable.

4.1.3 TRANSMITTER

When transmit mode is initiated, the user disables the receiver by applying a "low" on the RX enable (J201 pin 4). A "shaped" supply voltage is applied to J201 pin 3 (7.5 Tx).The 7.5 Tx line supplies power to the pre-driver (Q501), driver (Q521), to the gate of and final amplifier (Q541). The 7.5 Tx line provides bias to the antenna switch diodes (CR571 and CR572) which switches the antenna port to the transmitter output. A 7 pole lowpass filter at the output of the final amplifier provides harmonic filtering.

Pin 6 of J201 on the transceiver is the Tx modulation input to the transmitter. This signal is used to modulate the TCXO and VCO on the transceiver. The modulated signal is applied to the transmitter at the desired channel of operation.The modulation flatness adjustment on the transceiver is optimized at the center of the band and pre-adjusted in the factory. Refer to Section 5 for modulation adjustments.

4.1.4 RECEIVER

The receiver is an FM dual down conversion superheterodyne configuration with a first IF frequency of 21.45 MHz and second IF frequency of 450 kHz. In receive mode, the 7.5 Tx supply on J201 pin 3 is turned off disabling the transmitter. The antenna switch diodes are biased off which switches the antenna port to the receiver input. The user applies 5Vdc to the receiver enable input (J201 pin 4) which switches power to the receiver and shifts the VCO to the receive local oscillator band. The received RF signal is passed through the antenna switch to the two pole front-end bandpass filter formed by L201, C204, CR281, L202, C205, L203, and CR282. The signal

is applied to the low noise amplifier (Q202) and a second three pole bandpass filter, similar to the two pole bandpass filter previously described. The bandpass filters are tuned by voltage variable capacitors and are adjusted to the desired operating frequency via variable resistor R920. (Refer to Section 5 for steps to follow to tune the receiver to the desired frequency.)

The RF signal is then applied to the Mixer (down converter) U231 where it is converted to the IF frequency by mixing with the appropriate local oscillator frequency from the Synthesizer/VCO. The 21.45 MHz IF is applied to buffer amp Q231 and crystal filters Z231/Z232. The IF signal is then applied to the Demodulator IC (U241) where it is converted to 450 kHz by mixing with the second phase-locked local oscillator section of U241and filtered by Z241/Z242. The recovered audio signal is applied to J201 pin 13. The Receive Signal Strength Indicator (RSSI) is an analog voltage derived from the demodulator IC U241. This voltage ranges from approximately 0.5 to 2.5 Vdc and is representative of the signal strength of the received signal.

CIRCUIT DESCRIPTION

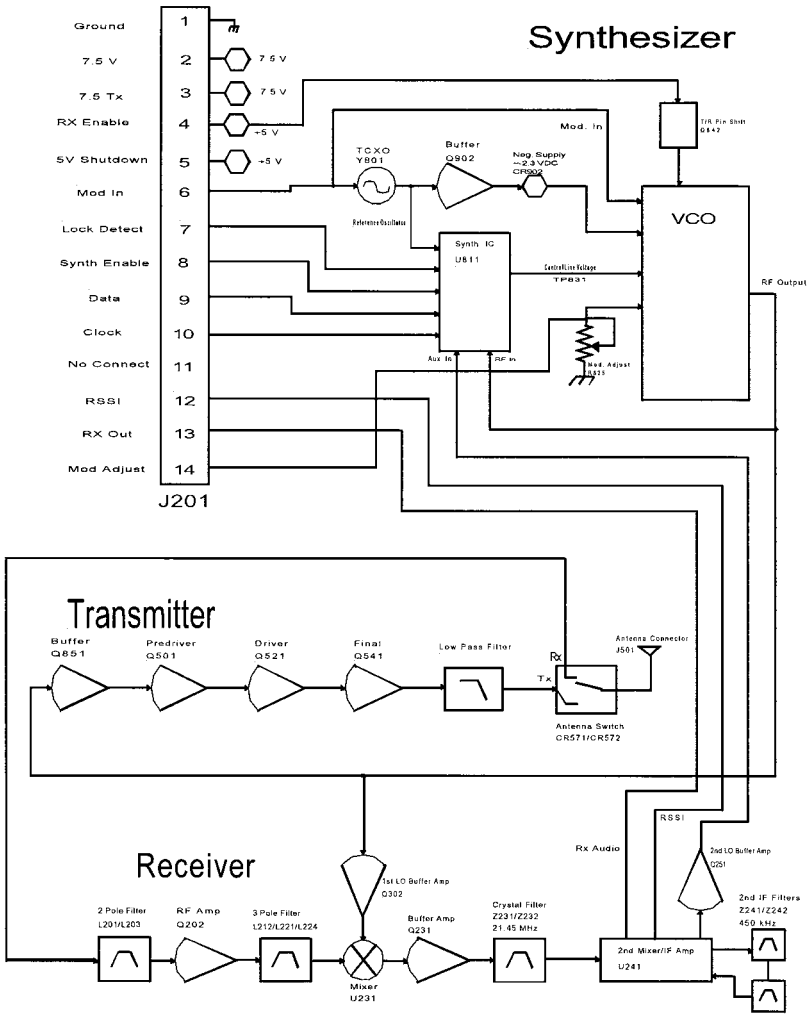

Figure 4-1 Data Transceiver Block Diagram