Virtual Wire Link Test

A received message is displayed on a single line in the MESSAGES RECEIVED window, whether it is made up of one or more packets. When the whole message is received, it is displayed. If a multi-packet message is partially received and then the first packet of new message is received, the partial message is discarded and reception of the new message is begun.

When text reaches the bottom of the MESSAGES RECEIVED or the MESSAGES SENT window, the text will scroll until ALT-C is invoked to clear all windows, When 79 characters are input or the Enter Key is pressed in the ENTER MESSAGE TO SEND window, this window is cleared and the cursor moves back to the left side of the window.

In the event that the link between the PC and the protocol board is lost (low battery voltage, ON/OFF switch off, no cable, etc.) a TIME OUT - VW UNIT NOT RESPONDING alarm message will be displayed. If a packet is unacknowledged after eight tries, a LINK FAULT message will be displayed in the STATUS column of the MESSAGES SENT window.

There are many other possible ways to interact with the Virtual Wire® Link Layer Protocol. The main purposes of the terminal program is to demonstrate software handshaking with the protocol and to support initial Demo Kit testing.

5 Theory of Operation

5.1 Data Radio Boards

I/O Interface- Referring to the Data Radio Board schematic diagram, connector P1 is the interface connector to the protocol board. Pin 1 is the transmitter data input and can be driven directly by a CMOS gate. The transmitter is pulse ON-OFF modulated by a signal

on this line changing from 0 volts to Vcc ±0.3 volts. A high level turns the transmitter oscillator on and a low level turns it off. The input impedance to this line is approximately 18K ohms. Pin 2 is the Vcc line for the transmitter. Vcc can be applied to this line on a continuous basis without a current penalty, since the transmitter does not draw current until the data input line is pulled high.

Pin 3 is the PTT line that enables the transmit mode. This line puts the transmit/receive RF switch in the transmit mode when it is high (2.5 volts minimum at 2.0 mA maximum). Pin 4 provides power to the receiver AGC circuitry, 2.7 to 3.3 volts. Pin 5 is ground. Pin 6 is a reference voltage output (VRef) from the hybrid receiver that is used in the "low battery" detection process on the protocol board. Pin 7 provides power to the receiver hybrid, 2.7 to 3.3 volts. Pin 8 is the data output from the comparator in the receiver hybrid. This data output is CMOS compatible and is capable of driving a single CMOS gate. The last connection to the data radio board is the 50 ohm antenna input. The antenna can either be connected directly to the board or connected remotely by using a 50 ohm coaxial cable.

Transmitter- Referring to the Data Radio Board schematic diagram, the RF transmitter is an HX surface mount hybrid. Pin 1 of the HX device is the transmitter data input previously discussed as connected directly to Pin 1 of connector P1. Pin 2 is the transmitter Vcc (power) connection. The HX hybrids are specified to draw a maximum peak current of 10 to 11 mA with a Vcc of 3 volts. Since the transmitter is only turned on when the data line is high, the average transmitter current depends on the duty cycle of the incoming data. Pin 3 of the HX device is ground and Pin 4 is the RF output. The RF output power of the HX is nominally 0 dBm with a 50 ohm load. The transmitter power is applied to the antenna port through the transmit/receive switch, Q1. When the PTT line is pulled high, Q1 is turned on to connect the transmitter to the antenna, Q3 is turned on to short the receiver input to ground and Q2 is turned off to disconnect the receiver input from the antenna during transmission.

Receiver- The receiver itself is an RX hybrid receiver. The architecture, theory and operational characteristics of this receiver are included in the application note, "New UHF Receiver Architecture Achieves High Sensitivity and Very Low Power Consumption". The Vcc is applied to Pin 1 of the hybrid from Pin 7 of connector P1. A 10 uF bypass capacitor, C5, is also connected to this pin. This capacitor is necessary to keep the RX internal comparator switching noise out of the data base-band amplifier circuitry in the RX. Pin 2 is the base-band data output. The signal at Pin 2 is the demodulated filtered data before it is applied to the comparator input. The Pin 2 output is dc coupled to the internal detector output. The output from Pin 2 is connected to the comparator input, on Pin 3, by the coupling capacitor, C6. The value of the coupling capacitor is determined by the longest pulse width to be encountered in the data stream. The capacitor must be large enough to prevent the long data pulses from sagging at the comparator input. Capacitive coupling is used for two reasons. The first is to prevent the change in dc offset of the base-band amplifier from false triggering the comparator. The second is to prevent the dc output from the detector, produced by an in-band CW or FM interfering signal, from triggering the comparator while allowing changes in dc level, due to the desired signal, to pass through to the comparator input. Note that a resistor, R4, is connected between the comparator input and ground on the 916.5 MHz boards. This will be explained in conjunction with the discussion on Pin 5. Pin 4 is a dc ground. Pin 5 is the comparator threshold override pin. If this pin is left open, the threshold voltage for the comparator is 25 mV. If it is shorted, the threshold voltage is zero volts. The 916.5 MHz RX receivers have a nominal sensitivity level of -80 dBm whereas the 300 and 400 MHz RX's have a nominal sensitivity level of -100 dBm. The internal 25 mV threshold level is very desirable for the lower frequency, full sensitivity receivers to reduce spurious noise at the comparator output. A zero volt threshold is desirable for the 916.5 MHz receivers to obtain the maximum sensitivity possible. Thus, Pin 5 is grounded for 916.5 MHz receivers and left open for the lower frequency receivers. Spurious noise on the comparator output of the 916.5 MHz receivers is avoided by using a 10 megohm resistor, R4, from Pin 3 to ground. This resistor effectively reduces the dc offset on the comparator input which is equivalent to using a very low threshold level. Pin 6 is the reference voltage output of the power supply included in the custom IC used in the RX. This pin must be bypassed by a

1 uF capacitor, C4, to avoid comparator switching noise in the base-band amplifier. Pin 7 is the comparator output or data output. The comparator is capable of driving a single CMOS gate input. Pins 8 and 9 are primarily RF grounds. Pin 10 is the RF input port of the RX device. This port is to be driven from a 50 ohm source.

AGC/Antenna Switch- The out-of-band interfering signal rejection of the amplifier-sequenced receiver architecture is excellent and allows the receiver to perform in the presence of large interfering signals without range degradation. However, there are some applications that will encounter in-band interference. The majority of in-band interference encountered is CW and primarily comes from unintentional radiators such as clock harmonics from computers or local oscillators from superheterodyne receivers. The AGC circuit discussed here is primarily intended for CW or FM in-band interfering signals. These are of particular concern in an office environment. The RX receiver, as discussed in the previous section, has capacitive coupling between the base-band amplifier output and the comparator input. Thus, the dc level generated in the detector and base-band amplifier by either an FM or a CW signal is blocked from the comparator input and only the desired signal passes. The limiting factor is the dc level at which the detector and its associated base-band amplifier saturate. The lower frequency RX's (433.92 MHz) saturate at an in-band CW or FM carrier level of approximately -80 dBm. The 916.5 MHz RX's saturate at a level of approximately -50 dBm. The AGC circuit used on the data radio board is simply intended to prevent saturation of the detector and base-band amplifier by keeping such in-band interfering signals below the saturation level at the receiver input.

Referring to the schematic diagram for the data radio board, an RF attenuator is placed between the antenna and the receiver input. Transistors Q2 and Q3 serve as the main RF attenuator elements. Each has an attenuation range of approximately 20 dB. Thus, with Q2 in series with the RF line and Q3 in shunt to ground, this two stage attenuator has a total AGC range of approximately 40 dB and an "on" insertion loss of 1 dB. This effectively extends the range over which the receiver can operate without saturation by 40 dB. The reference voltage for the AGC circuit is derived from the VRef Pin 6 of the RX.

This reference voltage is very constant from one receiver IC to another. The signal level dependent input to the AGC circuit is derived from the base-band output of the receiver which is dc-coupled to the internal RF detector. The dc offset of the base-band output, with no signal applied to the receiver, can vary 25 or 30 mV from one receiver IC to another. This makes it necessary to include a 500 kohm potentiometer, R10, in the circuit to adjust the engage point for the AGC. The VRef voltage and the base-band signal are both applied to the inverting and non-inverting inputs, respectively, of the operational amplifier, U1A. The data is filtered out of the base-band signal using C8. R7 sets the dc gain of the amplifier and C7, in conjunction with C8, set the time constant or corner frequency of the AGC circuit. The time constant of the AGC circuit was chosen to be long enough to avoid a response to the individual data bits of the desired signal. The output of U1A is applied to the bases of Q1 and Q3 through diode D1. Thus, as the interfering signal level increases, transistors Q1 and Q3 are gradually turned on. Transistor Q3 shorts the signal to ground and transistor Q1 presents the output impedance of the unpowered HX device to ground at the antenna input to add additional RF attenuation. The PTT line presents 50 kohms to ground in the receive mode, so it does not affect the AGC voltage applied to Q1 and Q3. The output of U1A is also applied to the inverting input of U1B. This operational amplifier merely serves as an inverter to drive the series RF attenuator, Q2. Thus, as Q1 and Q3 are gradually being turned on by an increasing signal level, Q2 is gradually being turned off. This describes the operation of the AGC circuit.

As discussed in the preceding "Transmitter" discussion, the RF attenuators Q1, Q2 and Q3 also serve as the transmit/receive RF switch for the data radio board. In the transmit mode, the PTT line is pulled high, overriding the AGC circuit by directly biasing the bases of Q1 and Q3 on and turning the base of Q2 off through R15 and U1B. This connects the transmitter to the antenna port and disconnects the receiver from the antenna port. In the receive mode, PTT is low, allowing the receiver to be connected to the antenna port with its input level controlled by the AGC circuit only.