Operational Theory of the PRC-001 ClearNet Proximity Reader Controller

The PRC-001 "ClearNet" Proximity Reader Controller is a new access control reader product being introduced by ISONAS Incorporated. This device is unique because it has the ability to make access control decisions on a standalone basis due to its onboard relay and monitor inputs and outputs, and it can be seamlessly connected together controlled by a PC host system to make the access control decisions in a network mode. An individual with a valid RF/ID transponder in a card or tag has the ability to enter through a door fitted with the PRC-001 door access reader.

This reader controller is designed to be mounted to a door mullion that is made of any material including metal, since the design is metal compensated. The PRC-001 is powered by a 12 volt DC power source and can communicate directly to a PC host system through its RS-485 serial communication interface. The communication between an RF/ID card or tag transponder, and a reader controller is accomplished via magnetic coupling between the antennae on both the transponder and reader.

Description of the RF System:

The ClearNet Reader Controller system block diagram is shown in Figure 1. A 7.3728 MHz oscillator crystal in the PRC-001 generates a 125 kHz signal which drives a 1.5" x 3.5" loop antenna made out of insulated copper wire in a freestanding coil attached to the circuit card assembly. When a card/tag with an RF/ID transponder is within 2 inches from the surface of the reader face, its antenna coil picks up the 122.9 kHz magnetic field, which is rectified in the transponder ASIC, powering it up. The transponder ASIC divides the 122.9 kHz clock frequency by 8 and 10, then emits its own unique ID code in the form of, 15.4 kHz and 12.3 kHz frequency-shift keyed (FSK) signal bursts. (The RF system can also detect ASK signal bursts at 3.8 kHz from transponder ASICs in cards or tags). The 15.4 kHz and 12.3 kHz signals represent data in the form of 1's and 0's respectively. A microcontroller IC performs the task of identifying this signal and determines the 16 bit preamble from the meaningful 32 bits through error checking and noise cancellation. This received data from a valid card or tag is then passed on through the RS-485 communication interface to a PC host system, or is validated internally with resident memory (EEPROM) inside the reader to grant or deny access.

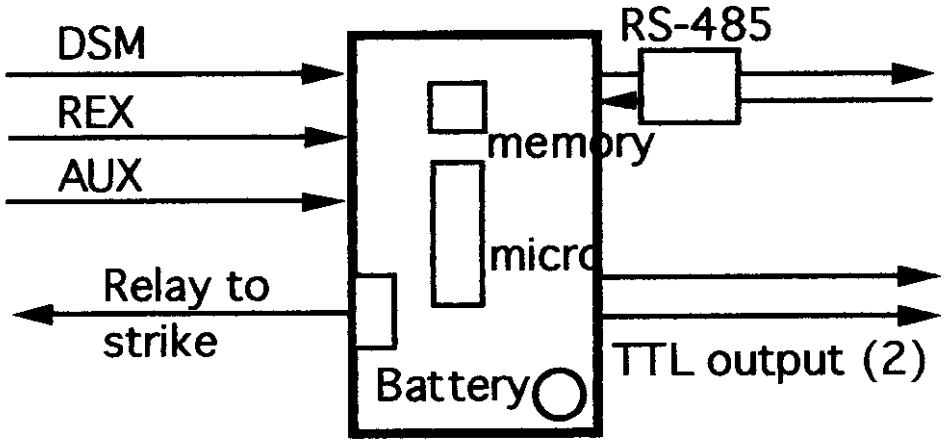

Figure 1 - System Block Diagram of ClearNet Reader

Description of the Microcontroller System:

The microcontroller block diagram is shown in Figure 2. An 8 bit microcontroller (PIC16C73) runs on a 7.3728 MHz clock signal that is divided by 60 to generate a 122.9 kHz pulse. This 122.9 kHz signal is fed to the transmitter. The microcontroller also divides this generated 122.9 kHz pulse by 8 and 10 to sample the received signal from an external transponder, or by 32 to sample a received signal using ASK. This detection decision is based on proprietary algorithms which then determines the proper divisor to use for analysis of the return signal. The digitized data received is then identified by the microcontroller. The microcontroller verifies the start of the signal by checking the preamble bits and reads the meaningful data bits. It checks for errors and sends this card/tag identification code to a network host via an RS-485 interface chip when polled, or to the onboard memory (EEPROM) to verify the data bits. The microcontroller also controls two bi-color LEDs, a beeper, a relay and two TTL outputs. The microcontroller also responds to three monitor inputs and a tamper switch.

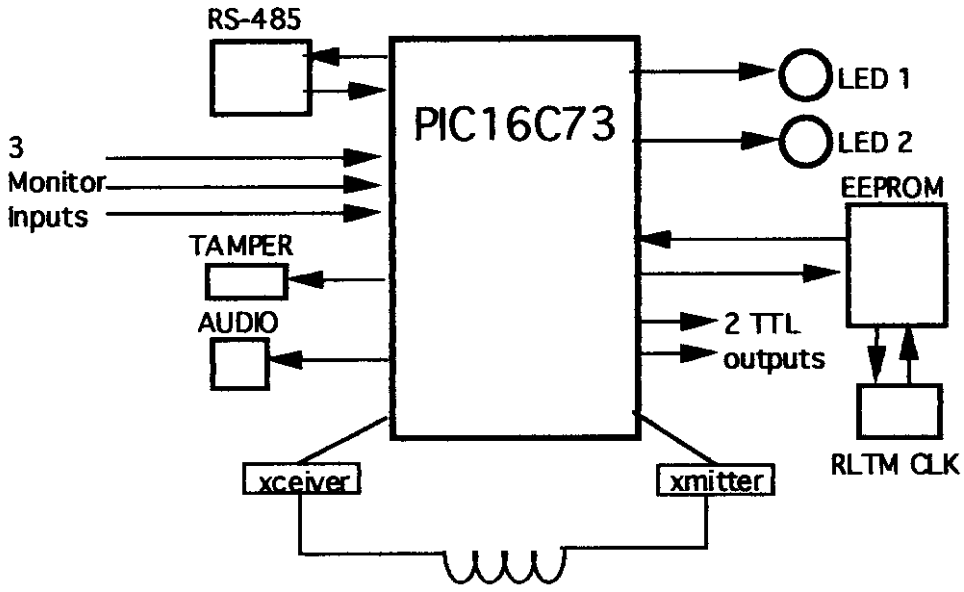

Figure 2 - Microcontroller Block Diagram