Technical Description and Block diagram of 8022N pager - RF part

A) Theory of Operation

The RF demodulation process is based on conventional double conversion superheterodyne method. The first IF (intermediate frequency) is selected to be 21.4MHz. The second IF is 455KHz. The demodulation process is done by the FM-IF IC (KA8514) or TA31145. The FM-IF IC includes voltage regulator, low battery detection circuit, mixer, oscillator, FSK comparator and limiting IF amplifier. The operation principles of this paging receiver are depicted in Figure 2 and the schematics.

B) Antenna Circuit and Amplifier

Antenna of the pager is constructed by silver plated copper loop. By proper tuning a variable capacitor, the loop antenna will be matched to the amplifier and hence the signal picked up would be amplified. The amplified RF signal is then applied to a mixer through a wide-band SAW filter. The SAW filter is mainly used for first image signal suppression.

C) First Local Oscillator and Mixer

The oscillating signal is generated by a crystal oscillator with one stage of frequency multiplier. The LO signal is then mixed with the RF signal by mixer to generate the 21.4MHz IF signal. The 21.4MHz crystal filter is used to filter the 21.4MHz IF signal with second image rejection purpose.

D) FM-IF Circuit

The FM-IF IC converts the 21.4MHz IF signal to 455KHz second IF by the internal second mixer with externally connected crystal of either 20.945MHz. Ceramic filters are used to improve the adjacent channel rejection response. The 455KHz IF signal will then be amplified, limited and discriminated by a ceramic resonator to the base-band analogue signal. Inside the chip there is a level comparator for converting the analogue signal to the digital data. Besides, the chip can power up the whole RF front end with a regulated 1Vdc. With the low voltage alarm function, the MCU can detect the battery from running flat.

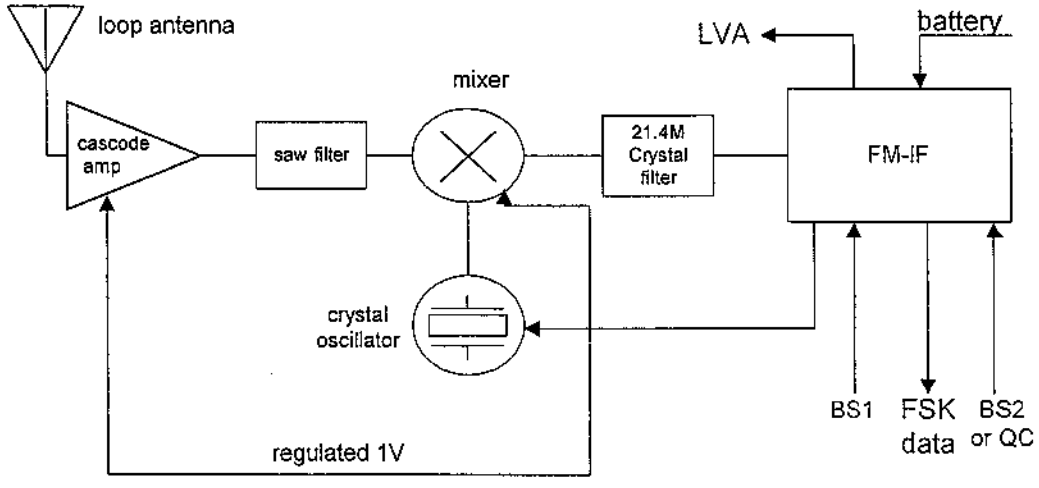

Figure 2: Block diagram of 2-level FSK RF demodulation architecture.

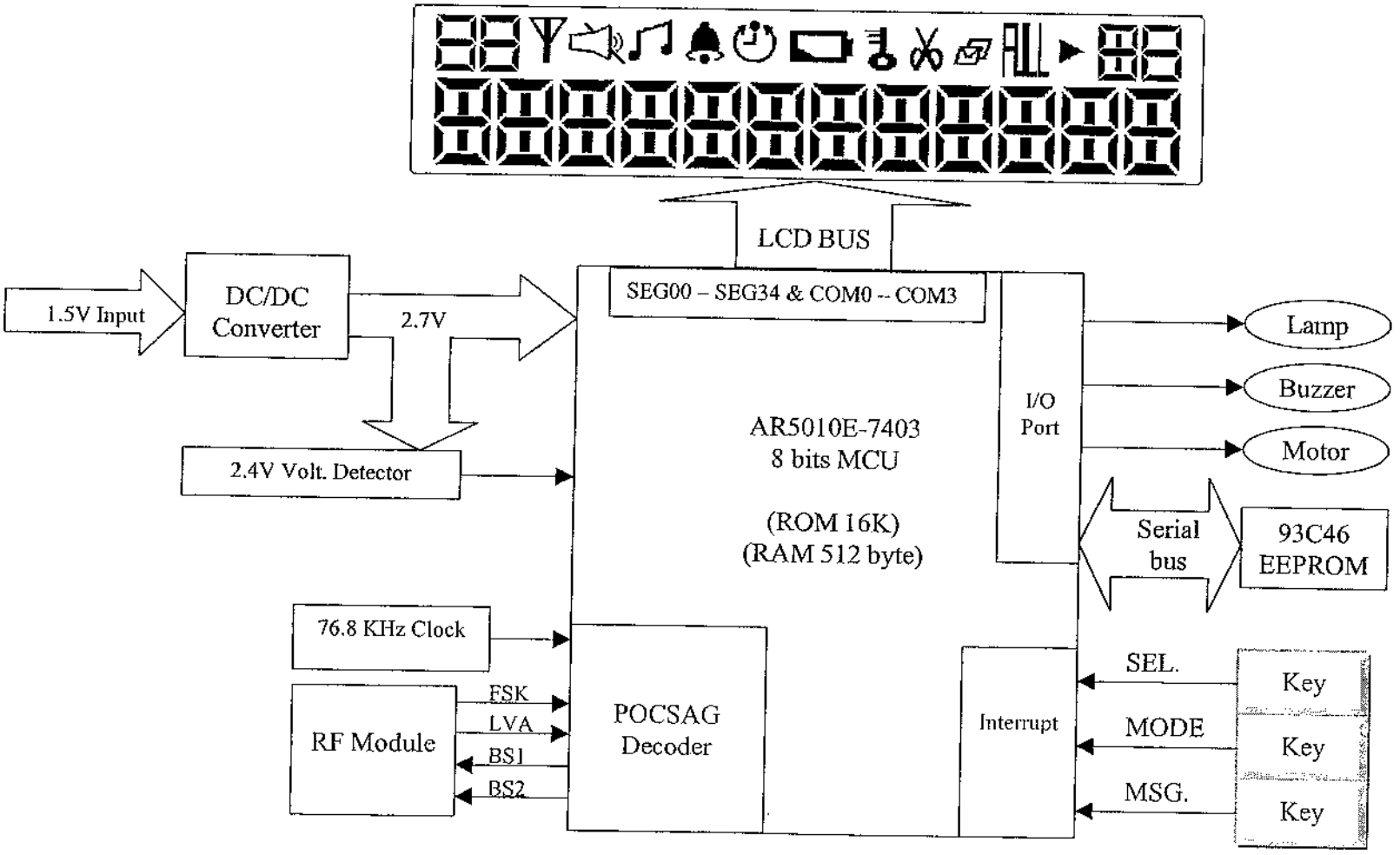

Figure 1 Block diagram of 8022N digital module