8015N Digital Board Hardware Description

A) Overview

The 8015N Pager is an alpha-numeric display FLEX pager. It has two keys and a 96 x 7 dots matrix with clock and 7 static icons LCD display. It is controlled by SAMSUNG KS88C2064 8-bits MCU. The FLEX signal data is received by the FLEX decoder Motorola XC68175 IC (or TI TLV5591) and will store to the memory (RAM) of the MCU. The block diagram of digital module is shown in figure 1. The user can use the key to read the received message that will be displayed on the LCD glass. When the new user message is arrived, the pager can set the alert signals to user such as buzzing sound or vibration from vibrator.

B) FLEX decoder

The FLEX decoder is Motorola XC68175 IC or TI TLV5591 using a FLEXchip signal processor to connect the RF module to MCU of the digital module. The decoder will control the RF module ON & OFF and receive the 2 bits FSK data. The decoder will decode the FSK data and acknowledge to the MCU if CAP code (address) is correct. When the new message arrive, the decoder will generate the interrupt to the MCU. The decoder will also acknowledge the MCU about the low battery condition if voltage is below 1.1V. The 76.8K Hz crystal is used to drive the FLEX decoder. FLEX chip will communicate to MCU by 32 bits SPI.

C) MCU

The core MCU is 8-bits SAMSUNG KS88C2064 which will handle all the work of pager. The MCU has an initial procedure that read the initial setting from EEPROM and setup the I/O device. The MCU will receive the RF signal through RF module and FLEX decoder. After MCU receive the signal with respect address, it will turn the buzzer on or motor on to acknowledge the user. The user can access the pager by the key input to read the message from the LCD and setup the pager function. The 2 MHz resonator and 32.768 KHz crystal is used to drive the MCU. The DC/DC converter step up the battery voltage 1.5V to supply voltage 2.7V for MCU, FLEX decoder, EEPROM and LCD module. A 2.4V voltage detector with a RC delay circuit is used as reset circuit to the MCU.

D) I/O DEVICE

LCD -	A 96 x 7 dots matrix with clock and 7 static icons LCD display is used. It can display up to 16 alpha-numeric character. It can be checked in self-test mode.
Buzzer & Motor -	is used to acknowledge the user.
Lamp -	is used to see the LCD in darkness place.
Key -	The key pad is a input device. In 8015N, there are two input keys.
EEPROM -	93C56, 2K bit serial EEPROM, is used to save the initial setting.
DC/DC converter -	The voltage converter provide the necessary voltage level from 1.5V battery. Current voltage of DC/DC converter output is 2.7V.

A) Theory of Operation

The RF demodulation process is based on conventional double conversion superheterodyne method. The first IF (intermediate frequency) is selected to be 21.4MHz. The second IF is 455KHz. The demodulation process is done by the FM-IF IC (KA8515) or TA31149. The FM-IF IC includes voltage regulator, low battery detection circuit, mixer, oscillator, FSK comparator and limiting IF amplifier. The operation principles of this paging receiver are depicted in Figure 2 and the schematics.

B) Antenna Circuit and Amplifier

Antenna of the pager is constructed by silver plated copper loop. By proper tuning a variable capacitor, the loop antenna will be matched to the amplifier and hence the signal picked up would be amplified. The amplified RF signal is then applied to a mixer through a wide-band SAW filter. The SAW filter is mainly used for first image signal suppression.

C) First Local Oscillator and Mixer

The oscillating signal is generated by a crystal oscillator with one stage of frequency multiplier. The LO signal is then mixed with the RF signal by mixer to generate the 21.4MHz IF signal. The 21.4MHz crystal filter is used to filter the 21.4MHz IF signal with second image rejection purpose.

D) FM-IF Circuit

The FM-IF IC converts the 21.4MHz IF signal to 455KHz second IF by the internal second mixer with externally connected crystal of either 20.945MHz. Ceramic filters are used to improve the adjacent channel rejection response. The 455KHz IF signal will then be amplified, limited and discriminated by a ceramic resonator to the base-band analogue signal. Inside the chip there is a level comparator for converting the analogue signal to the 2 bits digital data. i.e. FSK1 and KSF2. Besides, the chip can power up the whole RF front end with a regulated 1Vdc. With the low voltage alarm function, the MCU can detect the battery from running flat.

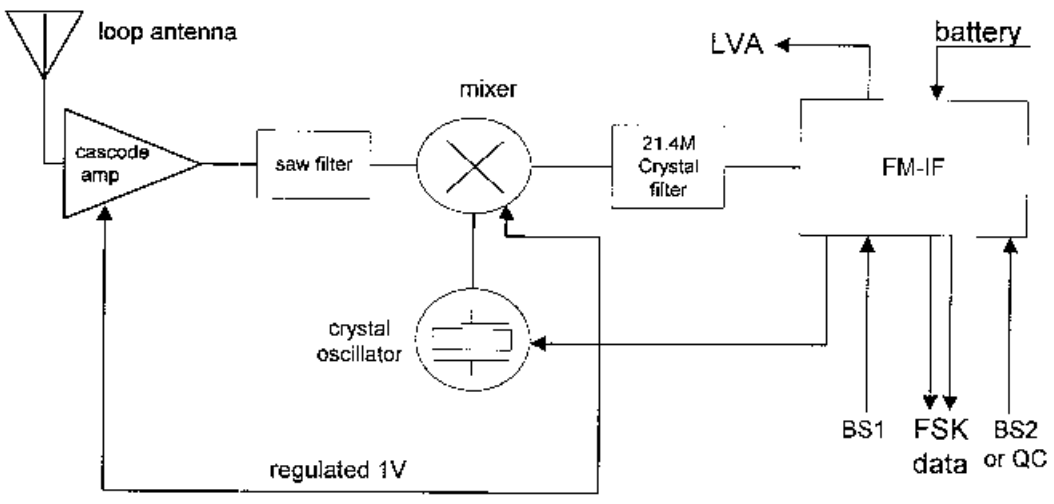

Figure 2: Block diagram of 2-level FSK RF demodulation architecture.