BJ-UV99 CIRCUIT DESCRIPTION

I. Receiver Signal Path

1. RF Signal

■ UHF **Signal**

UHF signal is passed through a high-pass filter network and a low-pass filter network to the antenna switch diodes D1, D2, and D3, then passed through BPF tuned filter circuit (D29, D30) to the UHF RF amplifier T18. The amplified UHF signal is passed through another BPF tuned filter circuit (D31, D32) to the first mixer T19. Meanwhile, the UHF local signal from the UHF-VCO (Q7) is delivered to first mixer T19, yielding the 38.55MHz UHF first IF.

■ **VHF Signal**

VHF Signal is passed through a low-pass filter network and a high-pass filter network to the antenna switch diodes D3, D4, and D6, then passed through BPF tuned filter circuit (D44, D45) to the VHF RF amplifier T20. The amplified VHF signal is passed through BPF tuned filter circuit (D33, D34) to the first mixer T21. Meanwhile, the VHF local signal from the VHF-VCO (Q6) is delivered to first mixer T21, yielding the 38.55MHz VHF first IF.

2. IF and AF Signal

The 38.55MHz UHF and VHF first IF is passed through the switch (D9, D11) to the crystal filter (FL1, FL2), which strips away unwanted mixer products, then is passed through IF amplifier T35 to the IF IC U3. Meanwhile, the output of 13.0 MHz TCXO crystal Y1 is multiplied threefold by T36 to provide the 39MHz

second local signal, then delivered to the IF IC U3. Within the IF IC U3, the 39MHz second local signal is mixed with the 38.55 MHz first local signal to produce the 450 KHz second IF.

The 450 KHz second IF is delivered to the ceramic filter FL3 which strips away all but the desired signal, then it passes through the IF amplifier within U3 to the ceramic discriminator CR1, which removes any amplitude variations in the 450 KHz IF signal before detection of speech.

The filtered audio signal passes through the CPU (U4) to process, then it is delivered to the audio switch VR4, which adjusts the audio sensitivity. After being delivered to U4 to amplify, it is applied to the loudspeaker.

3. Squelch Control

When no carrier is being received, noise at the output of the detector stage in U3 is amplified and band-pass is filtered by the noise amp section of U3. The resulting DC voltage is delivered to CPU (U4), which compares the squelch threshold level to that which set by the settings menu.

While no carrier is being received, CPU will deliver a control level, which passes through T25, and T40, to disable the audio output from the speaker.

II. Transmitter Signal Path

1. AF Signal

The speech signal from the microphone is delivered to the AF amplifier U11. The amplified speech signal is delivered to the limiting amplifier T13 and T14 to prevent over-modulation, and then is delivered to a low-pass filter network.

■ UHF

The adjusted speech signal is delivered to varactor diode D24, which frequency modulates the transmitting VCO, made up of UHF-VCO Q7.

The modulated transmit signal is passed through buffer amplifiers Q1, Q2 and diode switches D7, D8 to the pre-drive amplifier T7.

The amplified transmit signal from T7 is passed through the driver amplifier T5 to the driver amplifier T3, then finally amplified by power amplifier T1, providing up to 4 Watts of power output. These three stages of the power amplifier's gain are controlled by the APC circuit.

The 4-Watt RF signal is passed through a high-pass filter network to the antenna switch D1, D2, and D5, and then passed through a low-pass filter network and another high-pass filter network to the ANT jack.

■ VHF

The adjusted speech signal is delivered to varactor diode D25, which frequency modulates the transmitting VCO, made up of VHF-VCO Q6.

The modulated transmit signal is passed through buffer amplifiers Q5, Q4 and diode switches D10, D12 to the pre-drive amplifier T8.

The amplified transmit signal from T7 is passed through the driver amplifier T6 to the driver amplifier T4, then finally amplified by power amplifier T32, providing up to 5 Watts of power output. These three stages of the power amplifier's gain are controlled by the APC circuit.

The 5-Watt RF signal is passed through a low-pass filter network to the antenna switch D3, D4, and D6, and then passed through a high-pass filter network and another low-pass filter network to the ANT jack.

2. APC (Automatic Power Control) Circuit

■ UHF

The power amplifier output is rectified by resistance network then delivered to APC U8, as a DC voltage which is proportional to the output level of the power amplifier.

At U8, the rectified DC voltage from the power amplifier is compared to the reference voltage from the main CPU U4 to produce a control voltage, which regulates the supply voltage to the driver amplifier T3 and power amplifier T1, so as to maintain stable output power under varying antenna loading conditions.

■ VHF

The power amplifier output is rectified by resistance network then delivered to APC U8, as a DC voltage which is proportional to the output level of the power amplifier.

At U8, the rectified DC voltage from the power amplifier is compared to the reference voltage from the main CPU U4 to produce a control voltage, which regulates the supply voltage to the driver amplifier T4 and power amplifier T32, so as to maintain stable output power under varying antenna loading conditions.

3、PTT (Push to Talk) Circuit

■ UHF

When the PTT switch is pressed, the CPU U4 receives the “PTT” command.

When the “PTT” command is received, the CPU U4 delivers control signal, which activates the TX switch, made up of Q12, Q13 and Q23.

When the TX switch is activated, it controls the antenna switch diodes D1, D2, and D5, diode switches D7 and D8, and APC switches T30 and T31, which activate the UHF transmitter circuit.

■ VHF

When the PTT switch is pressed, the CPU U4 receives the “PTT” command.

When the “PTT” command is received, the CPU U4 delivers control signal, which activates the TX switch, made up of Q12, Q13 and Q21.

When the TX switch is activated, it controls the antenna switch diodes D3, D4, and D6, diode switches D10 and D12, and APC switches T28 and T29, which

activate the VHF transmitter circuit.

III. PLL Circuit

A portion of the output from UHF-VCO Q7 is passed through buffer amplifier Q404 to the programmable divider PLL IC U12, where it is divided according to the frequency dividing data associated with the main CPU U4. It is then sent to the phase comparator.

A portion of the output from VHF-VCO T408 is passed through buffer amplifier T405 to the programmable divider PLL IC U12, where it is divided according to the frequency dividing data associated with the main CPU U4. It is then sent to the phase comparator.

The phase comparator U12 compares the phase between the frequency-divided oscillation frequency of the VCO circuit and the comparative frequency, and its output is a pulse corresponding to the phase difference. This pulse is integrated by the loop filter into a control voltage (VCV) to control the oscillation frequency of the VCOs.