TELSON INFORMATION & COMMUNICATION CO., LTD.

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THEORY OF OPERATION

(MODEL:PA60)

I . FREQUENCY GENERATION

The frequency generation circuit is composed of the synthesizer U401 and the VCO. The block diagram illustrates the interconnect and support circuitry used in the design. Refer to the schematic for reference designator.

The supplied voltage for the synthesizer is the regulated 4.0 V which also serves the rest of the radio. In addition to the VCO, The synthesizer must be interconnected with the logic and AF filter circuitry. Programming for the synthesizer is accomplished through the clock, data and strobe signals (pin 6, 7 and 8) from the microprocessor U701.

A serial data is sent whenever the synthesizer is programmed. A DC 4V signal from pin 1 indicates to the microprocessor that the synthesizer is locked, and unlock is indicated by a low voltage on this pin. The audio signal from the AF filter is modulated by D402 of VCO.

PLL FREQUENCY SYNTHESIZER

The U401(PLL IC) includes all the functions such as the phase comparator, the programmable divider, the lock detector, and reference oscillator.

The synthesizer uses a 21.25 MHz crystal (X401) to provide the reference frequency for the system.

The loop filter, composed of R404 – 407, C408 - 410 provides the necessary DC steering voltage for the VCO as well as filtering of spurious signals from the phase detector. The pre-scaler for the PLL is internal to U401 with the value determined by the frequency band of operation.

The TCXO(21.25MHz) is the temperature compensation circuit to maintain the frequency within the allowable error range even on -20℃.

The phase comparator send out the output power to the loop filter through pin14 of the U401. When phase comparator detects phase difference(unlock), LD terminal (pin5) outputs "LOW". When phase comparator locks, LD terminal outputs "HIGH".

V C O

The VCO, in conjunction with the synthesizer (U401), oscillates 462.5625 MHz to 467.7125 MHz in the transmit mode and 441.1625 MHz to 446.3125 MHz in the receive

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mode. The VCO consists of the Colpitts oscillator of the Q402. A sample of the RF signal from the enabled oscillator is routed from Q403, C424, through to the pre-scaler input. After frequency comparison in the synthesizer, a resultant control voltage is supplied into the VCO. This voltage is a DC voltage between 1.0 and 3.5 volts when the PLL is locked on specified frequency.

In the receive mode, the RF signal through Q403 is the local oscillator RF injection and it is applied to the first mixer at Q103.

In the transmit mode, the RF signal at Q403 is run to the input of the pre-drive transistor (Q501 base). This RF signal is the Tx RF injection. Also in transmit mode, The audio signal to be frequency modulated onto the carrier is received by the transmit VCO modulation circuitry at audio in.

During receiving, a relative low frequency should be oscillate compared to transmission. Therefor, the D401 is adversely biased by the Q401, and as a result, the C414 which is added in serial to the resonance circuit of the VCO is added to oscillate the desired reception frequency.

Ⅱ. RECEIVER

The receiver of the UHF consists of 4 major blocks each: the Front-end ,the Mixer , the First IF and the second IF/Demodulator IC.

FRONT - END

The UHF Front-end contains two separate circuits ; the RF Amplifier and SAW Filter. The RF Amplifier, consist of two transistor Q101 and Q102 is the cascade in all-bipolar form which is also referred to as common · emitter-common · base (CE-CB) connection. This Amplifier has approximately 20dB gain owing to high output impedance , a noise figure of approximately 3dB and is supplied by the receive 4.0V line.

The SAW Filter is BPF of high stability and reliability with good performance and is fixed-tuned design to eliminate the need for tuning and to provide narrow-band operation. The 3dB bandwidth is approximately 6MHz, centered on 465MHz with an insertion loss of approximately 4dB.

The net-gain from the Front-end selection is approximately 20dB in the center of the band, falling to approximately 4dB at band edges, with a center band noise figure of approximately 5.5dB.

MIXER

The Mixer operates with a local oscillator drive level minimum -4dBm. The mixer provides excellent isolation between the ports and operates over a large bandwidth. The received signal is mixed down to 21.7MHz, the frequency of the first IF.

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FIRST IF

The first IF consists of a 21.7MHz crystal filter and amplifier. The crystal filter provides second image protection and intermodulation protection with approximately 3.75kHz bandwidth(3dB) for 12.5kHz models. The IF Amplifier, Q104, provides approximately 10dB of gain at 21.7MHz.

SECOND IF/DEMODULATOR IC

The Second IF/Demodulator IC(DBL5018-V; U201) accepts the 21.7MHz IF input and mixes it with a second local oscillator signal(21.25MHz). This produces a second IF of 455kHz, which is filtered externally by a ceramic filter and passed back into the IC for amplification.

The signal is passed to a quadrature detector for demodulation and, after being filtered, is passed to the output. The IC, along with some external components, controls the squelch sensitivity, squelch tail, and hysteresis. Internal variable resistor, VR201, controls the noise squelch setting.

Ⅲ. TRANSMITTER

The PA60 transceiver is composed of five basic circuits : a Pre-Driver, Driver, Final Amplifier, Antenna Switch and a Harmonic Filter. Refer to the block diagram and the schematic for more information.

POWER AMPLIFIER

The Power Amplifier consists of three stages : a Pre-Diver, Driver, Power Amplifier. It requires a supply voltage of 6.0 volts, and is capable of supplying maximum 0.5W(ERP).

POWER CONTROL

R502 and 505, which control the current of Pre-driver Amp(Q501, 502), can control the bias input level of final TX power Amp(Q503, 504). And the input level can control the TX power level.

ANTENNA SWITCH

The antenna switch circuit consists of two pin diodes (D501 and D101), In the transmit mode, POW-TX LINE is applied to the circuit to bias the diodes "on". The shunt diode (D101) shorts out the receiver port and the PI network, which operates as a quarter wave

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transmission line and transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter.

In the receive mode, The diodes are both off, hence, there exists a low attenuation path between the antenna and receiver ports.

HARMONIC FILTER

The harmonic filter consists of part of C102, L101, C103, L102, C104, L103, C105. The design of the harmonic filter is 7th order chevyshev filter with 0.1dB ripple. This type filter has the advantage that it can give greater attenuation in the stop-band for a given ripple level.

Ⅳ. AUDIO PATHS

RX AUDIO PATH

Audio from pin9 of U201(IF IC) pass through de-emphasis U202(NJM386). After de-emphasis and volume adjustment by MCU.(pin13, 14, 15, 16), it is fed to the Audio Power Amplifier, U202. This is a Bridged-tied Load amplifier with a fixed gain of 40dB, developing 250mW output at less than 10% harmonic distortion into the 8Ω internal loudspeaker with 6V. Maximum audio power output is approximately 180mW.

TX AUDIO TONES

The TX audio is fed from the microphone to Mic Amp, U301 which contains the pre-emphasis components. The gain of U301 is limited to prevent over-deviation. The output level is adjusted by the Max Deviation circuit, VR301, and it is fed into into the TX VCO.