Section 3
Technical description

The ST450 comprises the following modules:

a.	The transmitter motherboard	WD1581
b.	The VCO module	WD1592

3.1 TRANSMITTER MOTHERBOARD

Refer to circuit diagram WD1581/001 and component overlay WD1581/XX2 at the rear of this manual.

3.1.1 INPUT AMPLIFIER

The modulation input is applied to IC4a and IC4b which comprise the variable gain input amplifier/clipper. In analogue mode, both op amps operate in parallel as a virtual earth inverting amplifier with gain set by RV1. PL1 selects a flat frequency response, a pre-emphasis network (C11/R4) or direct connection for squarewave inputs.

Removing PL4 and selecting PL1-2 allows IC4 to act as a window comparator with a window of 2.5V ±0.5V, for use with duobinary (three level) digital inputs.

3.1.2 AUDIO FILTERING

IC5 and IC6 restrict the modulation bandwidth in order to limit the transmitted RF energy in the adjacent channels. IC5 is a transconductance (current output) amplifier driving a capacitive load C46. This results in a defined maximum slew rate stage or slope limiting filter. The output current and hence slew rate is preset by RV3. TR9 provides bias temperature compensation. IC6a is a 3 pole Sallen and Key audio filter with a cutoff of about 3kHz. Removing solder links S1, S2 increases bandwidth for use with high speed GMSK modems. IC6b forms a variable gain buffer amplifier.

3.1.3 MODULATION

To extend the modulation bandwidth below the loop frequency of the simple phase-locked-loop in the WD1592 VCO module, modulation is applied to both the VCO and the reference TCXO (a technique known as dual point modulation).

3.1.4 FREQUENCY REFERENCE

The frequency reference for the phase-locked-loop is provided by either U1 TCXO (for normal UHF units) or the VCXO around TR10, (X2 for VHF and wideband use). The output in either case is fed to the WD1592 VCO module.

3.1.5 RF STAGES

The RF signal from the WD1592 VCO module is fed via D14 to the buffer amplifier TR14. Diodes D14 increase isolation from the VCO in hot standby. TR14 provides a common emitter stage with emitter resistor biasing. The base bias of TR14 is derived from the switched power amplifier rail via the following stage.

TR11 and TR12 are a parallel pair of common emitter wideband driver amplifiers. TR13 provides temperature stable bias with output power being adjusted by RV4 (high-power mode). A reactive match into the final is used (C56, L13) .

The output from the driver amplifiers is fed to the power amplifier TR8 operating from a nominal 7V rail. The output from the power amplifier is fed via the matching capacitors C29,C26 to the output low-pass filter L1, L3, L4 and L7. Another pin diode switch D5 is implemented to further enhance hot standby RF isolation. Alternative inductors (L13/12, L4/5) are provided to support the VHF version.

3.1.6 POWER CONTROL

In high power mode, the output power is adjusted by altering the driver current/output level via RV4, the class C output stage operating from the +7V provided by the dropout regulator TR7, IC2a.

In low power mode RV2 reduces the reference voltage to IC2a and hence the power amplifier/driver supply rail. With reduction in output power the collector current in the final stage falls until IC2b is brought into play. This constitutes a current source with sense resistor R38, stabilising power amplifier TR8 biasing at low output powers. RV2 provides adjustment from 1mW to full output.

Diode D3 ensures base bias to TR8 is off in cold standby.

In the 1W output version R56 is removed, raising the PA supply to approximately 9.5V, and an MRF 557 output device is used.

3.1.7 VOLTAGE REGULATOR

An integrated regulator IC1 provides the +5V rail. This device is controlled by STBY input (PL2-3)

3.1.8 CONTROL PROCESSOR

Synthesiser programming and switching functions are achieved by the PIC16C84 micro IC3. All channel setup and frequency information is contained on internal EEPROM on this chip which can be re-programmed via the connector PL5. One of the two channel select inputs (CS1) includes the buffer TR3 to allow C5 to double as an RS232 input in serial control mode. A 3.58MHz ceramic resonator provides the processor clock.

3.2 VCO MODULE

Refer to circuit diagram WD1592/001 and component overlay WD1592/001 at the rear of this manual.

VCO TR6 is a low noise colpitts oscillator using a high Q tank inductor L6 and low loss varicaps D5 and D6. Emitter current is cascaded through buffer TR5 which with control transistor TR4 provides constant current biasing for the entire oscillator. L5/C34/C42 provide the decoupling required for the VCO. Diodes D3a and D3b improve bias stability over temperature. Varicap D6 provides a low sensitivity input for baseband modulation of the VCO.

The buffer VCO output is amplified by TR3 then split between synthesiser IC1 and output buffer TR1. The output buffer current is cascaded into the synthesiser (which draws up to 8mA) and the preceding buffer TR3. As the emitter voltage of TR1 provides the VDD rail for IC1 (at about 2.8V) a temperature stable base bias network built around TR2 is used.

The output level is adjusted by RV1 which sets the standing current through both TR3 and to a degree TR1. The output buffer TR1 produces 1.5mW for its resistive collector match.

Diode D7 (turned on by external current sink) reduces the output level from VCO when in hot standby mode. C7 is only fitted on the SR450 oscillator.

3.2.1 SYNTHESISER

IC1 provides the phase comparator, lock detector, prescaler and A/M/R registers. The device is rated to 1.1GHz at 8mA from a 2.7V rail.

An on chip current output charge pump drives the loop filter around C23 to control the VCO. The charge pump operates directly from the +5V rail to provide a useful control voltage range from 1 to 3.5V.

The synthesiser is controlled over a 3 wire synchronous bus (clock/data/strobe) and is programmed by a 36 bit control sequency from the processor. In normal operation the data input pin is used as a lock detector output via R10 and the lock detect circuitry around D1.

The WD1592 is housed in its own shielded enclosure to maximise VCO isolation.